SHARP

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To; _____

PRELIMINARY

SPECIFICATIONS

Product Type 16M (x8/x16) Flash Memory + 2M (x8) SRAM

LRS1329A

Model No. (LRS1329A)

This device specification is subject to change without notice.

*This specifications contains 32 pages including the cover and appendix.
*Refer to LH28F400BV, LH28F800BV, LH28F160BV Series Appendix (FUM99903).

CUSTOMERS ACCEPTANCE

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  •Office electronics
  •Instrumentation and measuring equipment
  •Machine tools
  •Audiovisual equipment
  •Home appliance
  •Communication equipment other than for trunk lines

  (2) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.

  •Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
  •Mainframe computers
  •Traffic control systems
  •Gas leak detectors and automatic cutoff devices
  •Rescue and security equipment
  •Other safety devices and safety equipment, etc.

  (3) Do not use the products covered herein for the following equipment which demands extremely high performance in terms of functionality, reliability, or accuracy.

  •Aerospace equipment
  •Communications equipment for trunk lines
  •Control equipment for the nuclear power industry
  •Medical equipment related to life support, etc.

  (4) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.

- Please direct all queries regarding the products covered herein to a sales representative of the company.

Contents

1. Description

The LRS1329A is a combination memory organized as 2,097,152 × 8 / 1,048,576 × 16 bit flash memory and 262,144 × 8 bit static RAM in one package.

Features

- Power supply • • • • 2.7V to 3.6V
- Operating temperature • • • • -25°C to +85°C
- Not designed or rated as radiation hardened
- 72 pin CSP (LCSP072-P-0811) plastic package
- Flash memory has P-type bulk silicon, and SRAM has P-type bulk silicon.

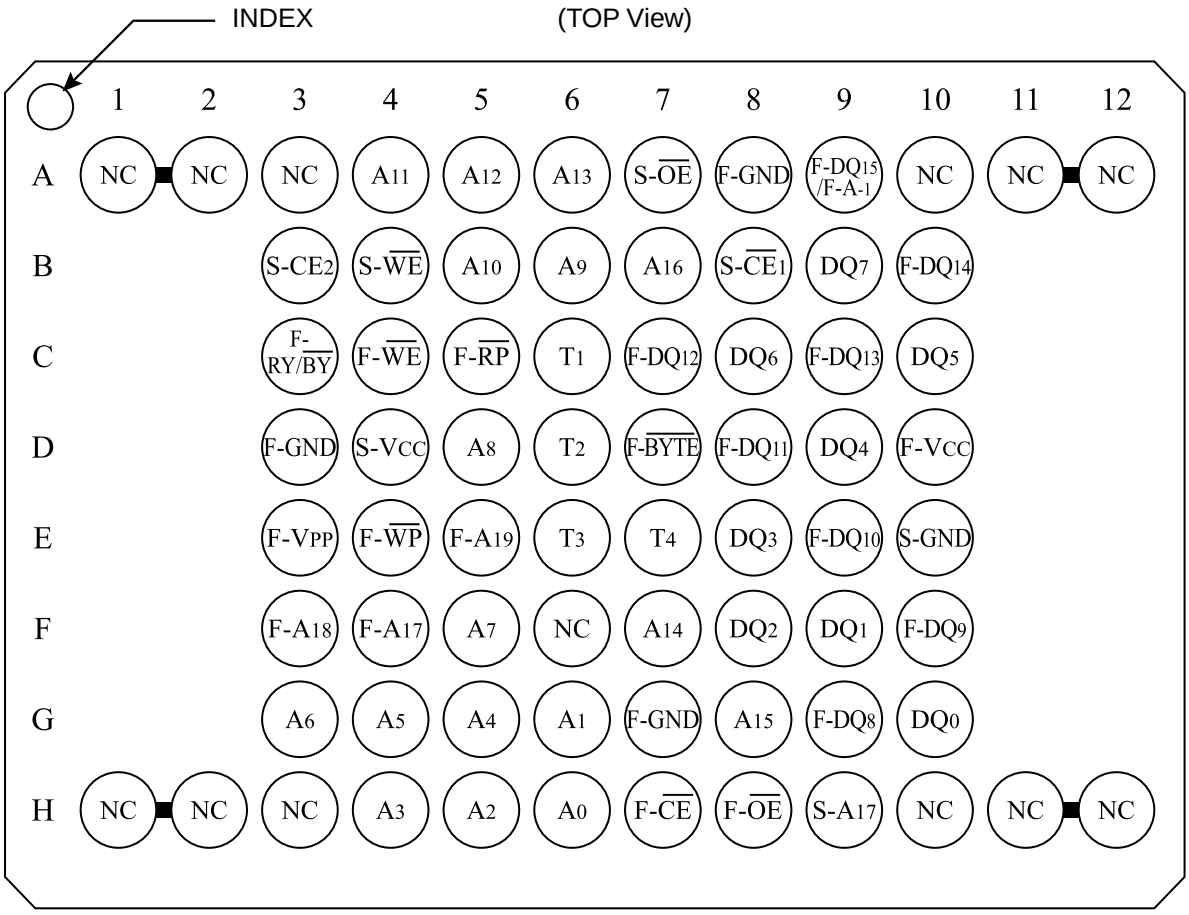
Flash Memory

- Access Time • • • • 100ns (Max.)
- Power Supply current (The current for F-V_{CC} pin and F-V_{PP} pin)
  - Read • • • • 25 mA (Max. t_{CYCLE} = 200ns, CMOS Input)
  - Word/Byte write • • • • 57 mA (Max.)
  - Block erase • • • • 42 mA (Max.)
  - Reset Power-Down • • • • 15µA (Max. F-$\overline{RP}$ = GND ± 0.2V, I_{OUT}(F-RY/$\overline{BY}$) = 0mA)
  - Standby • • • • 65µA (Max. F-$\overline{CE}$ = F-$\overline{RP}$ = F-V_{CC} ± 0.2V)
- Optimized Array Blocking Architecture for each Bank.
  - Two 4k-word/8k-byte Boot Blocks
  - Six 4k-word/8k-byte Parameter Blocks
  - Thirty-one 32k-word/64k-byte Main Blocks
  - Top Boot Location
- Extended Cycling Capability
  - 100,000 Block Erase Cycles
- Enhanced Automated Suspend Options
  - Word/Byte Write Suspend to Read
  - Block Erase Suspend to Word/Byte Write
  - Block Erase Suspend to Read

SRAM

- Access Time • • • • 85 ns (Max.)
- Power Supply current
  - Operating current • • • • 35mA (Max. t_{RC},t_{WC} = Min.)
  - • • • • 6 mA (Max. t_{RC},t_{WC} = 1µs, CMOS Input)
  - Standby current • • • • 30µA (Max.)
  - Data retention current • • • • 30µA (Max.)

2. Pin Configuration



Note) From T_1 to T_4 pins are needed to be open.
Two NC pins at the corner are connected.
Do not float any GND pins.

Pin	Description	Type
A_0 to A_{16}	Address Inputs (Common)	Input
F-A_{-1}, F-A_{17} to F-A_{19}	Address Inputs (Flash) F-A_{-1} : Not used in x16 mode. F-A_{-1} : L.S.B in x8 mode.	Input
S-A_{17}	Address Inputs (SRAM)	Input
F-$\overline{CE}$	Chip Enable Inputs (Flash)	Input
S-$\overline{CE}_1$, S-CE_2	Chip Enable Inputs (SRAM)	Input
F-$\overline{WE}$	Write Enable Input (Flash)	Input
S-$\overline{WE}$	Write Enable Input (SRAM)	Input
F-$\overline{OE}$	Output Enable Input (Flash)	Input
S-$\overline{OE}$	Output Enable Input (SRAM)	Input
F-$\overline{RP}$	Reset Power Down Input (Flash) Block erase and Word/Byte Write : V_{IH} or V_{HH} Read : V_{IH} or V_{HH} Reset Power Down : V_{IL}	Input
F-$\overline{WP}$	Write Protect Input (Flash) Two Boot Blocks Locked : V_{IL} (With F-$\overline{RP}$ = V_{HH} Erase of Write can operate to all block)	Input
F-$\overline{BYTE}$	Byte Enable (Flash); x8 mode : V_{IL}, x16 mode : V_{IH}	Input
F-RY/$\overline{BY}$	Ready/Busy Output (Flash) During an Erase or Write operation : V_{OL} Block Erase and Word/Byte Write Suspend : High-Z (High impedance) Reset Power Down : High-Z (High impedance)	Open Drain Output
DQ_0 to DQ_7	Data Inputs and Outputs (Common)	Input / Output
F-DQ_8 to F-DQ_{15}	Data Inputs and Outputs (Flash) ; Not used in x8 mode.	Input / Output
F-V_{CC}	Power Supply (Flash)	Power
S-V_{CC}	Power Supply (SRAM)	Power
F-V_{PP}	Write, Erase Power Supply (Flash) Block Erase and Word/Byte Write : F-V_{PP} = V_{PPH} All Blocks Locked : F-V_{PP} < V_{PPLK}	Power
F-GND	GND (Flash)	Power
S-GND	GND (SRAM)	Power
NC	Non Connection (Should be all open)	-
T_1 to T_4	Test pin (Should be all open)	-

3. Truth Table(1)

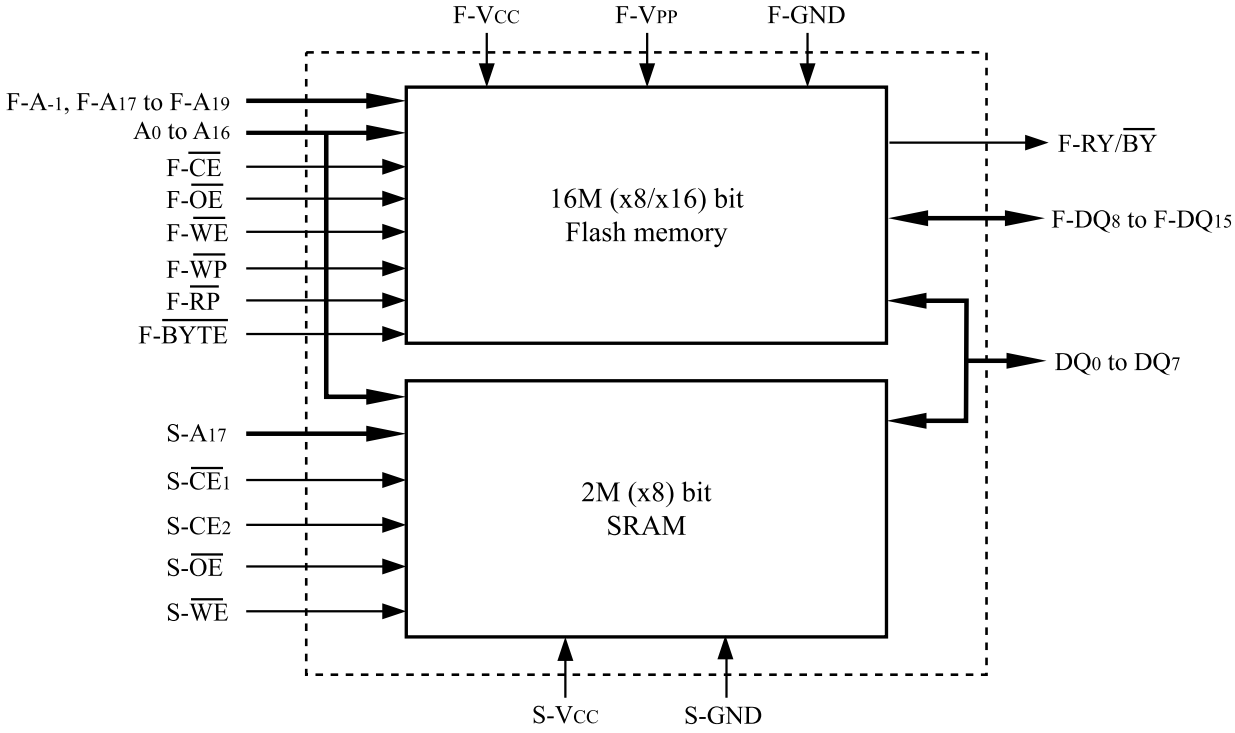
Flash	SRAM	Notes	F-$\overline{CE}$	F-$\overline{RP}$	F-$\overline{OE}$	F-$\overline{WE}$	F-$\overline{BYTE}$	S-$\overline{CE}_1$	S-CE_2	S-$\overline{OE}$	S-$\overline{WE}$	DQ_0 to DQ_7	F-DQ_8 to F-DQ_{15}
Read	Standby	4,5,6	L	H	L	H	H	(7)		X	X	D_{OUT}	
							L					D_{OUT}	High-Z
Output Disable		5,6			H		H					High-Z	
							L						
Write		2,3,4,5,6				L	H					D_{IN}	
							L					D_{IN}	High-Z
Standby	Read	6	H	H	X	X	X	L	H	L	H	D_{OUT}	High-Z
	Output Disable	6								H		High-Z	
	Write	6									L	D_{IN}	
Reset Power Down	Read	6	X	L	X	X	X	L	H	L	H	D_{OUT}	High-Z
	Output Disable	6								H		High-Z	
	Write	6									L	D_{IN}	
Standby	Standby	6	H	H	X	X	X	(7)		X	X	High-Z	
Reset Power Down		6	X	L									

Notes:

1. L = V_{IL}, H = V_{IH}, X = H or L. Refer to DC Characteristics. High-Z = High impedance.
2. Command Writes involving block erase or word/byte write are reliably executed when F-V_{PP} = V_{PPH} and F-V_{CC} = 2.7V to 3.6V.
   Block erase or word/byte write with V_{IH} < F-$\overline{RP}$ < V_{HH} produce spurious results and should not be attempted.
3. Refer Section 5. Command Definitions for valid address input and D_{IN} during a write operation.
4. Never hold F-$\overline{OE}$ low and F-$\overline{WE}$ low at the same timing.
5. F-A_{-1} set to V_{IL} or V_{IH} in byte mode (F-$\overline{BYTE}$ = V_{IL})
6. F-$\overline{WP}$ set to V_{IL} or V_{IH}.
7. SRAM Standby Mode

S-$\overline{CE}_1$	S-CE_2
H	X
X	L

4. Block Diagram



5. Command Definitions for Flash Memory(1)

5.1 Command Definitions

Command	Bus Cycles Required	Note	First Bus Cycle			Second Bus Cycle		
			Oper(2)	Address(3)	Data(3)	Oper(2)	Address(3)	Data(3)
Read Array / Reset	1		Write	XA	FFH			
Read Identifier Codes	≥ 2	4	Write	XA	90H	Read	IA	ID
Read Status Register	2		Write	XA	70H	Read	XA	SRD
Clear Status Register	1		Write	XA	50H			
Block Erase	2	5	Write	BA	20H	Write	BA	D0H
Word/Byte Write	2	5	Write	WA	40H or 10H	Write	WA	WD
Block Erase and Word/Byte Write Suspend	1	5	Write	XA	B0H			
Block Erase and Word/Byte Write Resume	1	5	Write	XA	D0H			

Notes:

1. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.
2. Bus operations are defined in 3. Truth Table.
3. XA = Any valid address within the device.
   IA = Identifier code address.
   BA = Address within the block being erased.
   WA = Address of memory location to be written.
   SRD = Data read from status register (See 6. Status Register Definition).
   WD = Data to be written at location WA. Data is latched on the rising edge of F-$\overline{WE}$ or F-$\overline{CE}$ (whichever goes high first).
   ID = Data read from identifier codes (See 5.2 Identifier Codes).
4. See Identifier Codes in section 5.2.
5. See Write Protection Alternatives in section 5.3.

5.2 Identifier Codes(1)

Codes	Address [A_{19} - A_0]	Data [DQ_7 - DQ_0]
Manufacture Code	00000H	B0H
Device Code	00001H	48H

Notes:

1. Read Identifier Codes command is defined in 5.1 Command Definitions.

5.3 Write Protection Alternatives

Operation	F-V_{PP}	F-$\overline{RP}$	F-$\overline{WP}$	Effect
Block Erase or Word/Byte Write	V_{IL}	X	X	All Blocks Locked.
	>V_{PPLK}(1)	V_{IL}	X	All Blocks Locked.
		V_{HH}	X	All Blocks Unlocked.
		V_{IH}	V_{IL}	2 Boot Blocks Locked.
			V_{IH}	All Blocks Unlocked.

Note:

1. F-V_{PP} is guaranteed only with the nominal voltages.

6. Status Register Definition

WSMS	ESS	ES	WBWS	VPPS	WBWSS	DPS	R
7	6	5	4	3	2	1	0

SR.7 = WRITE STATE MACHINE STATUS (WSMS) 1 = Ready 0 = Busy	Notes: Check SR.7 or F-RY/$\overline{BY}$ to determine Block Erase or Word/Byte Write completion.
SR.6 = ERASE SUSPEND STATUS (ESS) 1 = Block Erase Suspended 0 = Block Erase in Progress/Completed	SR.6 - SR.0 are invalid while SR.7 = “0”. If both SR.5 and SR.4 are “1”s after a Block Erase attempt, an improper command sequence was entered.
SR.5 = ERASE STATUS (ES) 1 = Error in Block Erase 0 = Successful Block Erase	
SR.4 = WORD/BYTE WRITE STATUS (WBWS) 1 = Error in Word/Byte Write 0 = Successful Word/Byte Write	
SR.3 = F-V_{PP} STATUS (VPPS) 1 = F-V_{PP} Low Detect, Operation Abort 0 = F-V_{PP} OK	SR.3 does not provide a continuous indication of F-V_{PP} level. The WSM (Write State Machine) interrogates and indicates the F-V_{PP} level only after Block Erase or Word/Byte Write command sequences. SR.3 is not guaranteed to reports accurate feedback only when F-$V_{PP} \neq V_{PPH}$.
SR.2 = WORD/BYTE WRITE SUSPEND STATUS (WBWSS) 1 = Word/Byte Write Suspended 0 = Word/Byte Write in Progress/Completed	SR.1 does not provide a continuous indication of F-$\overline{WP}$ and F-$\overline{RP}$ values. The WSM interrogates the F-$\overline{WP}$ and F-$\overline{RP}$ only after Block Erase or Word/Byte Write command sequences. It informs the system, depending on the attempted operation, if the F-$\overline{WP}$ is not V_{IH}, F-$\overline{RP}$ is not V_{HH}.
SR.1 = DEVICE PROTECT STATUS (DPS) 1 = F-$\overline{WP}$ or F-$\overline{RP}$ Lock Detected, Operation Abort 0 = Unlocked	
SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)	SR.0 is reserved for future use and should be masked out when polling the status register.

7. Memory Map for Flash Memory

Top Boot

[A19 ~ A0]		[A19 ~ A-1]
FFFFF	4K-word/8K-byte Boot Block 0	1FFFFF
FF000 FEFFF	4K-word/8K-byte Boot Block 1	1FE000 1FDFFF
FE000 FDFFF	4K-word/8K-byte Parameter Block 0	1FC000 1FBFFF
FD000 FCFFF	4K-word/8K-byte Parameter Block 1	1FA000 1F9FFF
FC000 FBFFF	4K-word/8K-byte Parameter Block 2	1F8000 1F7FFF
FB000 FAFFF	4K-word/8K-byte Parameter Block 3	1F6000 1F5FFF
FA000 F9FFF	4K-word/8K-byte Parameter Block 4	1F4000 1F3FFF
F9000 F8FFF	4K-word/8K-byte Parameter Block 5	1F2000 1F1FFF
F8000 F7FFF	32K-word/64K-byte Main Block 0	1F0000 1EFFFF
F0000 EFFFF	32K-word/64K-byte Main Block 1	1E0000 1DFFFF
E8000 E7FFF	32K-word/64K-byte Main Block 2	1D0000 1CFFFF
E0000 DFFFF	32K-word/64K-byte Main Block 3	1C0000 1BFFFF
D8000 D7FFF	32K-word/64K-byte Main Block 4	1B0000 1AFFFF
D0000 CFFFF	32K-word/64K-byte Main Block 5	1A0000 19FFFF
C8000 C7FFF	32K-word/64K-byte Main Block 6	190000 18FFFF
C0000 BFFFF	32K-word/64K-byte Main Block 7	180000 17FFFF
B8000 B7FFF	32K-word/64K-byte Main Block 8	170000 16FFFF
B0000 AFFFF	32K-word/64K-byte Main Block 9	160000 15FFFF
A8000 A7FFF	32K-word/64K-byte Main Block 10	150000 14FFFF
A0000 9FFFF	32K-word/64K-byte Main Block 11	140000 13FFFF
98000 97FFF	32K-word/64K-byte Main Block 12	130000 12FFFF
90000 8FFFF	32K-word/64K-byte Main Block 13	120000 11FFFF
88000 87FFF	32K-word/64K-byte Main Block 14	110000 10FFFF
80000 7FFFF	32K-word/64K-byte Main Block 15	100000 0FFFFF
78000 77FFF	32K-word/64K-byte Main Block 16	0F0000 0EFFFF
70000 6FFFF	32K-word/64K-byte Main Block 17	0E0000 0DFFFF
68000 67FFF	32K-word/64K-byte Main Block 18	0D0000 0CFFFF
60000 5FFFF	32K-word/64K-byte Main Block 19	0C0000 0BFFFF
58000 57FFF	32K-word/64K-byte Main Block 20	0B0000 0AFFFF
50000 4FFFF	32K-word/64K-byte Main Block 21	0A0000 09FFFF
48000 47FFF	32K-word/64K-byte Main Block 22	090000 08FFFF
40000 3FFFF	32K-word/64K-byte Main Block 23	080000 07FFFF
38000 37FFF	32K-word/64K-byte Main Block 24	070000 06FFFF
30000 2FFFF	32K-word/64K-byte Main Block 25	060000 05FFFF
28000 27FFF	32K-word/64K-byte Main Block 26	050000 04FFFF
20000 1FFFF	32K-word/64K-byte Main Block 27	040000 03FFFF
18000 1FFFF	32K-word/64K-byte Main Block 28	030000 02FFFF
10000 0FFFF	32K-word/64K-byte Main Block 29	020000 01FFFF
08000 07FFF	32K-word/64K-byte Main Block 30	010000 00FFFF
00000		000000

8. Absolute Maximum Ratings

Symbol	Parameter	Notes	Ratings	Unit
V_{CC}	Supply voltage	1,2	-0.2 to +4.0	V
V_{IN}	Input voltage	1,3,4,6	-0.2 to V_{CC}+0.3	V
T_A	Operating temperature		-25 to +85	°C
T_{STG}	Storage temperature		-55 to +125	°C
F-V_{PP}	F-V_{PP} voltage	1,4,5	-0.2 to +14.0	V
F-$\overline{RP}$	F-$\overline{RP}$ voltage	1,4,5	-0.5 to +14.0	V

Notes:
1. The maximum applicable voltage on any pins with respect to GND.
2. Except F-V_{PP}.
3. Except F-$\overline{RP}$.
4. -1.0V undershoot and V_{CC} + 1.0V overshoot are allowed when the pulse width is less than 20 nsec.
5. +14.0V overshoot is allowed when the pulse width is less than 20 nsec.
6. V_{IN} should not be over V_{CC} + 0.3V.

9. Recommended DC Operating Conditions

(T_A = -25°C to +85°C)

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	2	2.7	3.0	3.6	V
V_{IH}	Input Voltage	1	2.2		V_{CC}+0.2	V
V_{IL}			-0.2		0.8	V
V_{HH}		3	11.4		12.6	V

Notes:
1. V_{CC} is the lower one of F-V_{CC} and S-V_{CC}.
2. V_{CC} includes both F-V_{CC} and S-V_{CC}.
3. This voltage is applicable to F-$\overline{RP}$ Pin only.

10. Pin Capacitance

(T_A = 25°C, f = 1MHz)

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit	Condition
C_{IN}	Input capacitance	1			20	pF	V_{IN} = 0V
$C_{I/O}$	I/O capacitance	1			22	pF	$V_{I/O}$ = 0V

Note:
1. Sampled but not 100% tested.

11. DC Electrical Characteristics(6)

DC Electrical Characteristics

(T_A = -25°C to +85°, V_{CC} = 2.7V to 3.6V)

Symbol	Parameter	Notes	Min.	Typ.(1)	Max.	Unit	Conditions	
I_{LI}	Input Leakage Current				±1.5	µA	$V_{IN} = V_{CC}$ or GND	
I_{LO}	Output Leakage Current				±1.5	µA	$V_{OUT} = V_{CC}$ or GND	
I_{CCS}	F-V_{CC} Standby Current	2,4,9		25	50	µA	CMOS Input F-$\overline{CE}$ = F-$\overline{RP}$ = F-V_{CC} ± 0.2V	
				0.2	2	mA	TTL Input F-$\overline{CE}$ = F-$\overline{RP}$ = V_{IH}	
I_{CCD}	F-V_{CC} Reset Power-Down Current	4,9		5	10	µA	F-$\overline{RP}$ = GND ± 0.2V I_{OUT}(F-RY/$\overline{BY}$) = 0mA	
I_{CCR}	F-V_{CC} Read Current	3,4			25	mA	CMOS Input F-$\overline{CE}$ = GND, f = 5MHz, I_{OUT} = 0mA	
					30	mA	TTL Input F-$\overline{CE}$ = V_{IL}, f = 5MHz, I_{OUT} = 0mA	
I_{CCW}	F-V_{CC} Word/Byte Write Current	7			17	mA	F-V_{PP} = V_{PPH}	
I_{CCE}	F-V_{CC} Block Erase Current	7			17	mA	F-V_{PP} = V_{PPH}	
I_{CCWS} I_{CCES}	F-V_{CC} Word/Byte Write or Block Erase Suspend Current				6	mA	F-$\overline{CE}$ = V_{IH}	
I_{PPS} I_{PPR}	F-V_{PP} Standby or Read Current	4		±2	±15	µA	F-V_{PP} ≤ F-V_{CC}	
				10	200	µA	F-V_{PP} > F-V_{CC}	
I_{PPD}	F-V_{PP} Reset Power-Down Current	4		0.1	5	µA	CMOS Input F-$\overline{RP}$ = GND ± 0.2V	
I_{PPW}	F-V_{PP} Word/Byte Write Current	7		12	40	mA	F-V_{PP} = V_{PPH}	
I_{PPE}	F-V_{PP} Block Erase Current	7		8	25	mA	F-V_{PP} = V_{PPH}	
I_{PPWS} I_{PPES}	F-V_{PP} Word/Byte Write or Block Erase Suspend Current			10	200	µA	F-V_{PP} = V_{PPH}	
I_{SB}	S-V_{CC} Standby Current				30	µA	S-$\overline{CE}_1$, S-CE_2 ≥ S-V_{CC} - 0.2V or S-CE_2 ≤ 0.2V	
I_{SB1}	S-V_{CC} Standby Current				3	mA	S-$\overline{CE}_1$ = V_{IH} or S-CE_2 = V_{IL}	
I_{CC1}	S-V_{CC} Operation Current				35	mA	S-$\overline{CE}_1$ = V_{IL}, S-CE_2 = V_{IH} V_{IN} = V_{IL} or V_{IH}	t_{CYCLE} =Min. $I_{I/O}$ = 0mA
I_{CC2}	S-V_{CC} Operation Current				6	mA	S-$\overline{CE}_1$ = 0.2V, S-CE_2 = SV_{CC} -0.2V, V_{IN} = S-V_{CC} -0.2V or 0.2V	t_{CYCLE} = 1µs $I_{I/O}$ = 0mA

DC Electrical Characteristics (Continue)

(T_A = -25°C to +85°C, V_{CC} = 2.7V to 3.6V)

Symbol	Parameter	Notes	Min.	Typ.(1)	Max.	Unit	Conditions
V_{IL}	Input Low Voltage	7	-0.2		0.8	V	
V_{IH}	Input High Voltage	7	2.2		V_{CC} +0.2	V	
V_{OL}	Output Low Voltage	2,7			0.4	V	I_{OL} = 2.0mA
V_{OH}	Output High Voltage	2,7	2.4			V	I_{OH} = -1.0mA
V_{PPLK}	F-V_{PP} Lockout during Normal Operations	5,7			1.5	V	
V_{PPH}	F-V_{PP} Word/Byte Write Block Erase Operations		2.7		3.6	V	
V_{LKO}	F-V_{CC} Lockout Voltage		1.5			V	
V_{HH}	F-$\overline{RP}$ Unlock Voltage	8	11.4		12.6	V	Unavailable F-$\overline{WP}$

Notes:

1. All currents are in RMS unless otherwise noted. Reference values at V_{CC} = 3.0V and T_A = +25°C.
2. Includes F-RY/$\overline{BY}$.
3. Automatic Power Savings (APS) for Flash Memory reduces typical I_{CCR} to 3mA at 2.7V in static operation.
4. CMOS inputs are either V_{CC} ± 0.2V or GND ± 0.2V. TTL inputs are either V_{IL} or V_{IH}.
5. Block erases and word/byte writes are inhibited when F-V_{PP} ≤ V_{PPLK} and not guaranteed in the range between V_{PPLK} (Max.) and V_{PPH} (Min.), and above V_{PPH} (Max.).
6. V_{CC} includes both F-V_{CC} and S-V_{CC}.
7. Sampled, not 100% tested.
8. F-$\overline{RP}$ connection to a V_{HH} supply is allowed for a maximum cumulative period of 80 hours.
9. F-$\overline{BYTE}$ is V_{CC} ± 0.2V in word mode and is GND ± 0.2V in byte mode.
   F-$\overline{WP}$ is V_{CC}± 0.2V or GND ± 0.2V

12. AC Electrical Characteristics for Flash Memory

12.1 AC Test Conditions

Input pulse level	0V to 2.7V
Input rise and fall time	5ns
Input and Output timing Ref. level	1.35V
Output load	1TTL + C_L (30pF)

12.2 Read Cycle

(T_A = -25°C to +85°C, F-V_{CC} = 2.7V to 3.6V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{AVAV}	Read Cycle Time		100		ns
t_{AVQV}	Address to Output Delay			100	ns
t_{ELQV}	F-$\overline{CE}$ to Output Delay	1		100	ns
t_{PHQV}	F-$\overline{RP}$ High to Output Delay			10	µs
t_{GLQV}	F-$\overline{OE}$ to Output Delay	1		45	ns
t_{ELQX}	F-$\overline{CE}$ to Output in Low-Z		0		ns
t_{EHQZ}	F-$\overline{CE}$ High to Output in High-Z			45	ns
t_{GLQX}	F-$\overline{OE}$ to Output in Low-Z		0		ns
t_{GHQZ}	F-$\overline{OE}$ High to Output in High-Z			20	ns
t_{OH}	Output Hold form Address, F-$\overline{CE}$ or F-$\overline{OE}$ Change, Whichever Occurs First		0		ns
t_{FVQV}	F-$\overline{BYTE}$ and A_{-1} to Output Delay			100	ns
t_{FLQZ}	F-$\overline{BYTE}$ Low to Output in High-Z			30	ns
t_{ELFV}	F-$\overline{CE}$ to F-$\overline{BYTE}$ High or Low			5	ns

Note:
1. F-$\overline{OE}$ may be delayed up to t_{ELQV} - t_{GLQV} after the falling edge of F-$\overline{CE}$ without impact on t_{ELQV}.

12.3 Write Cycle (F-$\overline{WE}$ Controlled)[1,5]

(T_A = -25°C to +85°C, F-V_{CC} = 2.7V to 3.6V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{AVAV}	Write Cycle Time		100		ns
t_{PHWL}	F-$\overline{RP}$ High Recovery to F-$\overline{WE}$ Going to Low	2	10		µs
t_{ELWL}	F-$\overline{CE}$ Setup to F-$\overline{WE}$ Going Low		0		ns
t_{WLWH}	F-$\overline{WE}$ Pulse Width		50		ns
t_{PHHWH}	F-$\overline{RP}$ V_{HH} Setup to F-$\overline{WE}$ Going High	2	100		ns
t_{SHWH}	F-$\overline{WP}$ V_{IH} Setup to F-$\overline{WE}$ Going High	2	100		ns
t_{VPWH}	F-V_{PP} Setup to F-$\overline{WE}$ Going High	2	100		ns
t_{AVWH}	Address Setup to F-$\overline{WE}$ Going High	3	50		ns
t_{DVWH}	Data Setup to F-$\overline{WE}$ Going High	3	50		ns
t_{WHDX}	Data Hold from F-$\overline{WE}$ High		0		ns
t_{WHAX}	Address Hold from F-$\overline{WE}$ High		0		ns
t_{WHEH}	F-$\overline{CE}$ Hold from F-$\overline{WE}$ High		0		ns
t_{WHWL}	F-$\overline{WE}$ Pulse Width High		30		ns
t_{WHRL}	F-$\overline{WE}$ High to F-RY/$\overline{BY}$ Going Low			100	ns
t_{WHGL}	Write Recovery before Read		0		ns
t_{QVVL}	F-V_{PP} Hold from Valid SRD, F-RY/$\overline{BY}$ High-Z	2,4	0		ns
t_{QVPH}	F-$\overline{RP}$ V_{HH} Hold from Valid SRD, F-RY/$\overline{BY}$ High-Z	2,4	0		ns
t_{QVSL}	F-$\overline{WP}$ V_{IH} Hold from Valid SRD, F-RY/$\overline{BY}$ High-Z	2,4	0		ns
t_{FVWH}	F-$\overline{BYTE}$ Setup to F-$\overline{WE}$ Going High		50		ns
t_{WHFV}	F-$\overline{BYTE}$ Hold from F-$\overline{WE}$ High		100		ns

Notes:

1. Read timing characteristics during block erase and word/byte write operations. Refer to AC Characteristics for read cycle.
2. Sampled, not 100% tested.
3. Refer to Section 5. Command Definitions for Flash Memory for valid A_{IN} and D_{IN} for block erase or word/byte write.
4. F-V_{PP} should be held at V_{PPH} until determination of block erase or word/byte write success (SR.1/3/4/5 = 0).
5. It is written when F-$\overline{CE}$ and F-$\overline{WE}$ are active. The address and data needed to execute a command are latched on the rising edge of F-$\overline{WE}$ or F-$\overline{CE}$ (Whichever goes high first).

12.4 Write Cycle (F-$\overline{CE}$ Controlled)[1,2,6]

(T_A = -25°C to +85°C, F-V_{CC} = 2.7V to 3.6V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{AVAV}	Write Cycle Time		100		ns
t_{PHEL}	F-$\overline{RP}$ High Recovery to F-$\overline{CE}$ Going Low	3	10		µs
t_{WLEL}	F-$\overline{WE}$ Setup to F-$\overline{CE}$ Going Low		0		ns
t_{ELEH}	F-$\overline{CE}$ Pulse Width		70		ns
t_{PHHEH}	F-$\overline{RP}$ V_{HH} Setup to F-$\overline{CE}$ Going High	3	100		ns
t_{SHEH}	F-$\overline{WP}$ V_{IH} Setup to F-$\overline{CE}$ Going High	3	100		ns
t_{VPEH}	F-V_{PP} Setup to F-$\overline{CE}$ Going High	3	100		ns
t_{AVEH}	Address Setup to F-$\overline{CE}$ Going High	4	50		ns
t_{DVEH}	Data Setup to F-$\overline{CE}$ Going High	4	50		ns
t_{EHDX}	Data Hold from F-$\overline{CE}$ High		0		ns
t_{EHAX}	Address Hold from F-$\overline{CE}$ High		0		ns
t_{EHWH}	F-$\overline{WE}$ Hold from F-$\overline{CE}$ High		0		ns
t_{EHEL}	F-$\overline{CE}$ Pulse Width High		25		ns
t_{EHRL}	F-$\overline{CE}$ High to F-RY/$\overline{BY}$ Going Low			100	ns
t_{EHGL}	Write Recovery before Read		0		ns
t_{QVVL}	F-V_{PP} Hold from Valid SRD, F-RY/$\overline{BY}$ High-Z	3,5	0		ns
t_{QVPH}	F-$\overline{RP}$ V_{HH} Hold from Valid SRD, F-RY/$\overline{BY}$ High-Z	3,5	0		ns
t_{QVSL}	F-$\overline{WP}$ V_{IH} Hold from Valid SRD, F-RY/$\overline{BY}$ High-Z	3,5	0		ns
t_{FVEH}	F-$\overline{BYTE}$ Setup to F-$\overline{WE}$ Going High		50		ns
t_{EHFV}	F-$\overline{BYTE}$ Hold from F-$\overline{WE}$ High		100		ns

Notes:

1. Read timing characteristics during block erase and word/byte write operations. Refer to AC Characteristics for read cycle.
2. In systems where F-$\overline{CE}$ defines the write pulse width (within a longer F-$\overline{WE}$ timing waveform), all setup, hold and inactive F-$\overline{WE}$ times should be measured relative to the F-$\overline{CE}$ waveform.
3. Sampled, not 100% tested.
4. Refer to Section 5. Command Definitions for Flash Memory for valid A_{IN} and D_{IN} for block erase or word/byte write.
5. F-V_{PP} should be held at V_{PPH} until determination of block erase or word/byte write success (SR.1/3/4/5 = 0).
6. It is written when F-$\overline{CE}$ and F-$\overline{WE}$ are active. The address and data needed to execute a command are latched on the rising edge of F-$\overline{WE}$ or F-$\overline{CE}$ (Whichever goes high first).

12.5 Block Erase and Word/Byte Write Performance[3]

(T_A = -25°C to +85°C, F-V_{CC} = 2.7V to 3.6V)

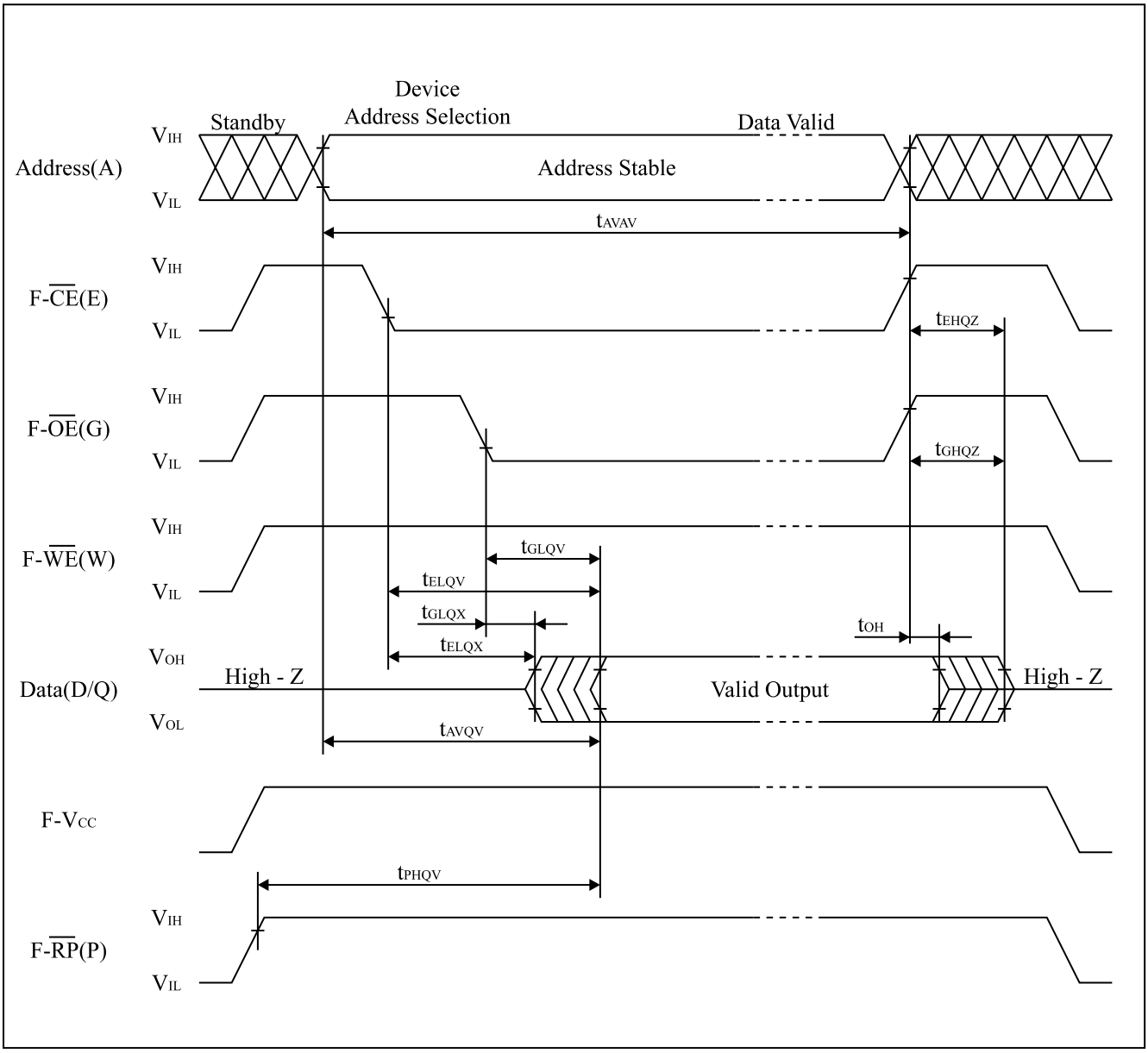
Symbol	Parameter		Notes	F-V_{PP} = 2.7V to 3.6V		Unit
				Typ.[1]	Max.	
t_{WHQV1} t_{EHQV1}	Word/Byte Write Time	32K/64K-Word/Byte Block	2	55		µs
		4K/8K-Word/Byte Block	2	60		µs
	Block Write Time (at word mode)	32K-Word Block	2	1.8		s
		4K-Word Block	2	0.3		s
	Block Write Time (at byte mode)	64K-Byte Block	2	3.6		s
		8K-Byte Block	2	0.6		s
t_{WHQV2} t_{EHQV2}	Block Erase Time	32K/64K-Word/Byte Block	2	1.2		s
		4K/8K-Word/Byte Block	2	0.5		s
t_{WHRZ1} t_{EHRZ1}	Word/Byte Write Suspend Latency Time to Read		4	7.5	8.6	µs
t_{WHRZ2} t_{EHRZ2}	Erase Suspend Latency Time to Read		4	19.3	23.6	µs

Notes:

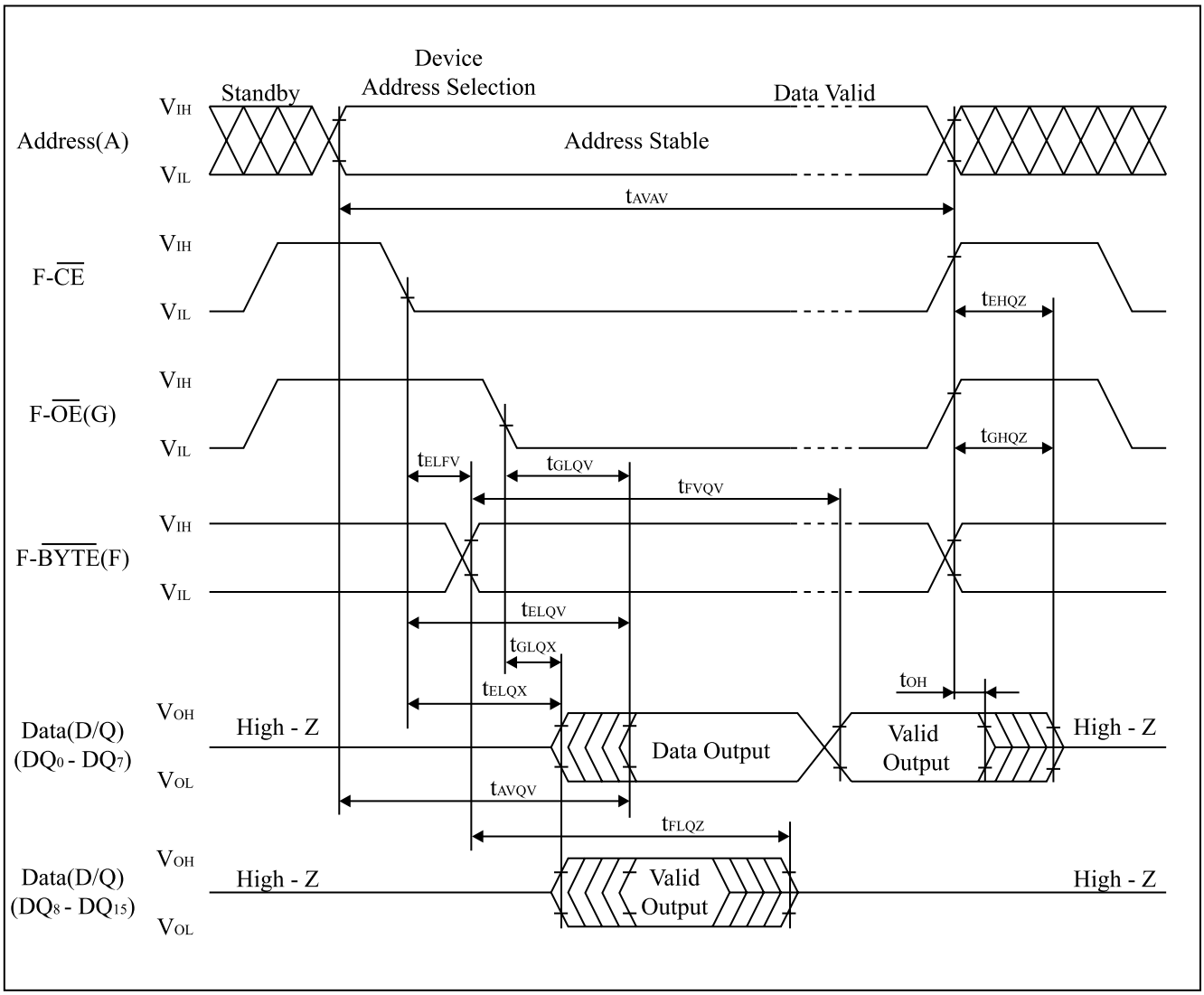
1. Reference values at T_A = +25°C and F-V_{CC} = 3.0V, F-V_{PP} = 3.0V. Assumes corresponding lock-bits are not set. Subject to change based on device characterization.
2. Excludes system-level overhead.
3. Sampled, not 100% tested.
4. A Latency time is required from issuing suspend command (F-$\overline{WE}$ or F-$\overline{CE}$ going high) until F-RY/$\overline{BY}$ going High-Z or SR.7 going “1”.

12.6 Flash Memory AC Characteristics Timing Chart

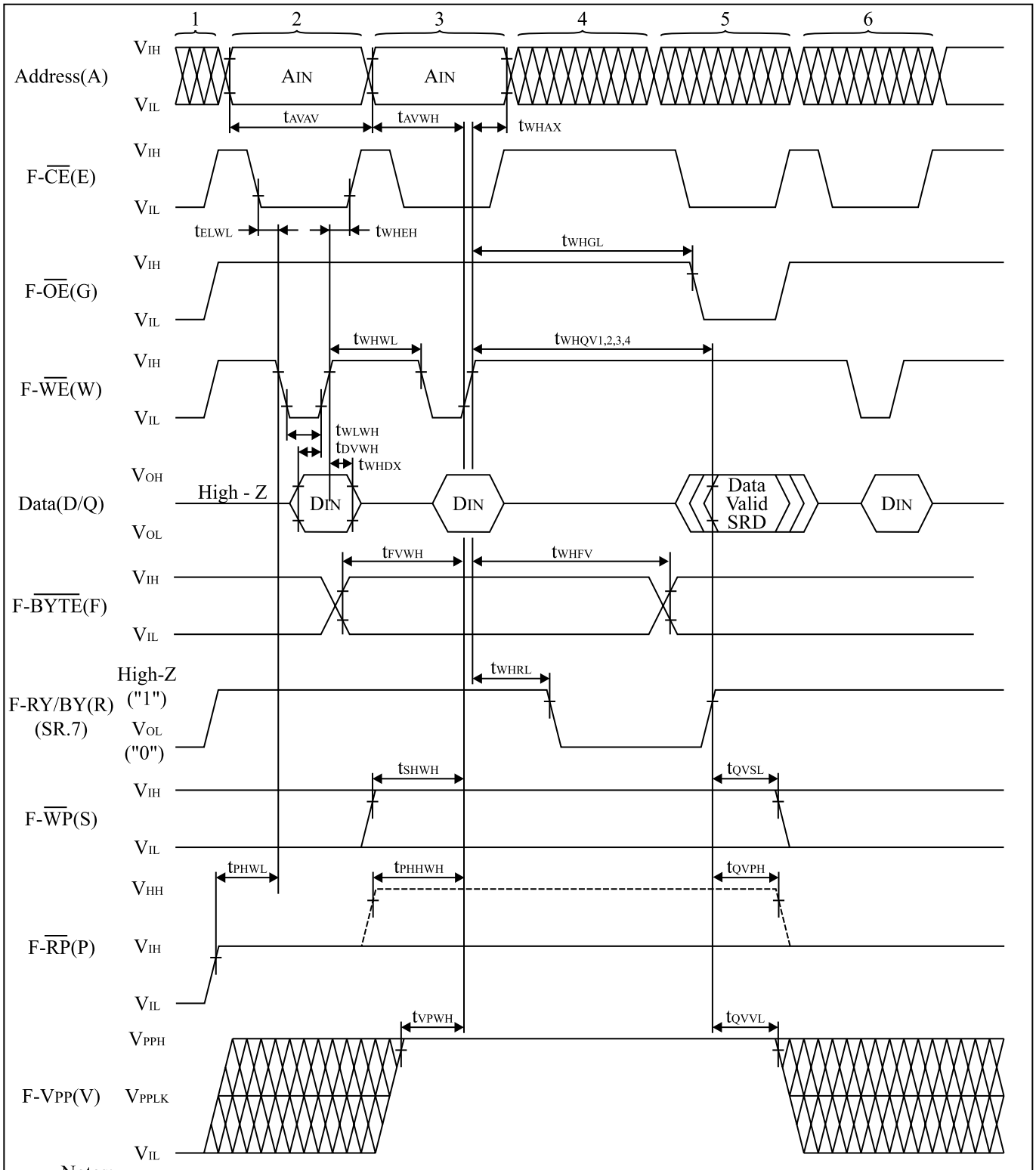
Read Cycle Timing Chart



F-$\overline{\text{BYTE}}$ Timing Waveform

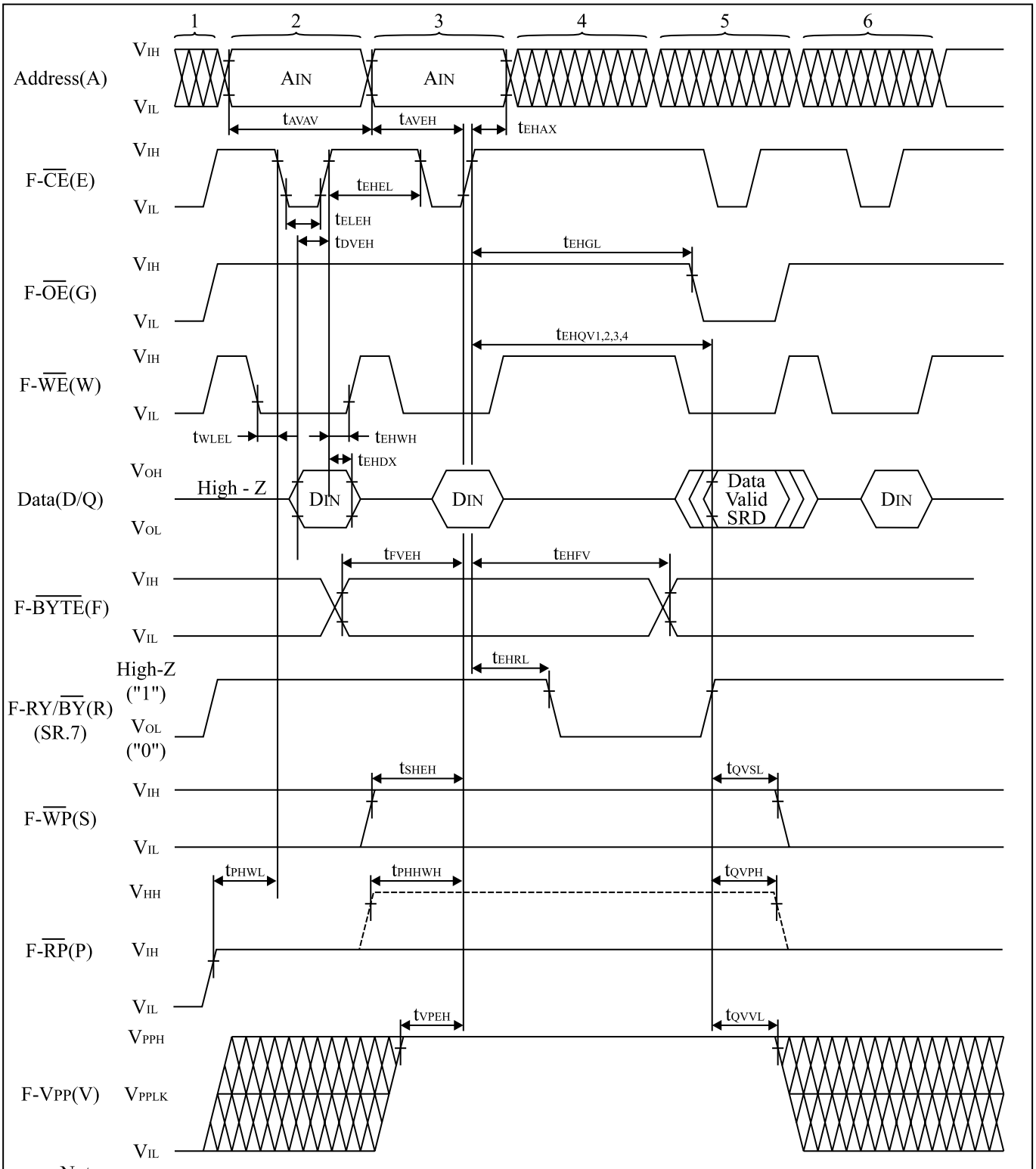


Write Cycle Timing Chart (F-$\overline{WE}$ Controlled)



Notes:
1. F-V_{CC} power-up and standby.
2. Write each setup command.
3. Write each comfirm command or valid address and data.
4. Automated erase or program delay
5. Read status register data.
6. Write Read Array command.

Write Cycle Timing Chart (F-$\overline{CE}$ Controlled)



Notes:
1. F-V_{CC} power-up and standby.
2. Write each setup command.
3. Write each comfirm command or valid address and data.
4. Automated erase or program delay
5. Read status register data.
6. Write Read Array command.

12.7 Reset Operations[1,2]

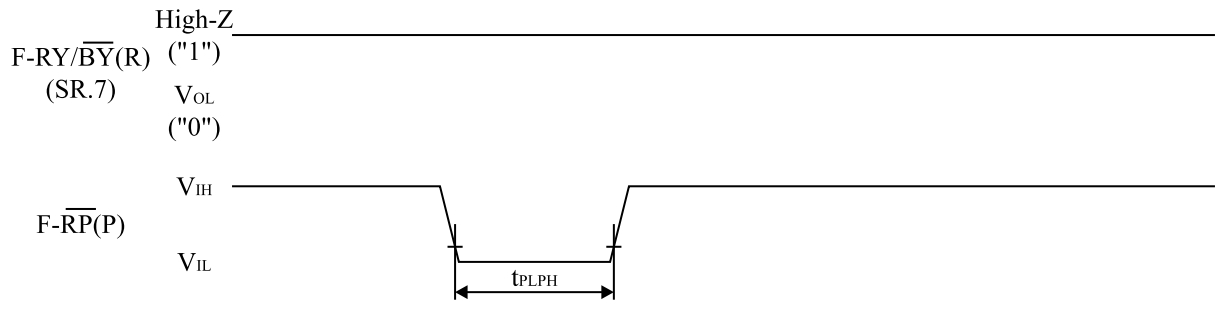
(T_A = -25°C to +85°C, F-V_{CC} = 2.7V to 3.6V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{PLPH}	F-$\overline{RP}$ Pulse Low Time (If F-$\overline{RP}$ is tied to F-V_{CC}, this specification is not applicable.)		100		ns
t_{PLRZ}	F-$\overline{RP}$ Low to Reset during Block Erase or Word/Byte Write			23.6	µs
t_{VPH}	F-V_{CC} = 2.7V to F-$\overline{RP}$ High	3	100		ns

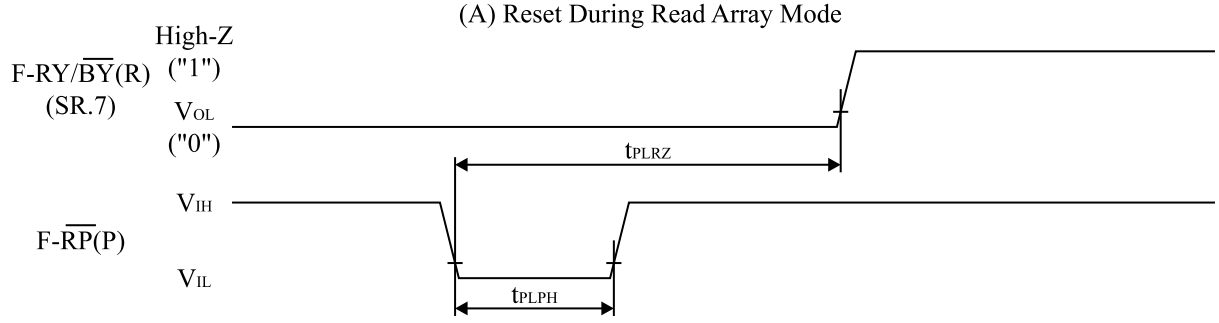
Notes:

1. If F-$\overline{RP}$ is asserted while a block erase or word/byte write operation is not executing, the reset will complete within 100ns.
2. A reset time, t_{PHQV}, is required from the later of F-RY/$\overline{BY}$(SR.7) going High-Z (“1”) or F-$\overline{RP}$ going high until outputs are valid. Refer to AC Characteristics-Read Cycle for t_{PHQV}.
3. When the device power-up, holding F-$\overline{RP}$ low minimum 100ns is required after F-V_{CC} has been in predefined range and also has been in stable there.

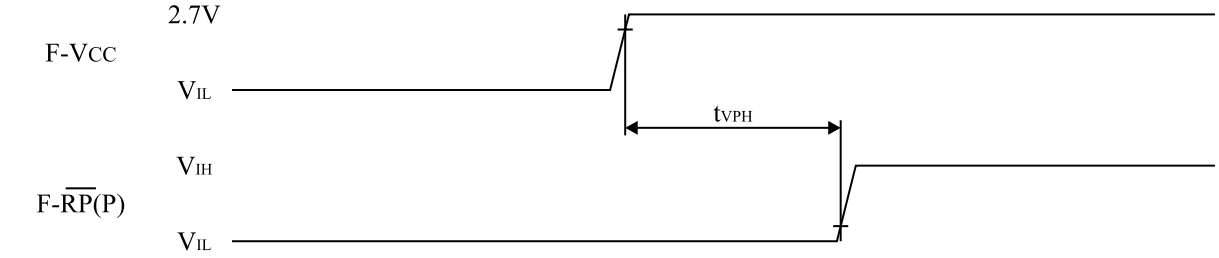
AC Waveform for Reset Operation



(A) Reset During Read Array Mode



(B) Reset During Block Erase or Word/Byte Write



(C) F-$\overline{RP}$ Rising Timing

13. AC Electrical Characteristics for SRAM

13.1 AC Test Conditions

Input pulse level	0.4V to 2.2V
Input rise and fall time	5ns
Input and Output timing Ref. level	1.5V
Output load	1TTL + C_L (30pF)(1)

Note:
1. Including scope and socket capacitance.

13.2 Read Cycle

(T_A = -25°C to +85°C, S-V_{CC} = 2.7V to 3.6V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{RC}	Read Cycle Time		85		ns
t_{AA}	Address access time			85	ns
t_{ACE1}	Chip enable access time (S-$\overline{CE}_1$)			85	ns
t_{ACE2}	Chip enable access time (S-CE_2)			85	ns
t_{OE}	Output enable to output valid			45	ns
t_{OH}	Output hold from address change		10		ns
t_{LZ1}	S-$\overline{CE}_1$ Low to output active	1	10		ns
t_{LZ2}	S-CE_2 Low to output active	1	10		ns
t_{OLZ}	S-$\overline{OE}$ Low to output active	1	5		ns
t_{HZ1}	S-$\overline{CE}_1$ High to output in High-Z	1	0	25	ns
t_{HZ2}	S-CE_2 High to output in High-Z	1	0	25	ns
t_{OHZ}	S-$\overline{OE}$ High to output in High-Z	1	0	25	ns

Note:
1. Active output to High-Z and High-Z to output active tests specified for a ±200mV transition from steady state levels into the test load.

13.3 Write Cycle

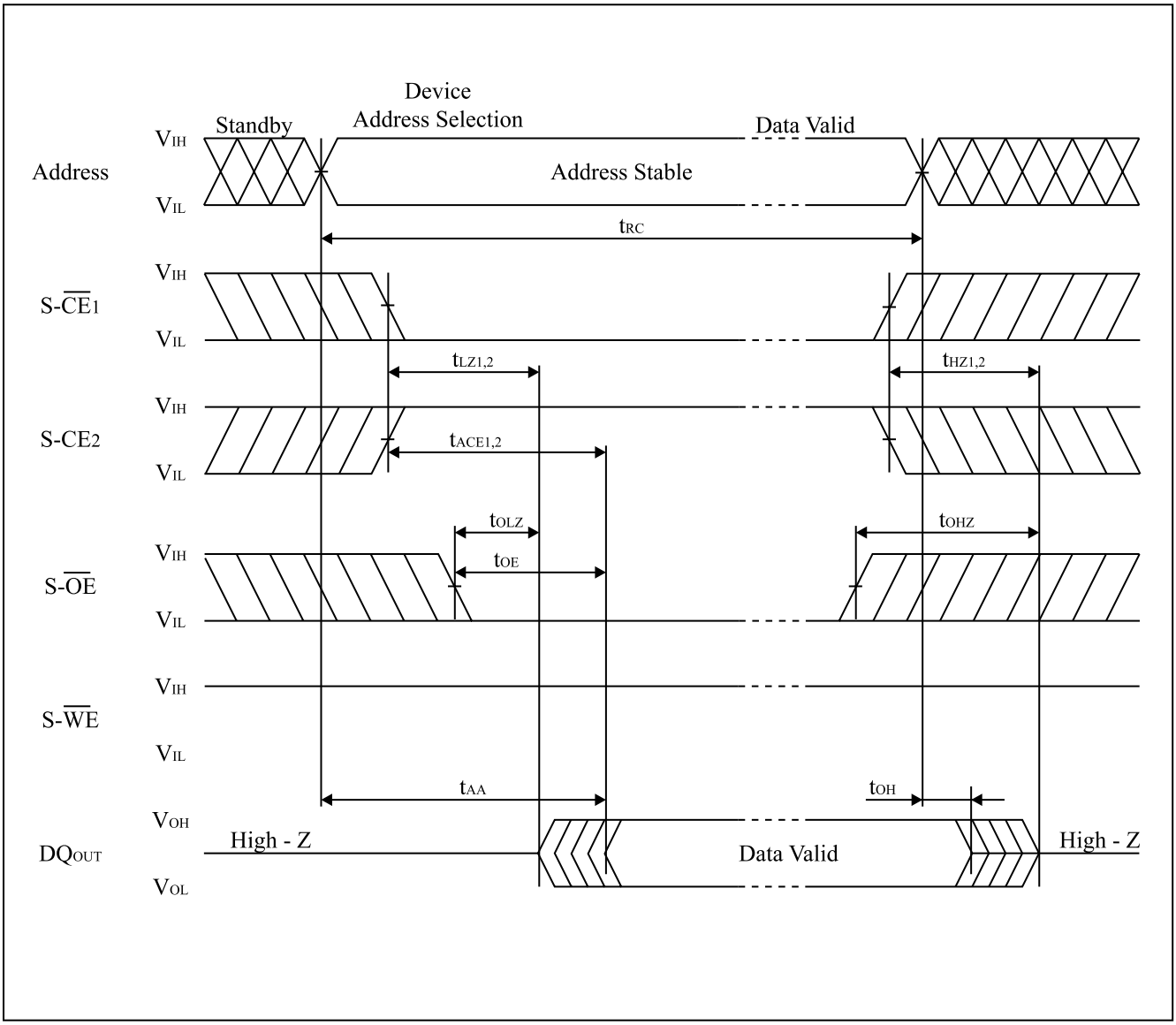
(T_A = -25°C to +85°C, S-V_{CC} = 2.7V to 3.6V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{WC}	Write cycle time		85		ns
t_{CW}	Chip enable to end of write		70		ns
t_{AW}	Address valid to end of write		70		ns
t_{AS}	Address setup time		0		ns
t_{WP}	Write pulse width		60		ns
t_{WR}	Write recovery time		0		ns
t_{DW}	Input data setup time		35		ns
t_{DH}	Input data hold time		0		ns
t_{OW}	S-$\overline{WE}$ High to output active	1	5		ns
t_{WZ}	S-$\overline{WE}$ Low to output in High-Z	1	0	25	ns

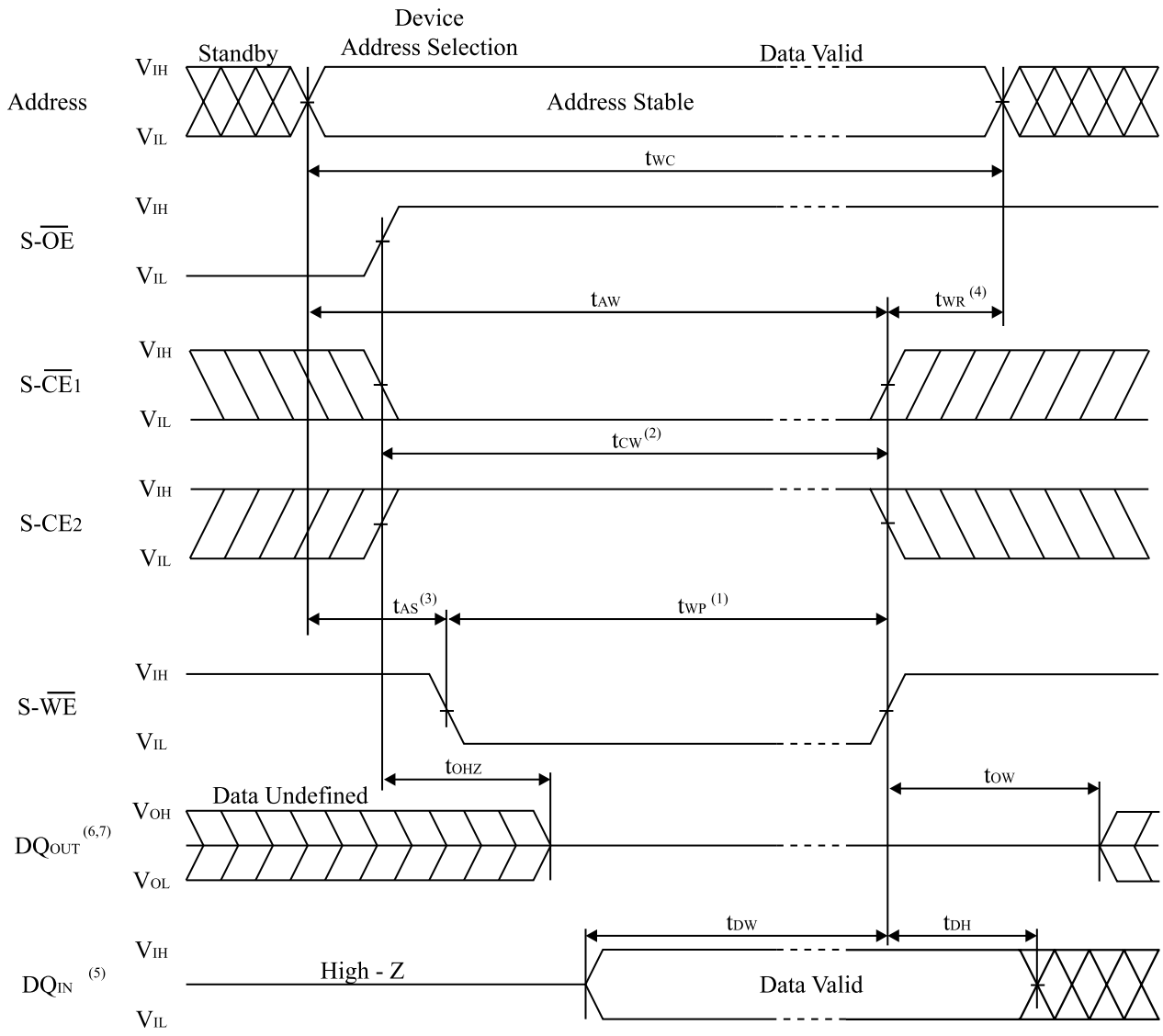
Note:
1. Active output to High-Z and High-Z to output active tests specified for a ±200mV transition from steady state levels into the test load.

13.4 SRAM AC Characteristics Timing Chart

Read cycle timing chart



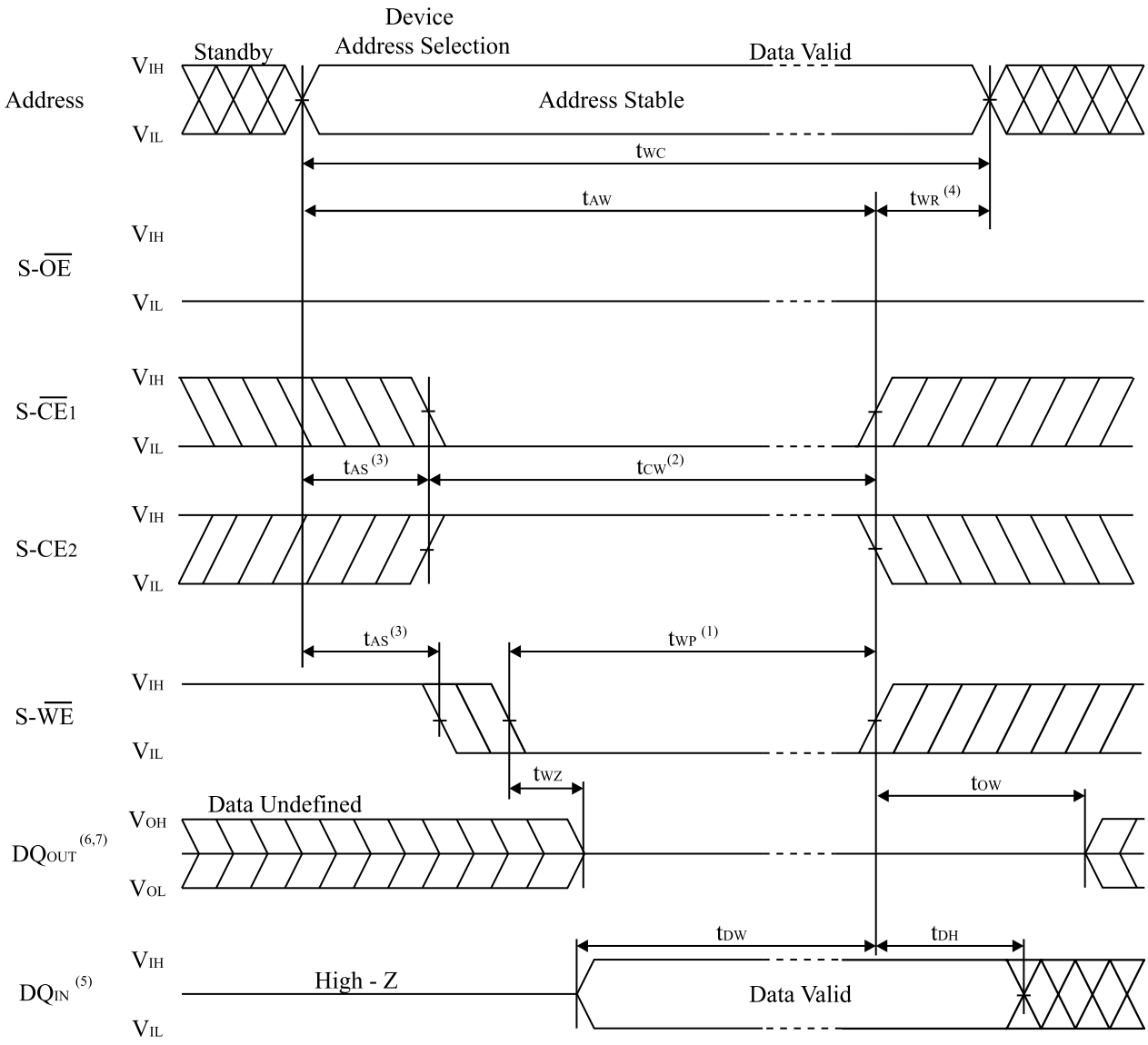
Write cycle timing chart (S-$\overline{OE}$ Controlled)



Notes:

1. A write occurs during the overlap of a low S-$\overline{CE}_1$, a high S-CE_2 and a low S-$\overline{WE}$.
   A write begins at the latest transition among S-$\overline{CE}_1$ going low, S-CE_2 going high and S-$\overline{WE}$ going low.
   A write ends at the earliest transition among S-$\overline{CE}_1$ going high, S-CE_2 going low and S-$\overline{WE}$ going high.
   t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of S-$\overline{CE}_1$ going low or S-CE_2 going high to the end of write.
3. t_{AS} is measured from the address valid to beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applies in case a write ends at S-$\overline{CE}_1$ going high, S-CE_2 going low or S-$\overline{WE}$ going high.
5. During this period DQ pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
6. If S-$\overline{CE}_1$ goes low or S-CE_2 goes high simultaneously with S-$\overline{WE}$ going low or after S-$\overline{WE}$ going low, the outputs remain in high impedance state.
7. If S-$\overline{CE}_1$ goes high or S-CE_2 goes low simultaneously with S-$\overline{WE}$ going high or before S-$\overline{WE}$ going high, the outputs remain in high impedance state.

Write cycle timing chart (S-$\overline{OE}$ Low fixed)



Notes:

1. A write occurs during the overlap of a low S-$\overline{CE}_1$, a high S-CE_2 and a low S-$\overline{WE}$.
   A write begins at the latest transition among S-$\overline{CE}_1$ going low, S-CE_2 going high and S-$\overline{WE}$ going low.
   A write ends at the earliest transition among S-$\overline{CE}_1$ going high, S-CE_2 going low and S-$\overline{WE}$ going high.
   t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of S-$\overline{CE}_1$ going low or S-CE_2 going high to the end of write.
3. t_{AS} is measured from the address valid to beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applies in case a write ends at S-$\overline{CE}_1$ going high, S-CE_2 going low or S-$\overline{WE}$ going high.
5. During this period DQ pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
6. If S-$\overline{CE}_1$ goes low or S-CE_2 goes high simultaneously with S-$\overline{WE}$ going low or after S-$\overline{WE}$ going low, the outputs remain in high impedance state.
7. If S-$\overline{CE}_1$ goes high or S-CE_2 goes low simultaneously with S-$\overline{WE}$ going high or before S-$\overline{WE}$ going high, the outputs remain in high impedance state.

14. Data Retention Characteristics for SRAM

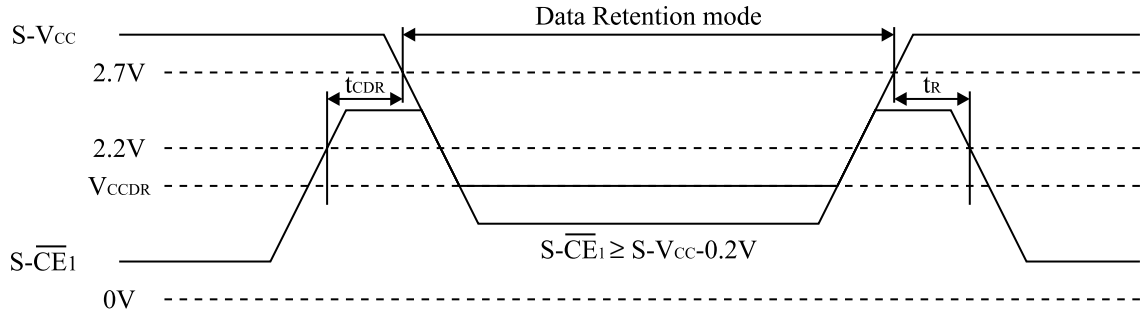
(T_A = -25°C to +85°C)

Symbol	Parameter	Note	Min.	Typ.(1)	Max.	Unit	Conditions
V_{CCDR}	Data Retention Supply voltage	2	2.0		3.6	V	$S\text{-}CE_2 \le 0.2V$ or $S\text{-}\overline{CE}_1 \ge S\text{-}V_{CC} - 0.2V$
I_{CCDR}	Data Retention Supply current	2		1	30	µA	$S\text{-}V_{CC} = 3.0V$ $S\text{-}CE_2 \le 0.2V$ or $S\text{-}\overline{CE}_1 \ge S\text{-}V_{CC} - 0.2V$
t_{CDR}	Chip enable setup time		0			ns	
t_R	Chip enable hold time		5			ms	

Notes

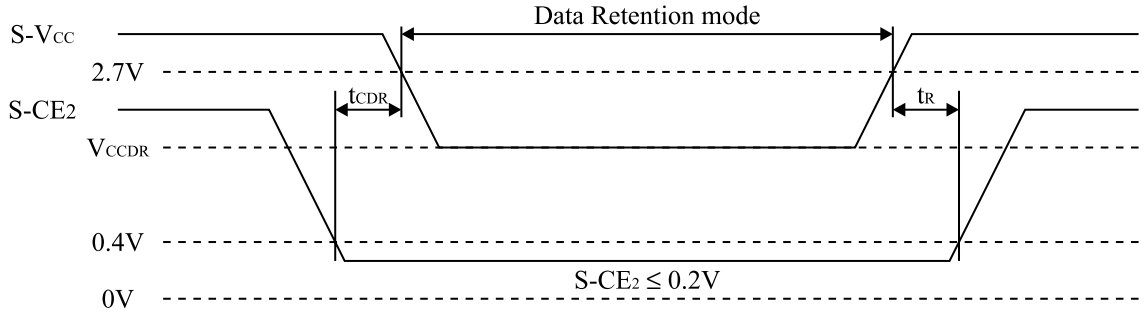
1. Reference value at T_A = 25°C, $S\text{-}V_{CC}$ = 3.0V.
2. $S\text{-}\overline{CE}_1 \ge S\text{-}V_{CC} - 0.2V$, $S\text{-}CE_2 \ge S\text{-}V_{CC} - 0.2V$ ($S\text{-}\overline{CE}_1$ controlled) or $S\text{-}CE_2 \le 0.2V$ ($S\text{-}CE_2$ controlled).

Data Retention timing chart ($S\text{-}\overline{CE}_1$ Controlled)(1)



Note:
1. To control the data retention mode at $S\text{-}\overline{CE}_1$, fix the input level of $S\text{-}CE_2$ between V_{CCDR} and V_{CCDR}-0.2V or 0V or 0.2V and during the data retention mode.

Data Retention timing chart ($S\text{-}CE_2$ Controlled)



15. Notes

This product is a stacked CSP package that a 16M (x8/x16) bit Flash Memory and a 2M (x8) bit SRAM are assembled into.

- Supply Power
  Maximum difference (between F-V_{CC} and S-V_{CC}) of the voltage is less than 0.3V.

- Power Supply and Chip Enable of Flash Memory and SRAM
  S-$\overline{CE}_1$ should not be “low” and S-CE_2 should not be “high” when F-$\overline{CE}$ is “low” simultaneously.
  If the two memories are active together, possibly they may not operate normally by interference noises or data collision on DQ bus.
  Both F-V_{CC} and S-V_{CC} are needed to be applied by the recommended supply voltage at the same time expect SRAM data retention mode.

- Power Up Sequence
  When turning on Flash memory power supply, keep F-$\overline{RP}$ “low”. After F-V_{CC} reaches over 2.7V, keep F-$\overline{RP}$ “low” for more than 100nsec.

- Device Decoupling
  The power supply is needed to be designed carefully because one of the SRAM and the Flash Memory is in standby mode when the other is active. A careful decoupling of power supplies is necessary between SRAM and Flash Memory. Note peak current caused by transition of control signals (F-$\overline{CE}$, S-$\overline{CE}_1$, S-CE_2).

16. Flash Memory Data Protection

Noises having a level exceeding the limit specified in the specification may be generated under specific operating conditions on some systems. Such noises, when induced onto F-$\overline{WE}$ signal or power supply, may be interpreted as false commands, causing undesired memory updating. To protect the data stored in the flash memory against unwanted writing, systems operating with the flash memory should have the following write protect designs, as appropriate.

■ The below describes data protection method.

1. Protecting data in specific block
   - By setting a F-$\overline{WP}$ to low, only the boot block can be protected against overwriting. Parameter and main blocks cannot be locked. System program, etc., can be locked by storing them in the boot block.
   - When a high voltage (V_{HH}) is applied to F-$\overline{RP}$, overwrite operation is enabled for all blocks.
   - For further information on controlling of F-$\overline{WP}$ and F-$\overline{RP}$ refer to the specification. (See Chapter 5. Command Definitions for Flash Memory)

2. Data Protection through F-V_{PP}
   - When the level of F-V_{PP} is lower than V_{PPLK} (lockout voltage), write operation on the flash memory is disabled. All blocks are locked and the data in the blocks are completely write protected.
   - For the lockout voltage, refer to specification. (See Chapter 11. DC Electrical Characteristics)

■ Data Protection during voltage transition

1. Data protection thorough F-$\overline{RP}$
   - When the F-$\overline{RP}$ is kept low during power up and power down sequence, write operation on the flash memory is disabled, write protecting all blocks.
   - For the details of F-$\overline{RP}$ control, refer to the specification. (See Chapter 12. AC Electrical Characteristics for Flash Memory)

17. Design Considerations

1. Power Supply Decoupling

To avoid a bad effect to the system by flash memory power switching characteristics, each device should have a 0.1µF ceramic capacitor connected between its F-V_{CC} and GND and between its F-V_{PP} and GND. Low inductance capacitors should be placed as close as possible to package leads.

2. F-V_{PP} Trace on Printed Circuit Boards

Updating the memory contents of flash memories that reside in the target system requires that the printed circuit board designer pay attention to the F-V_{PP} Power Supply trace. Use similar trace widths and layout considerations given to the F-V_{CC} power bus.

3. The Inhibition of Overwrite Operation

Please do not execute reprogramming “0” for the bit which has already been programed “0”. Overwrite operation may generate unerasable bit.

In case of reprogramming “0” to the data which has been programed “1”.
• Program “0” for the bit in which you want to change data from “1” to “0”.
• Program “1” for the bit which has already been programmed “0”.

For example, changing data from “1011110110111101” to “1010110110111100” requires “1110111111111110” programming.

4. Power Supply

Block erase and word/byte write with an invalid F-V_{PP} (See Chapter 11.DC Electrical Characteristics) produce spurious results and should not be attempted.
Device operations at invalid F-V_{CC} voltage (See Chapter 11.DC Electrical Characteristics) produce spurious results and should not be attempted.

18. Related Document Information(1)

Document No.	Document Name
FUM99903	LH28F400BV, LH28F800BV, LH28F160BV Appendix

Note:
1. International customers should contact their local SHARP or distribution sales offices.

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