

Low-Voltage Single-Chip Microcontrollers with On-Chip PLL and LCD Driver Circuits

Overview

The LC72341G/W, LC72342G/W, and LC72343G/W are single-chip microcontrollers with both a 1/4-duty 1/2-bias LCD driver circuit and a PLL circuit that can operate at up to 250 MHz integrated on the same chip. These ICs are ideal for use in portable audio equipment.

Functions

- · High-speed programmable divider
- Program memory (ROM)
 - LC72341G/W: 2048 words × 16 bits (4KB)
- LC72342G/W: 3072 words × 16 bits (6KB)
- LC72343G/W: 4096 words × 16 bits (8KB)
- Data memory (RAM)
 - LC72341G/W: 128 words \times 4 bits
 - LC72342G/W: 192 words × 4 bits
 - LC72343G/W: 256 words × 4 bits
- · Instruction cycle time
 - 40 μs (for all single-word instructions.)
- Stack
 - 4 levels (LC72341G/W)
 - 8 levels (LC72342G/W, and LC72343G/W)
- LCD driver
 - 48 to 80 segments (1/4-duty 1/2-bias drive)
- Timer interrupts
 - One timer circuit providing intervals of 1, 5, 10, and 50 ms.
- External interrupts
 - One external interrupt (INT)
- A/D converter
 - Two channels (5-bit successive approximation)
- Input ports
 - 7 (Of which two can be switched to function as A/D converter inputs)
- · Output ports
 - 6 (Of which one can be switched to function as the

- BEEP tone output. Two ports are open-drain ports.)
- I/O ports
- 16 (Of which 8 can be selected to function as LCD ports as mask options.)
- PLL circuit
 - Two types of dead band control are supported, and an unlock detection circuit is included.
 - Reference frequencies of 1, 3, 5, 6.25, 12.5, and 25 kHz can be provided.
- · Input frequency range
 - FM band: 10 to 130 MHz

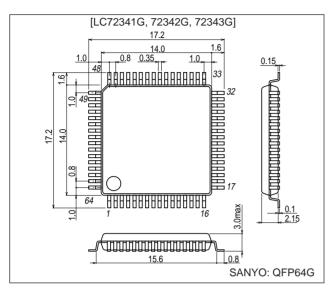
130 to 250 MHz

- AM band: 0.5 to 15 MHz
- IF counter
- HCTR input pin; 0.4 to 12 MHz
- Voltage detection circuit (VSENSE)
 - Detects the V_{DD} voltage and sets a flag
- External reset pin
 - Restarts execution from location 0 when the CPU and PLL circuits are operating
- · Power on reset circuit
 - Starts execution from location 0 at power on.
- · Universal counter
 - 20 bits
- · Beep tones
 - 3.1 and 1.5 kHz
- Halt mode: The microcontroller operating clock is stopped
- Backup mode: The crystal oscillator is stopped
- An amplifier for a low-pass filter is built in
- · CPU and PLL circuit operating voltage
 - 1.8 to 3.6 V
- RAM data retention voltage
 - 1.0 V or higher
- Packages
 - QIP-64G: 0.8-mm lead pitch
 - SQFP-64 : 0.5-mm lead pitch
- Any and all SANYO products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your SANYO representative nearest you before using any SANYO products described or contained herein in such applications.
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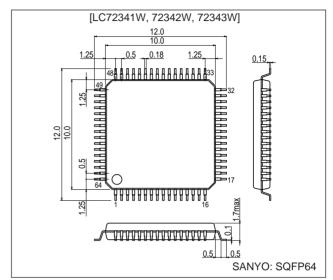
Package Dimensions

unit: mm

3231-QFP64G



unit: mm 3190-SQFP64



Specifications Absolute Maximum Ratings at $Ta=25^{\circ}C,\,V_{SS}=0~V$

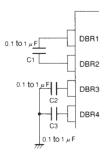
Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{DD} max		-0.3 to +4.0	V
Input voltage	V _{IN}	All input pins	-0.3 to V _{DD} + 0.3	V
Output valtage	V _{OUT} 1	AOUT, PE	-0.3 to +15	V
Output voltage	V _{OUT} 2	All output pins except V _{OUT} 1	-0.3 to V _{DD} to + 0.3	V
	I _{OUT} 1	PC, PD, PG, PH, EO	0 to 3	mA
	I _{OUT} 2	РВ	0 to 1	mA
Output current	I _{OUT} 3	AOUT, PE	0 to 2	mA
	I _{OUT} 4	S1 to S20	300	μA
	I _{OUT} 5	COM1 to COM4	3	mA
Allowable power dissipation	Pd max	$Ta = -20 \text{ to } +70^{\circ}\text{C}$	300	mW
Operating temperature	Topr		-20 to +70	°C
Storage temperature	Tstg		-45 to +125	°C

Allowable Operating Ranges at $Ta=-20\ to\ 70^{\circ}C,\ V_{DD}=1.8\ to\ 3.6\ V$

Dovomotor	Cumphal	Conditions		Ratings			
Parameter	Symbol	Conditions	min typ		max	Unit	
Supply voltage	V _{DD} 1	CPU and PLL operating voltage	1.8	3.0	3.6	V	
Supply voltage	V _{DD} 2	Memory retention voltage	1.0			V	
	V _{IH} 1	V _{IH} 2, V _{IH} 3, AMIN, FMIN, Input ports except HCTR and XIN.	0.7 V _{DD}		V _{DD}	V	
Input high-level voltage	V _{IH} 2	RES	0.8 V _{DD}		V_{DD}	V	
	V _{IH} 3	Port PF	0.6 V _{DD}		V_{DD}	V	
	V _{IL} 1	V _{IL} 2, V _{IL} 3, AMIN, FMIN, Input ports except HCTR and XIN.	0		0.3 V _{DD}	V	
Input low-level voltage	V _{IL} 2	RES	0		0.2 V _{DD}	V	
	V _{IL} 3	Port PF	0		0.2 V _{DD}	V	
	V _{IN} 1	XIN	0.5		0.6	Vrms	
Input amplitude	V _{IN} 2	FMIN, AMIN	0.035		0.35	Vrms	
Input amplitude	V _{IN} 3	FMIN	0.05		0.35	Vrms	
	V _{IN} 4	HCTR	0.035		0.35	Vrms	
Input voltage range	V _{IN} 5	ADI0, ADI1	0		V_{DD}	V	
	F _{IN} 1	XIN : CI ≤ 35 kΩ	70	75	80	kHz	
	F _{IN} 2	FMIN: V _{IN} 2, V _{DD} 1	10		130	MHz	
Input frequency	F _{IN} 3	FMIN: V _{IN} 3, V _{DD} 1	130		250	MHz	
Input frequency	F _{IN} 4	AMIN (H): V _{IN} 2, V _{DD} 1	2		40	MHz	
	F _{IN} 5	AMIN (L) : V _{IN} 2, V _{DD} 1	0.5		10	MHz	
	F _{IN} 6	HCTR: V _{IN} 4, V _{DD} 1	0.4		12	MHz	

Electrical Characteristics at Ta = -20 to $70^{\circ}C$, V_{DD} = 1.8 to 3.6 V (in the allowable operating ranges)

Parameter	Symbol	Conditions		Ratings		Unit
Farameter	Symbol	Conditions	min	typ	max	Offic
	I _{IH} 1	$X_{IN}: V_{I} = V_{DD} = 3.0 \text{ V}$			3	μΑ
land high land amount	I _{IH} 2	FMIN, AMIN, HCTR : $V_I = V_{DD} = 3.0 \text{ V}$	3	8	20	μΑ
Input high-level current	I _{IH} 3	Ports PA/PF (with no pull-down resistor), PC, PD, PG, and PH. \overline{RES} : $V_I = V_{DD} = 3.0 \text{ V}$			3	μА
	I _{IL} 1	$XIN: V_I = V_{DD} = V_{SS}$			-3	μA
	I _{IL} 2	FMIN, AMIN, HCTR : V _I = V _{DD} = V _{SS}	-3	-8	-20	μA
Input low-level current	I _{IL} 3	Ports PA/PF (with no pull-down resistor), PC, PD, PG, and PH. \overline{RES} : $V_I = V_{DD} = V_{SS}$			-3	μΑ
Input floating voltage	V _{IF}	PA/PF with pull-down resistors used			0.05 V _{DD}	V
Pull-down resistance	R _{PD} 1	PA/PF with pull-down resistors used, $V_{DD} = 3 \text{ V}$	75	100	200	kΩ
Hysteresis	V _H	RES	0.1 V _{DD}	0.2 V _{DD}		V
Voltage doubler reference voltage	DBR4	Ta = 25°C, referenced to V_{DD} , C3 = 0.47 μ F	1.3	1.5	1.7	V
Voltage doubler step-up voltage	DBR1, 2, 3	Ta = 25° C, C1 = 0.45μ F, C2 = 0.47μ F, no load	2.7	3.0	3.3	V



Note: C1, C2, and C3 must be provided even if no LCD is used.

Electrical Characteristics at Ta = -30 to 70° C, $V_{DD} = 1.8$ to 3.6 V (in the allowable operating ranges)

Parameter	Cumbal	Conditions		Unit		
Parameter	Symbol	Conditions	min	typ	max	Unit
	V _{OH} 1	PB : I _O = -1 mA	V _{DD} – 0.7 V _{DD}			V
	V _{OH} 2	PC, PD, PG, PH : I _O = -1 mA	V _{DD} – 0.3 V _{DD}			V
	V _{OH} 3	EO : I _O = -500 μA	V _{DD} – 0.3 V _{DD}			V
Output high-level voltage	V _{OH} 4	XOUT : I _O = -200 μA	V _{DD} – 0.3 V _{DD}			V
	V _{OH} 5	S1 to S20 : I _O = -20 μA: *1	2.0			V
	V _{OH} 6	COM1, COM2, COM3, COM4: I _O = -100 μA : *1	2.0			V
	V _{OL} 1	PB : I _O = -50 μA			0.7 V _{DD}	V
	V _{OL} 2	PC, PD, PE, PG, PH : I _O = -1 mA			0.3 V _{DD}	V
	V _{OL} 3	EO : I _O = -500 μA			0.3 V _{DD}	V
	V _{OL} 4	XOUT : I _O = -200 μA			0.3 V _{DD}	V
Output low-level voltage	V _{OL} 5	S1 to S20 : I _O = -20 μA: *1			1.0	V
	V _{OL} 6	COM1, COM2, COM3, COM4 : I _O = -100 μA : *1			1.0	V
	V _{OL} 7	PE : I _O = 5 mA			1.0	٧
	V _{OL} 8	AOUT : I _O = 1 mA, AIN = 1.3 V, V _{DD} = 3 V			0.5	V
Output off leakage current	I _{OFF} 1	Ports PB, PC, PD, PG, PH, and EO	-3		+3	μΑ
Output on leakage current	I _{OFF} 2	Ports AOUT and PE	-100	•	+100	nA
A/D conversion error		ADI0, ADI1, V _{DD} = V _{DD} 1	-1/2		+1/2	LSB

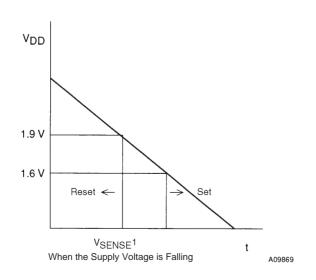
Note: 1. Capacitors C1, C2, and C3 must be connected to the DBR pins.

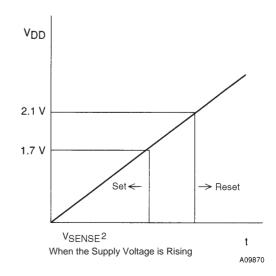
Electrical Characteristics at Ta = -20 to $70^{\circ}C$, $V_{DD} = 1.8$ to 3.6~V (in the allowable operating ranges)

Parameter	Symbol	Conditions		Unit			
Falanetei	Symbol	Conditions	min	typ	max	Offic	
Falling supply voltage detection voltage	V _{SENSE} 1	Ta = 25°C *2	1.6	1.75	1.9	V	
Rising supply voltage detection voltage	V _{SENSE} 2	Ta = 25°C *2	VSENSE1 +0.1		VSENSE1 +0.2	V	
	I _{DD} 1	V _{DD} 1 : F _{IN} 2 130 MHz, Ta = 25°C		5	15	mA	
	I _{DD} 2	V _{DD} 2: In halt mode at Ta = 25°C, *3		0.1		mA	
Supply current	I _{DD} 3	V_{DD} = 3.6 V, with the oscillator stopped, at Ta = 25°C, *4		1		μΑ	
	I _{DD} 4	V_{DD} = 1.8 V, with the oscillator stopped, at Ta = 25°C, *4		0.5		μA	

Notes: 1. The halt mode current is measured with the CPU executing 20 instructions every 125 ms.

When the V_{DD} voltage falls, the V_{SENSE} flag is set at the point that voltage falls under 1.75 V (typical). The TST instruction can be used to read the value of the V_{SENSE} flag. Applications can easily determine when the batteries are exhausted by monitoring this flag. After V_{SENSE} is set when the supply voltage falls, it will not be reset if the supply voltage rises by less than 0.1 V, because the voltages detected by the V_{SENSE} circuit differ when the supply voltage is falling and when the supply voltage is rising.





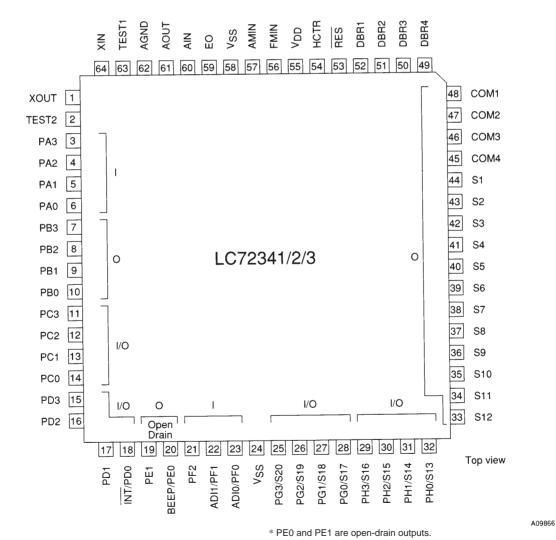
^{2.} The V_{SENSE} voltage

Note: 4. Backup Mode Current Test Circuit

Note: 3. Halt Mode Current Test Circuit

XOUT v_{DD} RES XOUT DBR1 RES V_{DD} DBR1 0.1 u F XIN DBR2 XIN DBR2 DBR3 DBR3 DRRA DBR4 FMIN FMIN V_{SS} PA, PF AMIN ٧ss AMIN HCTR HCTR AGND AGND TEST1. 2 AIN TEST1, 2 AIN All ports other than those specified in the figure All ports other than those specified in the figure A09871 must be left open. Set ports PC and PD to output. must be left open.
Set ports PC and PD to output. A09872 Select segments S13 to S20. Select segments S13 to S20.

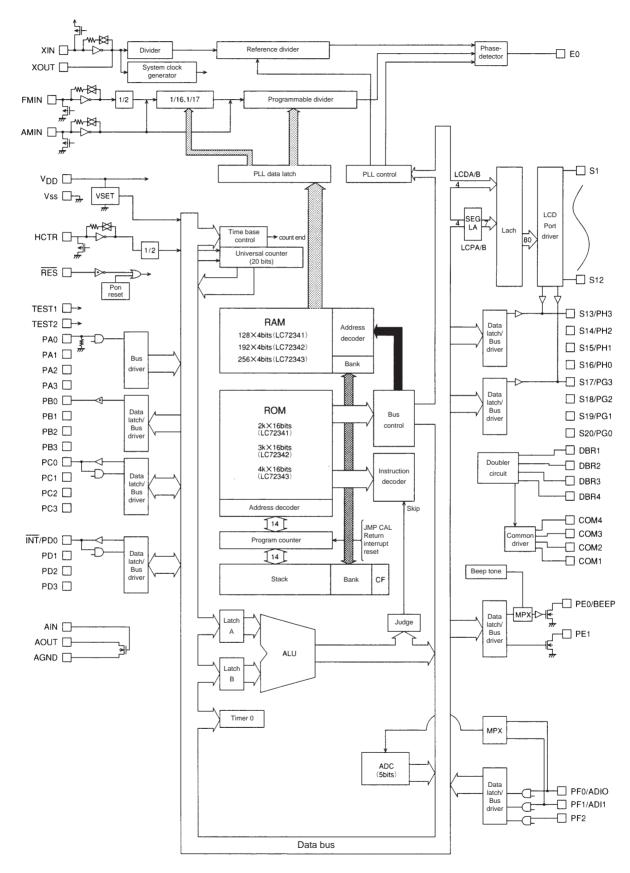
Pin Assignment



^{*} The I/O ports can be set to input or output individually.

 $[\]ensuremath{^*}$ The functions of the segment/general-purpose ports can be set in bit units.

Block Diagram



A09867

Pin Functions

Pin No.	Pin	I/O	Function	I/O circuit
64 1	XIN XOUT	I 0	Connections for a 75-kHz crystal oscillator element	A09873
63 2	TEST1 TEST2	I I	IC test pins. These pins must be tied to ground.	
6 5 4 3	PA0 PA1 PA2 PA3	ı	Special-purpose key return signal input ports designed with a low threshold voltage. When used in conjunction with port PB to form a key matrix, up to 3 simultaneous key presses can be detected. The four pull-down resistors are selected together in a single operation using the IOS instruction (PWn = 2, b1); they cannot be specified individually. Input is disabled in backup mode, and the pull-down resistors are disabled after a reset.	Input with built-in pull-down resistor A09874
10 9 8 7	PB3 PB2 PB1 PB0	0	Special-purpose key source signal output ports. Since unbalanced CMOS output transistor circuits are used, diodes to prevent short-circuits when multiple keys are pressed are not required. These ports go to the output high-impedance state in backup mode. These ports go to the output high-impedance state after a reset and remain in that state until an output instruction (OUT, SPB, or RPB) is executed. Care is required in designing the output loads if these pins are used for functions other than key source outputs.	Unbalanced CMOS push-pull circuit
14 13 12 11 18 17 16 15	PC0 PC1 PC2 PC3 INT/PD0 PD1 PD2 PD3	I/O	General-purpose I/O ports*. PD0 can be used as an external interrupt port. Input or output mode can be set in a bit unit using the IOS instruction (Pwn = 4, 5). A value of 0 specifies input, and 1 specifies output. These ports go to the input disabled high-impedance state in backup mode. They are set to function as general-purpose input ports after a reset.	CMOS push-pull circuit
20 19	BEEP/PE0 PE1		General-purpose output ports with shared beep tone output function (PE0 only). The BEEP instruction is used to switch PE0 between the general-purpose output port and beep tone output functions. To use PE0 as a general-purpose output port, execute a BEEP instruction with b2 set to 0. Set b2 to 1 to use PE0 as the beep tone output port. The b0 and b1 bits are used to select the beep tone frequency. There are two beep tone frequencies supported. When PE0 is set up as the beep tone output, executing an output instruction to PN0 only changes the state of the internal output latch, it does not affect the beep tone output in any way. Only the PE0 pin can be switched between the general-purpose output function and the beep tone output function; the PE1 pin only functions as a general-purpose output. These pins go to the high-impedance state in backup mode and remain in that state until an output instruction or a BEEP instruction is executed. Since these ports are open-drain ports, resistors must be inserted between these pins and V _{DD} . These ports are set to their general-purpose output port function after a reset.	N-channel open drain A09877
23 22 21	PF0/ADI0 PF1/ADI1 PF2	I	General-purpose input and A/D converter input shared function ports (PF2 is a general-purpose input only port). The IOS instruction (Pwn = FH) is used to switch between the general-purpose input and A/D converter port functions. The general-purpose input and A/D converter port functions. The general-purpose input and A/D converter port functions can be switched in a bit unit, with 0 specifying general-purpose input, and 1 specifying the A/D converter input function. To select the A/D converter function, set up the A/D converter pin with an IOS instruction with Pwn set to 1. The A/D converter is started with the UCC instruction (b3 = 1, b2 = 1). The ADCE flag is set when the conversion completes. The INR instruction is used to read in the data. If an input instruction is executed for one of these pins which is set up for analog input, the read in data will be at the low level since CMOS input is disabled. In backup mode these pins go to the input disabled high-impedance state. These ports are set to their general-purpose input port function after a reset. The A/D converter is a 5-bit successive approximation type converter, and features a conversion time of 1.28 ms. Note that the full-scale A/D converter voltage (1FH) is (63 · 96)V _{DD} .	CMOS input/analog input A09878

Note: * Applications must establish the output data in advance with an OUT, SPB, or RPB instruction and then set the pin to output mode with an IOS instruction when using the I/O switchable ports as output pins.

Continued on next page.

Continued from preceding page.

Compared to the continue of	Pin No.	Pin	I/O	Function	I/O circuit
PGS-820 PGS-820 PGS-8219				instruction is used for switching both between the segment output and general-purpose I/O functions and between input and output for the general-purpose I/O port function.* • When used as segment output ports	I CIVICIS DUSD-DUIL CITCUIT
The general-purpose UO port function is selected with the IOS instruction (Pwn = 9): b0 = 131 of 16Ph to 3 (Segment output, 1: Phi to 3) PH3/3168 30 PH2/315 31 PH1/314 32 PH0/S13 32 PH0/S13 33 PH0/S13 34 PH0/S13 35 PH0/S13 36 PH0/S13 37 PH0/S13 38 PH0/S13 39 PH3/S16 30 PH2/S15 31 PH0/S13 30 PH3/S16 30 PH2/S15 31 PH0/S13 31 PH0/S13 32 PH0/S13 32 PH0/S13 33 PH0/S13 34 PH0/S13 35 PH0/S13 35 PH0/S13 35 PH0/S13 36 PH0/S13 37 PH0/S13 38 PH0/S13 38 PH0/S13 39 PH0/S13 30 PH0/	25	PG3/S20			
PG15/18 PG05/17 PG0					<u> </u>
PG0/S17 When used as general-purpose I/O ports PH3/S16 PH3/S16 PH3/S16 PH3/S16 PH4/S13 PH4/S13 PH4/S13 PH5/S15 PH6/S13					
See Set in a bit unit. Do = PGO Do = PHO Do = PHO Do = PGO Do = PGO Do = PHO Do = PGO Do = PHO Do = PGO Do = PGO Do = PHO Do = PGO Do = PGO Do = PHO Do = PGO Do = PGO Do = PGO Do = PHO Do = PGO Do = P	28			When used as general-purpose I/O ports	
PH3/S16 So			I/O		<i>π</i>
PH2/S15	29	PH3/S16			A09879
PHI/S14 PHO/S13 b2 = PG3 (b: Input, 1: Output) b2 = PH2 (b: Input, 1: Output) b3 = PH3 b3 = PH3 b3 = PH3 b3 = PH3 b3 = PH3 b3 = PH3 b3 = PH3 b3 = PH3 b3 = PH3 b3 = PH3 b3 = PH3 b3 = PH3 b3 = PH3 b3 = PH3 b3 = PH3 b3 = PH3 b3 = PH3 b3 = PH3 b3 = PH3 b3 = PH3 b3 = PH3 b3 = PH3 b3 = PH3 b3 = PH3 b3 = PH3 b3 = PH3 b3 = PH3 b3 = PH3 b3 = PH3 b3 = PH3 b3 = PH3 b3 = PH3 b3 = PH3 b3 = PH3 b3 = PH3 b3 = PH3 b3 = PH3 b3 = PH3 b	30	PH2/S15		h1 – PC1 h1 – PH1	
In backup mode, these pins go to the input disabled, high-impedance state if set up as general-purpose outputs, and are fitted at the low level set up as segment outputs. Although the general-purpose port/LCD port set up as segment outputs after set up as segment outputs. Although the general-purpose port/LCD port setting is a mask option, the IOS instruction must be used as described above to set up the port function. CMOS push-pull circuit	31	PH1/S14		[0: Input. 1: Output] [0: Input. 1: Output]	
general-purpose outputs, and are fixed at the low level if set up as segment outputs. These ports are set up as segment outputs after a reset. Although the general-purpose port/LCD port setting is a mask option, the IOS instruction must be used as described above to set up the port function. CMOS push-pull circuit A14-duty 1/2-bias drive technique is used. The frame frequency is 75 Hz. In backup mode, the outputs are fixed at the low level. After a reset, the outputs are fixed at the low level. A14-duty 1/2-bias drive technique is used. CMO3 46 CMO4 47 CMO4 48 CMO5 push-pull circuit A14-duty 1/2-bias drive technique is used. The frame frequency is 75 Hz. In backup mode, the outputs are fixed at the low level. A14-duty 1/2-bias drive technique is used. The frame frequency is 75 Hz. In backup mode, the outputs are fixed at the low level. A14-duty 1/2-bias drive technique is used. The frame frequency is 75 Hz. In backup mode, the outputs are fixed at the low level. A14-duty 1/2-bias drive technique is used. The frame frequency is 75 Hz. In backup mode, the outputs are fixed at the low level. A14-duty 1/2-bias drive technique is used. The frame frequency is 75 Hz. In backup mode, the outputs are fixed at the low level. A14-duty 1/2-bias drive technique is used. The frame frequency is 75 Hz. In CPU operating mode or halt mode, applications must apply a low level for at least one full machine cycle to reset the system and restart execution with the PC set to location 0. This pin is connected in parallel with the internal power on rest circuit. A29882 The CNICA Size in put is a set when the count completes. Since this circuit functions as an AC amplifier, always use capacitor coupling with the input signal. Input is disabled in backup	32	PH0/S13		b3 = PG3 b3 = PH3	
must be used as described above to set up the port function. CMOS push-pull circuit				general-purpose outputs, and are fixed at the low level if set up as segment outputs. These ports are set up as segment outputs after a reset.	
A 1/4-duty 1/2-bias drive technique is used. The frame frequency is 75 Hz. In backup mode, the outputs are fixed at the low level. After a reset, the outputs are fixed at the low level. After a reset, the outputs are fixed at the low level. After a reset, the outputs are fixed at the low level. After a reset, the outputs are fixed at the low level. After a reset, the outputs are fixed at the low level. After a reset, the outputs are fixed at the low level. After a reset, the outputs are fixed at the low level. After a reset, the outputs are fixed at the low level. After a reset, the outputs are fixed at the low level. After a reset, the outputs are fixed at the low level. CDBR4 49 DBR3 50 DBR2 51 DBR1 52 I System reset input. In CPU operating mode or halt mode, applications must apply a low level for at least one full machine cycle to reset the system and restart execution with the PC set to location 0. This pin is connected in parallel with the internal power on reset circuit. Universal counter dedicated input port. - When taking frequency measurement mode and measurement time with the UCS instruction (b3 = 0, b2 = 0) and start the count with a UCCinstruction. CMOS amplifier input The CNTEND flag is set when the count completes. Since this circuit functions as an AC amplifier, always use capacitor coupling with the input signal. Input is disabled in backup					
S16 to S1 33 to 44 O The frame frequency is 75 Hz. In backup mode, the outputs are fixed at the low level. After a reset, the outputs are fixed at the low level. After a reset, the outputs are fixed at the low level. After a reset, the outputs are fixed at the low level. A 1/4-duty 1/2-bias drive technique is used. The frame frequency is 75 Hz. In backup mode, the outputs are fixed at the low level. After a reset, the outputs are fixed at the low level. After a reset, the outputs are fixed at the low level. After a reset, the outputs are fixed at the low level. After a reset, the outputs are fixed at the low level. CD power supply stepped-up voltage pins. System reset input. In CPU operating mode or halt mode, applications must apply a low level for at least one full machine cycle to reset the system and restart execution with the PC set to location 0. This pin is connected in parallel with the internal power on reset circuit. Universal counter dedicated input port. When taking frequency measurement mode and measurement time with the UCS instruction (to 3 = 0, b2 = 0) and start the count with a UCCinstruction. US by by by pin Measurement mode and measurement time with the UCS instruction (to 3 = 0, b2 = 0) and start the count with a UCCinstruction. LOS by by by pin Measurement mode and measurement time with the UCS instruction (to 3 = 0, b2 = 0) and start the count with a UCCinstruction. The ONTEND flag is set when the count completes. Since this circuit functions as an AC amplifier, always use capacitor coupling with the input signal. Input is disabled in backup					CMOS push-pull circuit
S1 33 to 44 O In terms frequency is 75 Hz. In backup mode, the outputs are fixed at the low level. After a reset, the Outputs are fixed at the low level. After a reset, the Outputs are fixed at the low level. AD0880 LCD driver common output pins. A 1/4-duty 1/2-bias drive technique is used. The frame frequency is 75 Hz. In backup mode, the outputs are fixed at the low level. After a reset, the outputs are fixed at the low level. After a reset, the outputs are fixed at the low level. After a reset, the outputs are fixed at the low level. LCD power supply stepped-up voltage pins. ECD power supply stepped-up voltage pins. System reset input. In CPU operating mode or halt mode, applications must apply a low level for at least one full machine cycle to reset the system and restart execution with the PC set to location 0. This pin is connected in parallel with the internal power on reset circuit. Universal counter dedicated input port. • When taking frequency measurement select the HCTR frequency measurement mode and measurement time with the UCS instruction (b3 = 0, b2 = 0) and start the count with a UCCinstruction. When taking frequency measurements. select the HCTR frequency measurement mode and measurement time with the UCS instruction (b3 = 0, b2 = 0) and start the count with a UCCinstruction. Who is a local in the internal power on reset circuit.	S16 to				_ }⊢
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COM4 45 COM3 46 COM2 47 COM1 48 DBR4 49 DBR3 50 DBR2 51 DBR1 52 System reset input. In CPU operating mode or halt mode, applications must apply a low level for at least one full machine cycle to reset the system and restart execution with the PC set to location 0. This pin is connected in parallel with the internal power on reset circuit. Universal counter dedicated input port. When taking frequency measurement on the and measurement time with the UCS instruction (b3 = 0, b2 = 0) and start the count with a UCCinstruction. UCS b3, b2 Input pin Measurement mode and measurement time with the UCS instruction (b3 = 0, b2 = 0) and start the count with a UCCinstruction. UCS b3, b2 Input pin Measurement mode and measurement time with the UCS instruction (b3 = 0, b2 = 0) and start the count with a UCCinstruction. The CNTEND flag is set when the count completes. Since this circuit unctions as an AC ampliffer, always use capacitor coupling with the input signal. Input is disabled in backup					<i>"</i>
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COM2 47 COM1 48 O The frame frequency is 75 Hz. In backup mode, the outputs are fixed at the low level. After a reset, the outputs are fixed at the low level. After a reset, the outputs are fixed at the low level. LCD power supply stepped-up voltage pins. CDM2 51	COM4	45		LCD driver common output pins.	
In backup mode, the outputs are fixed at the low level.	сомз	46			
After a reset, the outputs are fixed at the low level. DBR4	COM2	47	0		
DBR4 49 DBR3 50 DBR2 51 DBR1 52 System reset input. In CPU operating mode or halt mode, applications must apply a low level for at least one full machine cycle to reset the system and restart execution with the PC set to location 0. This pin is connected in parallel with the internal power on reset circuit. 1 Universal counter dedicated input port. • When taking frequency measurements, select the HCTR frequency measurement mode and measurement time with the UCS instruction (b3 = 0, b2 = 0) and start the count with a UCCinstruction. UCS b3, b2 Input pin Measurement mode and measure	COM1	48			—
DBR3 50 DBR2 51 DBR1 52 System reset input. In CPU operating mode or halt mode, applications must apply a low level for at least one full machine cycle to reset the system and restart execution with the PC set to location 0. This pin is connected in parallel with the internal power on reset circuit. Universal counter dedicated input port. When taking frequency measurement mode and measurement time with the UCS instruction (b3 = 0, b2 = 0) and start the count with a UCCinstruction. UCS b3, b2 Input pin Measurement mode and measurement mode and measurement time with the UCS instruction (b3 = 0, b2 = 0) and start the count with a UCCinstruction. UCS b3, b2 Input pin Measurement mode and mea				Arter a reset, the outputs are fixed at the low level.	A09881
DBR2 51 DBR1 52 CDD power supply stepped-up voltage pins.	DBR4	49			
DBR2 51 DBR1 52 System reset input. In CPU operating mode or halt mode, applications must apply a low level for at least one full machine cycle to reset the system and restart execution with the PC set to location 0. This pin is connected in parallel with the internal power on reset circuit. Universal counter dedicated input port. When taking frequency measurements, select the HCTR frequency measurement mode and measurement time with the UCS instruction (b3 = 0, b2 = 0) and start the count with a UCCinstruction. UCS b3, b2 Input pin Measurement mode and measurement mode UCS b1, b0 Measurement time 0 0 1 ms 0 1 4 ms 0 1 4 ms 1 0 8 ms 1 1 1 32	DBR3	50	_	LCD power supply stepped-up voltage pins.	
System reset input. In CPU operating mode or halt mode, applications must apply a low level for at least one full machine cycle to reset the system and restart execution with the PC set to location 0. This pin is connected in parallel with the internal power on reset circuit. *Universal counter dedicated input port. *When taking frequency measurements, select the HCTR frequency measurement mode and measurement time with the UCS instruction (b3 = 0, b2 = 0) and start the count with a UCCinstruction. UCS b3, b2				Franci called all countries	
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full machine cycle to reset the system and restart execution with the PC set to location 0. This pin is connected in parallel with the internal power on reset circuit. Value of the provided in parallel with the internal power on reset circuit.				System reset input.	T-17>-
full machine cycle to reset the system and restart execution with the PC set to location 0. This pin is connected in parallel with the internal power on reset circuit. Universal counter dedicated input port. When taking frequency measurements, select the HCTR frequency measurement mode and measurement time with the UCS instruction (b3 = 0, b2 = 0) and start the count with a UCCinstruction. The CNTEND flag is set when the count completes. Since this circuit functions as an AC amplifier, always use capacitor coupling with the input signal. Input is disabled in backup	53	RES	1	1 11 11 11 11 11 11 11 11 11 11 11 11 1	
Owhen taking frequency measurements, select the HCTR frequency measurement mode and measurement time with the UCS instruction (b3 = 0, b2 = 0) and start the count with a UCCinstruction. UCS b3, b2 Input pin Measurement mode UCS b1, b0 Measurement time 0 0 1 ms 1 0 ms 1					
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HCTR I O 0 HCTR Frequency measurement O 0 1 ms O 1 4 ms I 0 8 ms I 1 1 32 ms The CNTEND flag is set when the count completes. Since this circuit functions as an AC amplifier, always use capacitor coupling with the input signal. Input is disabled in backup				UCS b3, b2 Input pin Measurement mode UCS b1, b0 Measurement time	
The CNTEND flag is set when the count completes. Since this circuit functions as an AC amplifier, always use capacitor coupling with the input signal. Input is disabled in backup	70	LICTO	.	0 0 HCTR Frequency measurement 0 0 1 ms	<u></u> }⊢
The CNTEND flag is set when the count completes. Since this circuit functions as an AC amplifier, always use capacitor coupling with the input signal. Input is disabled in backup	70	HCTR	'	0 1 — 0 1 4ms	<i>m</i>
The CNTEND flag is set when the count completes. Since this circuit functions as an AC amplifier, always use capacitor coupling with the input signal. Input is disabled in backup				1 0 — 1 0 8 ms	A09883
amplifier, always use capacitor coupling with the input signal. Input is disabled in backup				1 1 1 — 1 1 32 ms	
				amplifier, always use capacitor coupling with the input signal. Input is disabled in backup	II

Note: * Applications must establish the output data in advance with an OUT, SPB, or RPB instruction and then set the pin to output mode with an IOS instruction when using the I/O switchable ports as output pins.

Continued on next page.

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Pin No.	Pin	I/O	Function	I/O circuit
56	FMIN	I	FM VCO (local oscillator) input. This pin is selected with the PLL instruction CW1. The input must be capacitor coupled. Input is disabled in backup mode, in halt mode, after a reset, and in PLL stop mode.	CMOS amplifier input
57	AMIN	I	AM VCO (local oscillator) input. This pin and the bandwidth are selected with the PLL instruction CW1. CW1 b1, b0 Bandwidth 1 0 2 to 40 MHz (SW) 1 1 0.5 to 10 MHz (MW, LW) The input must be capacitor coupled. Input is disabled in backup mode, in halt mode, after a reset, and in PLL stop mode.	CMOS amplifier input
59	E0	0	The main charge pump output. When the local oscillator frequency divided by N is higher than the reference frequency a high level is output, when lower, a low level is output, and the pin is set to the high-impedance state when the frequencies match. Output goes to the high-impedance state in backup mode, in halt mode, after a reset, and in PLL stop mode.	Push-pull CMOS output
60 61 62	AIN AOUT AGND	0	Transistor used for the low-pass filter amplifier. Connect AGND to ground.	A09887
24 58 55	V _{SS} V _{SS} V _{DD}	_ _ _	Power supply pin. This pin must be connected to ground. Power supply pin. This pin must be connected to ground. Power supply pin. This pin must be connected to V _{DD} .	

Handling of Unused Pins

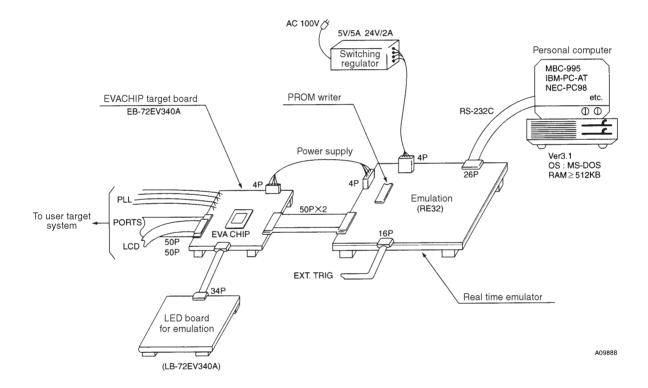
Pin No.	Pin	I/O type	Pin handling
3 to 6	PA port	I	Connect to V _{DD} or V _{SS} . May be left open if the pull-up resistor is selected with the IOS instruction.
7 to 10	PB port	0	Open
11 to 14	PC port	I/O	Connect to V _{DD} or V _{SS} when input is selected. Leave open if output is selected.
15 to 18	PD port	I/O	Connect to V_{DD} or V_{SS} when input is selected. Leave open if output is selected.
19, 20	PE port	0	Open
21 to 23	PF port	I	Connect to V _{DD} or V _{SS} . The PF2 pin only may be left open if the pull-up resistor is selected with the IOS instruction.
25 to 28	PG/S ports	I/O/S	Connect to V_{DD} or V_{SS} when input is selected. Leave open if output or LCD operation is selected.
29 to 32	PH/S ports	I/O/S	Connect to V_{DD} or V_{SS} when input is selected. Leave open if output or LCD operation is selected.
33 to 41	S port	0	Open
45 to 48	COM	0	Open
49	DBR1	_	Connect to DBR2 through a capacitor.
50	DBR2	_	Connect to DBR1 through a capacitor.
51	DBR3	_	Connect to V _{SS} through a capacitor.
52	DBR4	_	Connect to V _{SS} through a capacitor.
53	RES	I	V_{DD}
54	HCTR	I	V _{SS} Leave open if FMIN is used.
56	FMIN	I	Vss
57	AMIN	I	Vss
59	EO	0	Open
60	AIN	I	V _{SS}
61	AOUT	0	Open
63	TEST1	I	Connect to V _{SS} or leave open. Connection to V _{SS} is preferable.
2	TEST2	I	Connect to V _{SS} or leave open. Connection to V _{SS} is preferable.

Mask Options

	Port	Selection				
1	PG3/S20	General-purpose port	LCD port			
2	PG2/S19	General-purpose port	LCD port			
3	PG1/S18	General-purpose port	LCD port			
4	PG0/S17	General-purpose port	LCD port			
5	PH3/S16	General-purpose port	LCD port			
6	PH2/S15	General-purpose port	LCD port			
7	PH1/S14	General-purpose port	LCD port			
8	PH0/S13	General-purpose port	LCD port			

Development Environment and Tools

- The LC72P341 is available as a OTP version.
- The LC72EV340 is available as an evaluation chip.
- A total debugging system is formed by the combination of the TB-72EV32 evaluation chip board, the RE32 multifunction emulator, and a personal computer for system control.



Instruction Set

Instruction		Opco	ode	Machine code					
group	Mnemonic	1st	2nd	15 12	11	8	7 4	3 0	Operation
	AD	r	М	0100	00	DH	DL	r	$r \leftarrow (r) + (M)$
Si	ADS	r	М	0100	01	DH	DL	r	$r \leftarrow (r) + (M)$, skip if carry
tior	AC	r	М	0100	10	DH	DL	r	$r \leftarrow (r) + (M) + C$
struc	ACS	r	М	0100	11	DH	DL	¦ r	$r \leftarrow (r) + (M) + C$, skip if carry
Addition instructions	Al	M	I	0101	00	DH	DL	1	M ← (M) + I
iţi.	AIS	М	ı	0101	01	DH	DL		$M \leftarrow (M) + I$, skip if carry
Adc	AIC	М	ı	0101	10	DH	DL	<u> </u>	$M \leftarrow (M) + I + C$
	AICS	М	ı	0101	11	DH	DL	1	$M \leftarrow (M) + I + C$, skip if carry
	SU	r	М	0110	00	DH	DL	r r	$r \leftarrow (r) - (M)$
suc	SUS	r	М	0110	01	DH	DL	r	$r \leftarrow (r) - (M)$, skip if borrow
nctic	SB	r	М	0110	10	DH	DL	r	$r \leftarrow (r) - (M) - b$
nstrı	SBS	r	М	0110	11	DH	DL	r	$r \leftarrow (r) - (M) - b$, skip if borrow
i no	SI	М	ı	0111	00	DH !	DL		$M \leftarrow (M) - I$
acti	SIS	М	ı	0111	01	DH	DL		$M \leftarrow (M) - I$, skip if borrow
Subtraction instructions	SIB	М	I	0111	10	DH	DL	1	$M \leftarrow (M) - I - b$
U)	SIBS	М	I	0111	11	DH	DL	<u> </u>	$M \leftarrow (M) - I - b$, skip if borrow
	SEQ	r	М	0001	00	DH	DL	r	$(r) \leftarrow (M)$, skip if zero
_ ∽	SEQI	М	ı	0001	10	DH !	DL		(M) — I, skip if zero
Comparison instructions	SNEI	М	ı	0000	01	DH	DL	<u> </u>	(M) — I, skip if not zero
mpa	SGE	r	М	0001	10	DH	DL	r	(r) — (M), skip if not borrow
Si	SGEI	М	ı	0001	11	DH	DL		(M) — I, skip if not borrow
	SLEI	М	ı	0000	11	DH	DL	<u> </u>	(M) — I, skip if borrow
	ANDI	М	I	0010	01	DH	DL		$M \leftarrow (M) \text{ AND I}$
Logic and arithmetic instructions	ORI	М	I	0010	11	DH	DL	1	$M \leftarrow (M) \text{ OR } I$
thm	EXLI	М	I	0011	10	DH	DL	1	$M \leftarrow (M) XOR I$
c and arithm instructions	AND	r	М	0010	00	DH	DL	r r	$r \leftarrow (r) \text{ AND M}$
and	OR	r	М	0010	10	DH	DL	r	$r \leftarrow (r) OR M$
ogic i	EXL	r	М	0011	00	DH	DL	r	$r \leftarrow (r) XOR M$
_	SHR	r		0000	00	00	1110	r r	Shift r right with carry
SL	LD	r	М	1101	00	DH	DL	r	$r \leftarrow (M)$
ction	ST	М	r	1101	01	DH	DL	r	$M \leftarrow (r)$
stru	MVRD	r	М	1101	10	DH	DL	r	$[DH, rn] \leftarrow (M)$
je ⊒.	MVRS	М	r	1101	11	DH	DL	r	$M \leftarrow [DH, rn]$
Transfer instructions	MVSR	M1	M2	1110	00	DH	DL1	DL2	[DH, DL1] ← [DH, DL2]
Tr _S	MVI	М	I	1110	01	DH	DL	1	$M \leftarrow I$
Memory	TMT	М	N	1111	00	DH	DL	N	if M (N) = all 1, then skip
test instructions	TMF	М	N	1111	01	DH	DL	N	if M (N) = all 0, then skip
e e	JMP	AD	DR	100		ADE	DR (13 bits)	PC ← ADDR
utin III	CAL	AD	DR	101		ADE	DR (13 bits)	$PC \leftarrow ADDR$, $Stack \leftarrow (PC) + 1$
Jump and subroutine call instructions	RT			0000	00	00	1000	1	PC ← Stack
J.S. ∵E	RTI			0000	00	00	1001	i I	$PC \leftarrow Stack, BANK \leftarrow Stak, carry \leftarrow stack$
Q.	SS	I	N	1111	11	11	000 1	l N	(Status reg. I)N ← 1
ster 5-flo	RS	I	N	1111	11	11	001¦I	N	(Status reg. I)N ← 0
d flip	TST	I	N	1111	11	11	01 1	N	if (Status reg. I)N = all 1, then skip
Status register test and flip-flop control instructions	TSF	I	N	1111	11	11	10 I	N	if (Status reg. I)N = all 0, then skip
Sta tes cor inst	TUL	N		0000	00	00	1101	N	if Unlock F/F (N) = all 0, then skip

Continued on next page.

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Instruction		Opco	ode		Machine o			
group	Mnemonic	1st	2nd	15 12	11 8	7 4	3 0	Operation
<u>6</u>	PLL	М	r	1111	10 DH	DL	r	PLL reg. ← PLL data
ontr	TMS	I		0000	0000	1100	ı	Timer reg. ← I
Peripheral hardware control instructions	UCS	I		0000	0000	0001	I	UCS reg. ← I
al hardware instructions	UCC	I		0000	0000	0010	l I	UCC reg. ← I
l har	BEEP	I		0000	0000	0110	I	BEEP reg. ← I
in	DZC	I		0000	0000	1011	ı	DZC reg. ← I
- July - I	BANK	I		0000	0000	0111	l I	BANK ← I
Pe	IOS	Pn	I	1111	1110	Pn	I	IOS reg. Pn ← I
	INR	M	Rn	0011	10 DH	DL	r	M ← (Rn reg.)
် ရ	IN	М	Pn	1110	10 ¦DH	DL	Pn	$M \leftarrow (Pn)$
l stio	OUT	M	Ph	1110	11 DH	DL	Pn	$Pn \leftarrow M$
stru	SPB	Pn	N	0000	0010	Pn	N	(Pn) N ← 1
I/O instructions	RPB	Pn	N	0000	0011	Pn	N	(Pn) N ← 0
=	TPT	Pn	N	1111	1100	Pn	į N	if (Pn) N = all 1, then skip
	TPF	Pn	N	1111	1101	¦ Pn	l N	if (Pn) N = all 0, then skip
lor	LCDA	M	1	1100	00 DH	DL	DIGIT	LCD (DIGIT) ← M
ction	LCDB	М	1	1100	01 DH	DL	DIGIT	
LCD control instructions	LCPA	M	1	1100	10 DH	DL	DIGIT	LCD (DIGIT) ← Logic
ij	LCPB	M	I	1100	11 DH	DL	DIGIT	Array ← M
r	HALT	I		0000	0000	0100	ļ Ī	HALT reg. ← I, then CPU Stop
Other	CKSTP			0000	0000	0101		Stop Xtal OSC
inst	NOP			0000	0000	0000	į	No operation

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