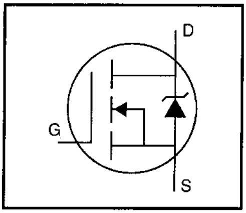
International Rectifier

PD-9.855

# IRFIBF20G

HEXFET® Power MOSFET

- Isolated Package
- High Voltage Isolation= 2.5KVRMS ⑤
- Sink to Lead Creepage Dist.= 4.8mm
- Dynamic dv/dt Rating
- Low Thermal Resistance




$V_{DSS}$ = 900V

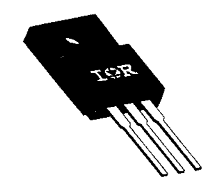
$R_{DS(on)}$ = 8.0Ω

$I_D$ = 1.2A

## Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 Fullpak eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The Fullpak is mounted to a heatsink using a single clip or by a single screw fixing.



TO-220 FULLPAK

DATA SHEETS

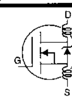
## Absolute Maximum Ratings

| | Parameter | Max. | Units |
|---|---|---|---|
| $I_D$ @ $T_C$ = 25°C | Continuous Drain Current, $V_{GS}$ @ 10 V | 1.2 | A |
| $I_D$ @ $T_C$ = 100°C | Continuous Drain Current, $V_{GS}$ @ 10 V | 0.79 | |
| $I_{DM}$ | Pulsed Drain Current ① | 4.8 | |
| $P_D$ @ $T_C$ = 25°C | Power Dissipation | 30 | W |
| | Linear Derating Factor | 0.24 | W/°C |
| $V_{GS}$ | Gate-to-Source Voltage | ±20 | V |
| $E_{AS}$ | Single Pulse Avalanche Energy ② | 150 | mJ |
| $I_{AR}$ | Avalanche Current ① | 1.2 | A |
| $E_{AR}$ | Repetitive Avalanche Energy ① | 3.0 | mJ |
| dv/dt | Peak Diode Recovery dv/dt ③ | 1.5 | V/ns |
| $T_J$<br>$T_{STG}$ | Operating Junction and<br>Storage Temperature Range | -55 to +150 | °C |
| | Soldering Temperature, for 10 seconds | 300 (1.6mm from case) | |
| | Mounting Torque, 6-32 or M3 screw | 10 lbf•in (1.1 N•m) | |

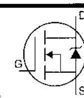
## Thermal Resistance

| | Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $R_{θJC}$ | Junction-to-Case | — | — | 4.1 | °C/W |
| $R_{θJA}$ | Junction-to-Ambient | — | — | 65 | |

# Electrical Characteristics @ $T_J$ = 25°C (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | 900 | — | — | V | $V_{GS}$=0V, $I_D$= 250µA |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | — | 1.1 | — | V/°C | Reference to 25°C, $I_D$= 1mA |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | — | — | 8.0 | Ω | $V_{GS}$=10V, $I_D$=0.72A ④ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 2.0 | — | 4.0 | V | $V_{DS}$=$V_{GS}$, $I_D$= 250µA |
| $g_{fs}$ | Forward Transconductance | 0.90 | — | — | S | $V_{DS}$=50V, $I_D$=0.72A ④ |
| $I_{DSS}$ | Drain-to-Source Leakage Current | — | — | 100 | µA | $V_{DS}$=900V, $V_{GS}$=0V |
| | | — | — | 500 | | $V_{DS}$=720V, $V_{GS}$=0V, $T_J$=125°C |
| $I_{GSS}$ | Gate-to-Source Forward Leakage | — | — | 100 | nA | $V_{GS}$=20V |
| | Gate-to-Source Reverse Leakage | — | — | -100 | | $V_{GS}$=-20V |
| $Q_g$ | Total Gate Charge | — | — | 38 | nC | $I_D$=1.7A |
| $Q_{gs}$ | Gate-to-Source Charge | — | — | 4.7 | | $V_{DS}$=360V |
| $Q_{gd}$ | Gate-to-Drain ("Miller") Charge | — | — | 21 | | $V_{GS}$=10V See Fig. 6 and 13 ④ |
| $t_{d(on)}$ | Turn-On Delay Time | — | 8.0 | — | ns | $V_{DD}$=450V |
| $t_r$ | Rise Time | — | 21 | — | | $I_D$=1.7A |
| $t_{d(off)}$ | Turn-Off Delay Time | — | 56 | — | | $R_G$=18Ω |
| $t_f$ | Fall Time | — | 32 | — | | $R_D$=280Ω See Figure 10 ④ |
| $L_D$ | Internal Drain Inductance | — | 4.5 | — | nH | Between lead, 6 mm (0.25in.) from package and center of die contact  |
| $L_S$ | Internal Source Inductance | — | 7.5 | — | | |
| $C_{iss}$ | Input Capacitance | — | 490 | — | pF | $V_{GS}$=0V |
| $C_{oss}$ | Output Capacitance | — | 55 | — | | $V_{DS}$=25V |
| $C_{rss}$ | Reverse Transfer Capacitance | — | 18 | — | | $f$=1.0MHz See Figure 5 |
| C | Drain to Sink Capacitance | — | 12 | — | pF | $f$=1.0MHz |

# Source-Drain Ratings and Characteristics

| | Parameter | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current (Body Diode) | — | — | 1.2 | A | MOSFET symbol showing the integral reverse p-n junction diode.  |
| $I_{SM}$ | Pulsed Source Current (Body Diode) ① | — | — | 4.8 | | |
| $V_{SD}$ | Diode Forward Voltage | — | — | 1.5 | V | $T_J$=25°C, $I_S$=1.2A, $V_{GS}$=0V ④ |
| $t_{rr}$ | Reverse Recovery Time | — | 350 | 530 | ns | $T_J$=25°C, $I_F$=1.7A |
| $Q_{rr}$ | Reverse Recovery Charge | — | 0.85 | 1.3 | µC | di/dt=100A/µs ④ |
| $t_{on}$ | Forward Turn-On Time | Intrinsic turn-on time is neglegible (turn-on is dominated by $L_S$+$L_D$) | | | | |

Notes:

① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)

② $V_{DD}$=50V, starting $T_J$=25°C, L=196mH $R_G$=25Ω, $I_{AS}$=1.2A (See Figure 12)

③ $I_{SD}$≤1.7A, di/dt≤70A/µs, $V_{DD}$≤600 , $T_J$≤150°C

④ Pulse width ≤ 300 µs; duty cycle ≤2%.

⑤ t=60s, $f$=60Hz

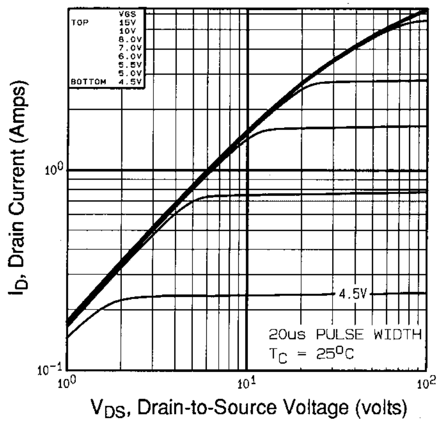



**Fig 1.** Typical Output Characteristics, $T_C$=25°C

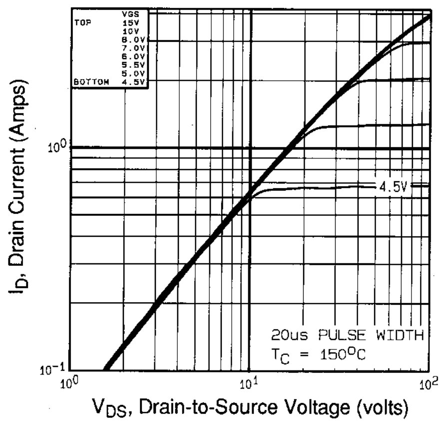



**Fig 2.** Typical Output Characteristics, $T_C$=150°C



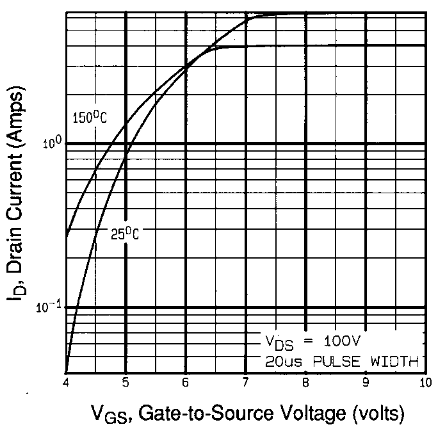



**Fig 3.** Typical Transfer Characteristics

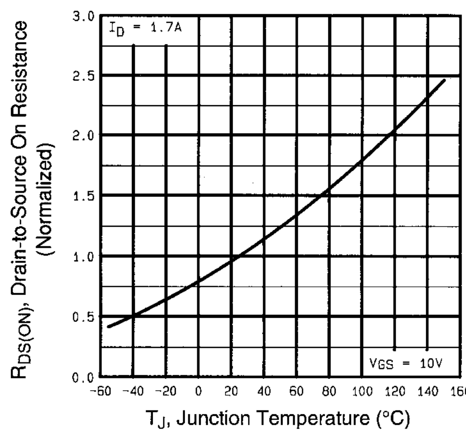



**Fig 4.** Normalized On-Resistance Vs. Temperature

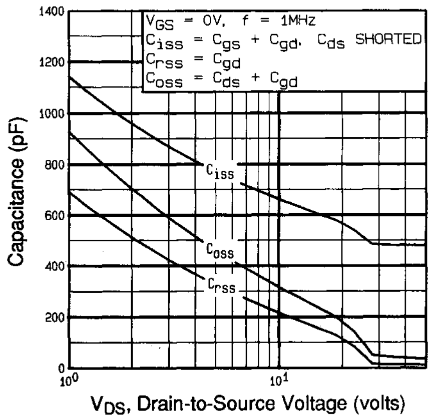



**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage

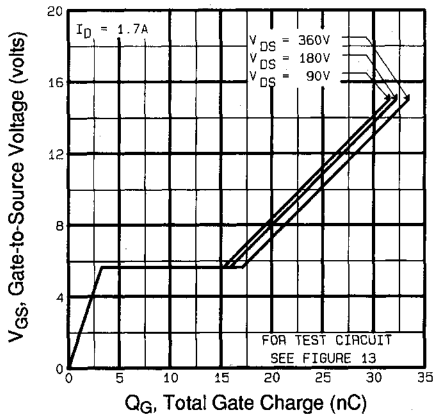



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage

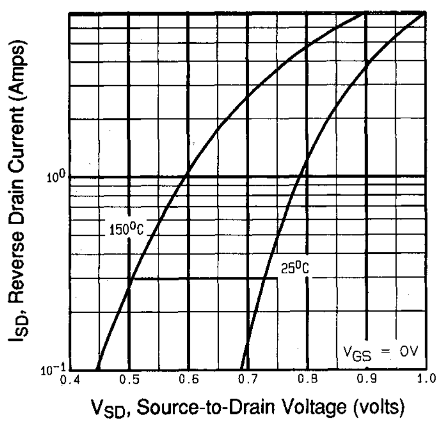



**Fig 7.** Typical Source-Drain Diode Forward Voltage

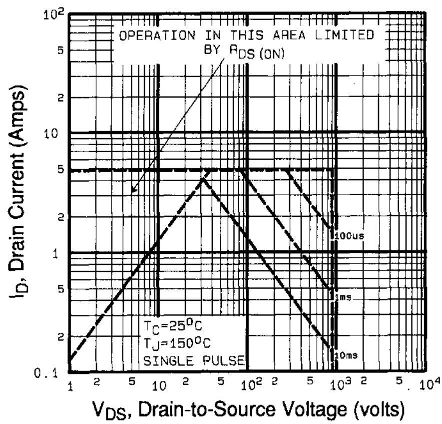



**Fig 8.** Maximum Safe Operating Area

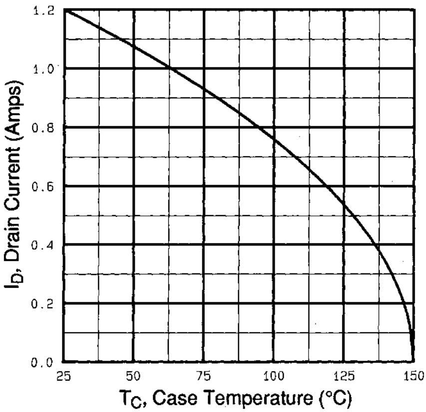



**Fig 9.** Maximum Drain Current Vs. Case Temperature

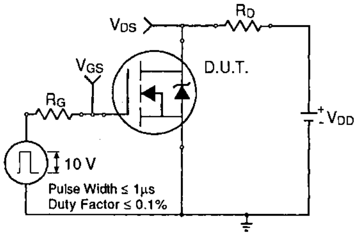



**Fig 10a.** Switching Time Test Circuit

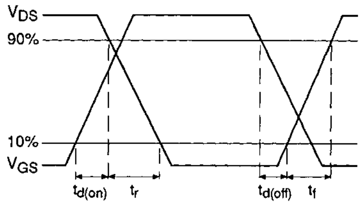



**Fig 10b.** Switching Time Waveforms



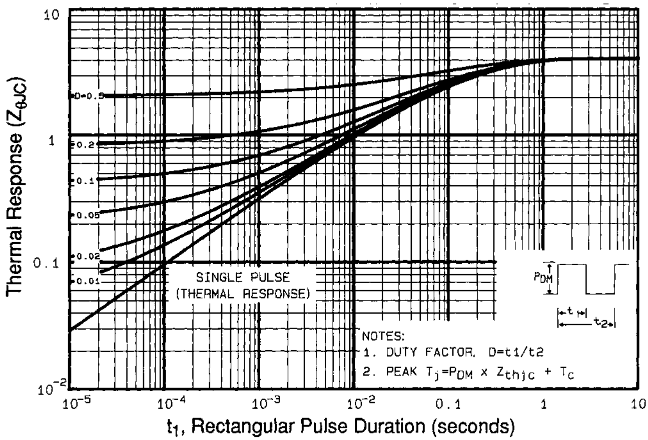



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

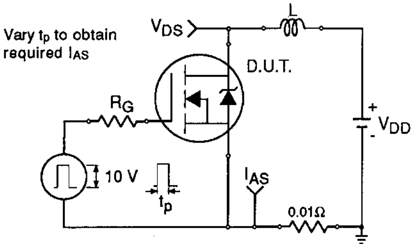



**Fig 12a.** Unclamped Inductive Test Circuit

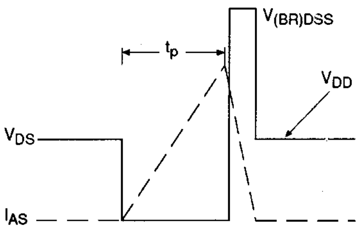



**Fig 12b.** Unclamped Inductive Waveforms

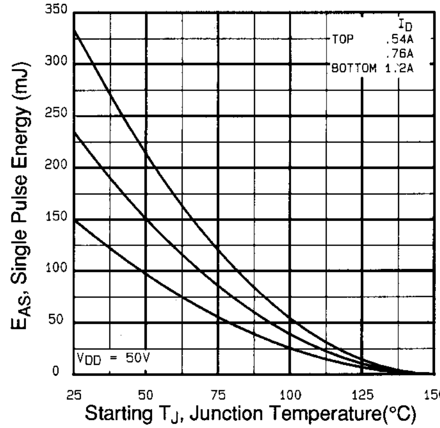



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

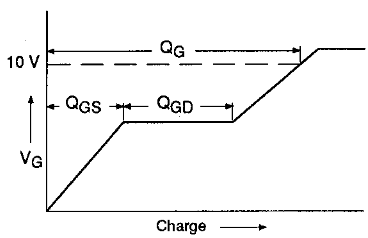



**Fig 13a.** Basic Gate Charge Waveform

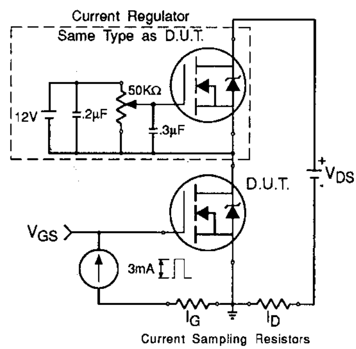



**Fig 13b.** Gate Charge Test Circuit

**Appendix A:** Figure 14, Peak Diode Recovery dv/dt Test Circuit – See page 1505

**Appendix B:** Package Outline Mechanical Drawing – See page 1510

**Appendix C:** Part Marking Information – See page 1517

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