



3.3V CMOS 32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS, 5 VOLT TOLERANT I/O, BUS-HOLD

IDT74LVCH32374A

FEATURES:

- Typical $t_{sk(o)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{CC} = 3.3V \pm 0.3V$, Normal Range
- $V_{CC} = 2.7V$ to $3.6V$, Extended Range
- CMOS power levels (0.4 μ W typ. static)
- All inputs, outputs, and I/O are 5V tolerant
- Supports hot insertion
- Available in 96-ball LFBGA package

DRIVE FEATURES:

- Balanced Output Drivers: $\pm 24mA$

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

DESCRIPTION:

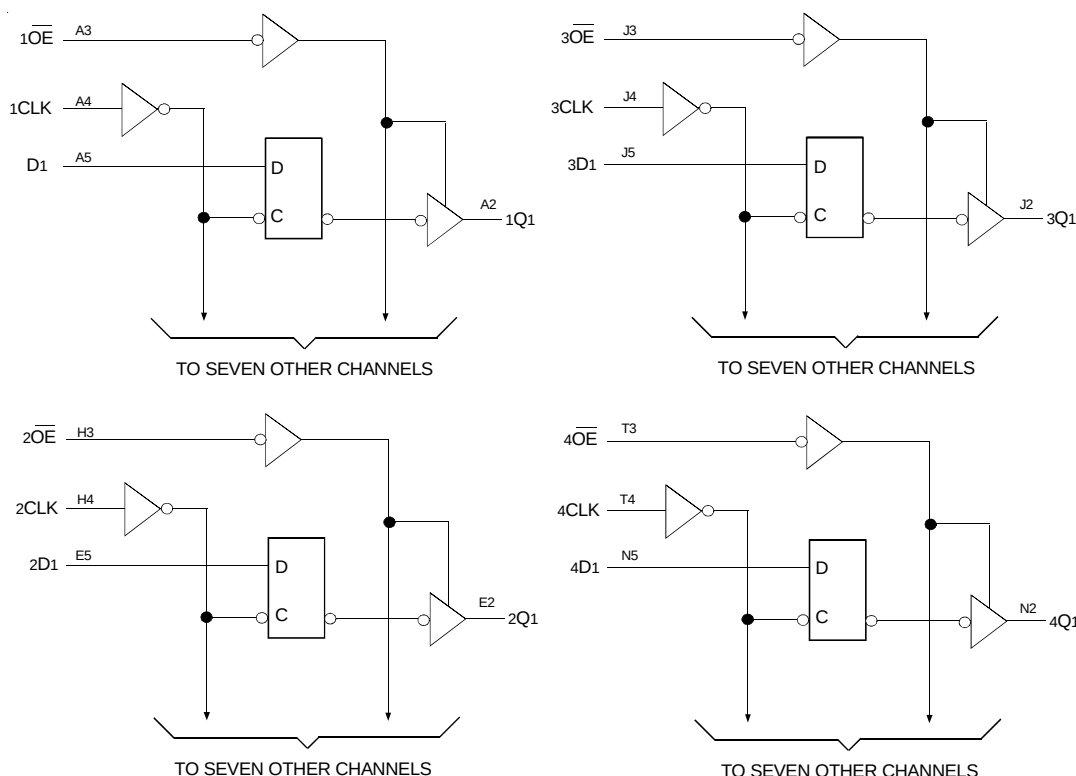
The LVCH32374A 32-bit edge-triggered D-type flip-flop is built using advanced dual metal CMOS technology. This high-speed, low-power register is ideal for use as a buffer register for data synchronization and storage. The Output Enable ($\overline{OE}$) and clock (CLK) controls are organized to operate the device as four 8-bit registers, two 16-bit registers, or one 32-bit register with common clock. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

All pins of the LVCH32374A can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

The LVCH32374A has been designed with a $\pm 24mA$ output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The LVCH32374A has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

FUNCTIONAL BLOCK DIAGRAM



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INDUSTRIAL TEMPERATURE RANGE

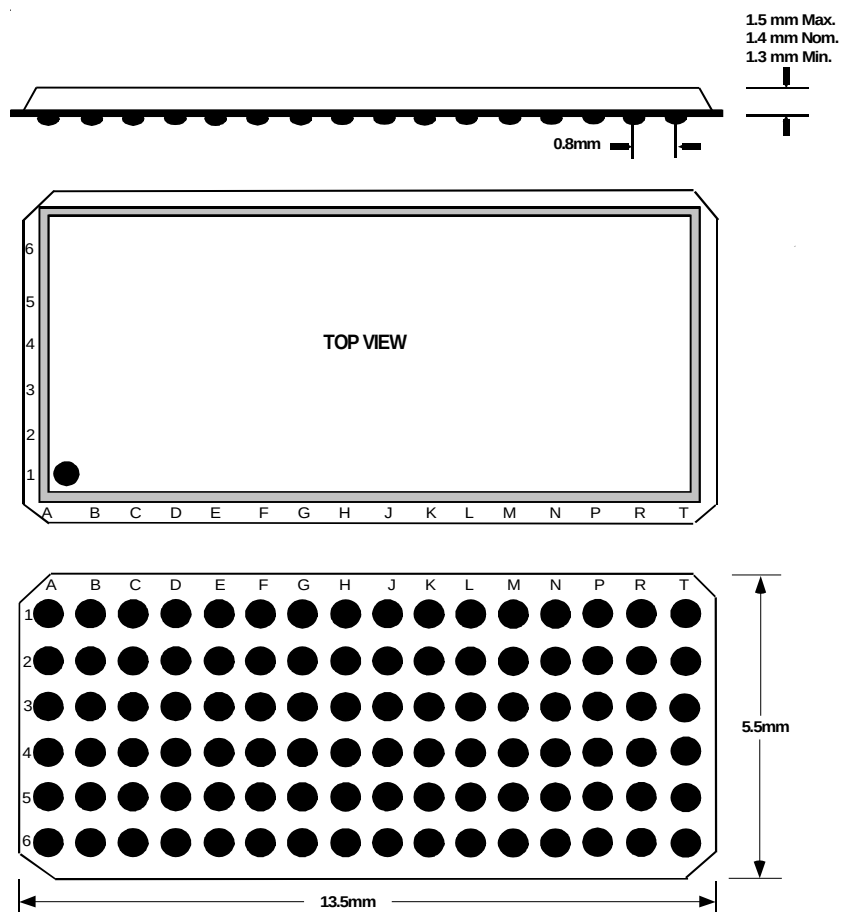
FEBRUARY 2000

PIN CONFIGURATION

6	1D2	1D4	1D6	1D8	2D2	2D4	2D6	2D7	3D2	3D4	3D6	3D8	4D2	4D4	4D6	4D7
5	1D1	1D3	1D5	1D7	2D1	2D3	2D5	2D8	3D1	3D3	3D5	3D7	4D1	4D3	4D5	4D8
4	1CLK	GND	Vcc	GND	GND	Vcc	GND	2CLK	3CLK	GND	Vcc	GND	GND	Vcc	GND	4CLK
3	1 $\overline{OE}$	GND	Vcc	GND	GND	Vcc	GND	2 $\overline{OE}$	3 $\overline{OE}$	GND	Vcc	GND	GND	Vcc	GND	4 $\overline{OE}$
2	1Q1	1Q3	1Q5	1Q7	2Q1	2Q3	2Q5	2Q8	3Q1	3Q3	3Q5	3Q7	4Q1	4Q3	4Q5	4Q8
1	1Q2	1Q4	1Q6	1Q8	2Q2	2Q4	2Q6	2Q7	3Q2	3Q4	3Q6	3Q8	4Q2	4Q4	4Q6	4Q7
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T

LFBGA
TOPVIEW

96 BALL LFBGA PACKAGE ATTRIBUTES



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
V _{TERM}	Terminal Voltage with Respect to GND	−0.5 to +6.5	V
T _{STG}	Storage Temperature	−65 to +150	°C
I _{OUT}	DC Output Current	−50 to +50	mA
I _{IK} I _{OK}	Continuous Clamp Current, V _I < 0 or V _O < 0	−50	mA
I _{CC} I _{SS}	Continuous Current through each V _{CC} or GND	±100	mA

NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	6.5	8	pF
C _{I/O}	I/O Port Capacitance	V _{IN} = 0V	6.5	8	pF

NOTE:

- As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
xD _x	Data Inputs ⁽¹⁾
xCLK	Clock Inputs
$\overline{xOE}$	3-State Output Enable Inputs (Active LOW)
xQ _x	3-State Outputs

NOTE:

- These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

FUNCTION TABLE⁽¹⁾

Function	Inputs			Outputs
	xD _x	xCLK	$\overline{xOE}$	xQ _x
Hi-Z	X	L	H	Z
	X	H	H	Z
Load Register	L	↑	L	L
	H	↑	L	H
	L	↑	H	Z
	H	↑	H	Z

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance
↑ = LOW-to-HIGH Transition

BUS-HOLD CHARACTERISTICS

Symbol	Parameter ⁽¹⁾	Test Conditions		Min.	Typ. ⁽²⁾	Max.	Unit
I _{BHH} I _{BHL}	Bus-Hold Input Sustain Current	V _{CC} = 3V	V _I = 2V	−75	—	—	μA
			V _I = 0.8V	75	—	—	
I _{BHH} I _{BHL}	Bus-Hold Input Sustain Current	V _{CC} = 2.3V	V _I = 1.7V	—	—	—	μA
			V _I = 0.7V	—	—	—	
I _{BHHO} I _{BHLO}	Bus-Hold Input Overdrive Current	V _{CC} = 3.6V	V _I = 0 to 3.6V	—	—	±500	μA

NOTES:

- Pins with Bus-Hold are identified in the pin description.
- Typical values are at V_{CC} = 3.3V, +25°C ambient.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V_{IH}	Input HIGH Voltage Level	$V_{CC} = 2.3\text{V}$ to 2.7V		1.7	—	—	V
		$V_{CC} = 2.7\text{V}$ to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	$V_{CC} = 2.3\text{V}$ to 2.7V		—	—	0.7	V
		$V_{CC} = 2.7\text{V}$ to 3.6V		—	—	0.8	
I_{IH} I_{IL}	Input Leakage Current	$V_{CC} = 3.6\text{V}$	$V_I = 0$ to 5.5V	—	—	± 5	μA
I_{OZH} I_{OZL}	High Impedance Output Current (3-State Output pins)	$V_{CC} = 3.6\text{V}$	$V_O = 0$ to 5.5V	—	—	± 10	μA
I_{OFF}	Input/Output Power Off Leakage	$V_{CC} = 0\text{V}$, V_{IN} or $V_O \leq 5.5\text{V}$		—	—	± 50	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = 2.3\text{V}$, $I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
V_H	Input Hysteresis	$V_{CC} = 3.3\text{V}$		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = 3.6\text{V}$	$V_{IN} = \text{GND}$ or V_{CC}	—	—	10	μA
			$3.6 \leq V_{IN} \leq 5.5\text{V}^{(2)}$	—	—	10	
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at $V_{CC} - 0.6\text{V}$, other inputs at V_{CC} or GND		—	—	500	μA

NOTES:

- Typical values are at $V_{CC} = 3.3\text{V}$, $+25^{\circ}\text{C}$ ambient.
- This applies in the disabled state only.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$V_{CC} = 2.3\text{V}$ to 3.6V	$I_{OH} = -0.1\text{mA}$	$V_{CC} - 0.2$	—	V
		$V_{CC} = 2.3\text{V}$	$I_{OH} = -6\text{mA}$	2	—	
		$V_{CC} = 2.3\text{V}$	$I_{OH} = -12\text{mA}$	1.7	—	
		$V_{CC} = 2.7\text{V}$		2.2	—	
		$V_{CC} = 3\text{V}$		2.4	—	
		$V_{CC} = 3\text{V}$	$I_{OH} = -24\text{mA}$	2.2	—	
V_{OL}	Output LOW Voltage	$V_{CC} = 2.3\text{V}$ to 3.6V	$I_{OL} = 0.1\text{mA}$	—	0.2	V
		$V_{CC} = 2.3\text{V}$	$I_{OL} = 6\text{mA}$	—	0.4	
			$I_{OL} = 12\text{mA}$	—	0.7	
		$V_{CC} = 2.7\text{V}$	$I_{OL} = 12\text{mA}$	—	0.4	
		$V_{CC} = 3\text{V}$	$I_{OL} = 24\text{mA}$	—	0.55	

NOTE:

- V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range.
 $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$.

OPERATING CHARACTERISTICS, $V_{CC} = 3.3V \pm 0.3V$, $T_A = 25^\circ C$

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power Dissipation Capacitance per Register Outputs enabled	$C_L = 0pF$, $f = 10MHz$	116	pF
CPD	Power Dissipation Capacitance per Register Outputs disabled		48	

SWITCHING CHARACTERISTICS⁽¹⁾

Symbol	Parameter	$V_{CC} = 2.7V$		$V_{CC} = 3.3V \pm 0.3V$		Unit
		Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay xCLK to xQx	—	4.9	1.5	4.5	ns
t_{PZH} t_{PZL}	Output Enable Time x $\overline{OE}$ to xQx	—	5.3	1.5	4.6	ns
t_{PHZ} t_{PLZ}	Output Disable Time x $\overline{OE}$ to xQx	—	6.1	1.5	5.5	ns
t_{SU}	Set-up Time HIGH or LOW, xDx to xCLK	1.9	—	1.9	—	ns
t_H	Hold Time HIGH or LOW, xDx after xCLK	1.1	—	1.1	—	ns
t_W	xCLK Pulse Width HIGH or LOW	3.3	—	3.3	—	ns
$t_{SK(0)}$	Output Skew ⁽²⁾	—	—	—	500	ps

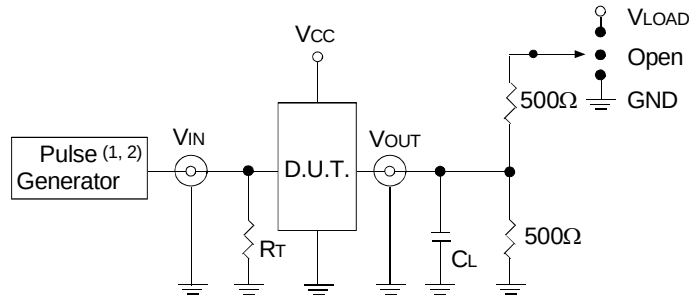
NOTES:

- See TEST CIRCUITS AND WAVEFORMS. $T_A = -40^\circ C$ to $+85^\circ C$.
- Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	V _{CC} ⁽¹⁾ =3.3V±0.3V	V _{CC} ⁽¹⁾ =2.7V	V _{CC} ⁽²⁾ =2.5V±0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF



Test Circuit for All Outputs

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

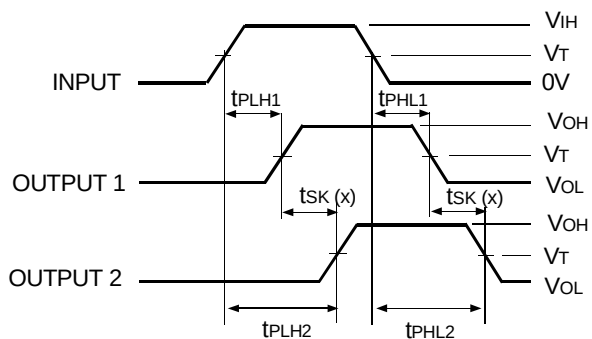
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_r ≤ 2.5ns; t_r ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_r ≤ 2ns; t_r ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other Tests	Open

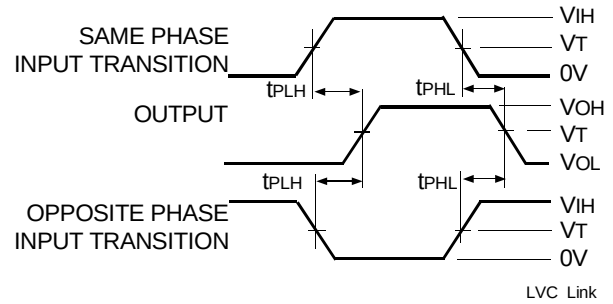


$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

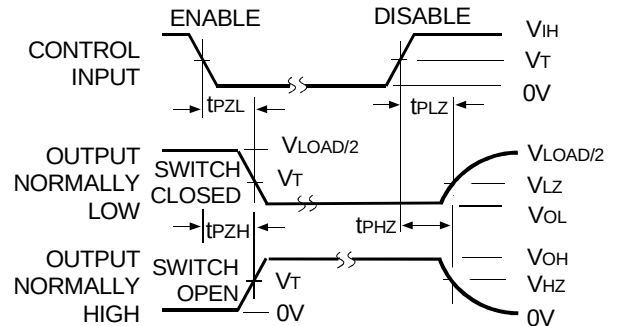
Output Skew - t_{SK(x)}

NOTES:

1. For t_{SK(0)} OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK(b)} OUTPUT1 and OUTPUT2 are in the same bank.



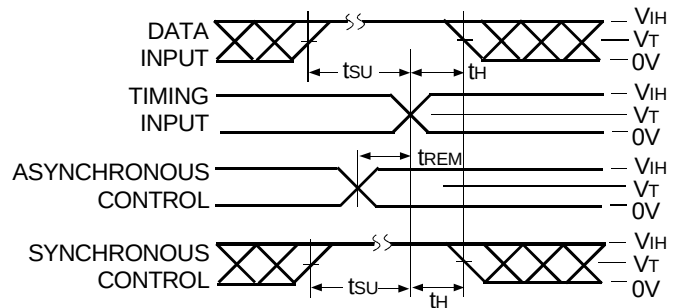
Propagation Delay



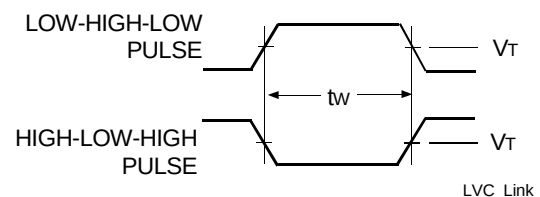
Enable and Disable Times

NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.



Set-up, Hold, and Release Times



Pulse Width

ORDERING INFORMATION

IDT	XX	LVC	X	XX	XXXX	XX	
	Temp. Range		Bus-Hold	Family	Device Type	Package	
						BF	Low-Profile Fine Pitch Ball Grid Array
					374A		32-Bit Edge-Triggered D-Type Flip-Flop with 5V Tolerant I/O
					32		32- Bit Bus Density, $\pm 24\text{mA}$
			H				Bus-hold
						74	-40°C to $+85^{\circ}\text{C}$



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