PRELIMINARY

Integrated Circuit Systems, Inc.

ICS8522

Low Skew, 1-to-17 Differential-to-LVHSTL Fanout Buffer

General Description

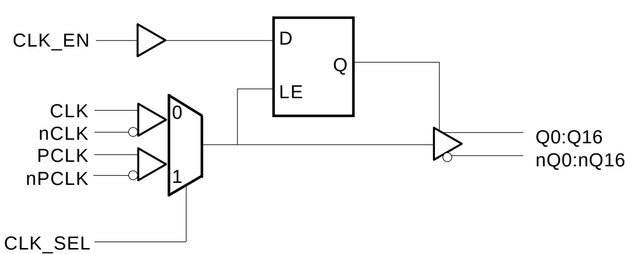
The ICS8522 is a low skew, 1-to-17 Differential-to-LVHSTL Fanout Buffer and a member of the HiPerClockS™ Family of High Performance Clock Solutions from ICS. The ICS8522 has two selectable clock inputs. The CLK, nCLK pair can accept most standard differential input levels. The PCLK, nPCLK pair can accept LVPECL, CML, or SSTL input levels. The clock enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output skew, part-to-part skew and crossover voltage characteristics make the ICS8522 ideal for interfacing to today's most advanced microprocessor and static RAMs.

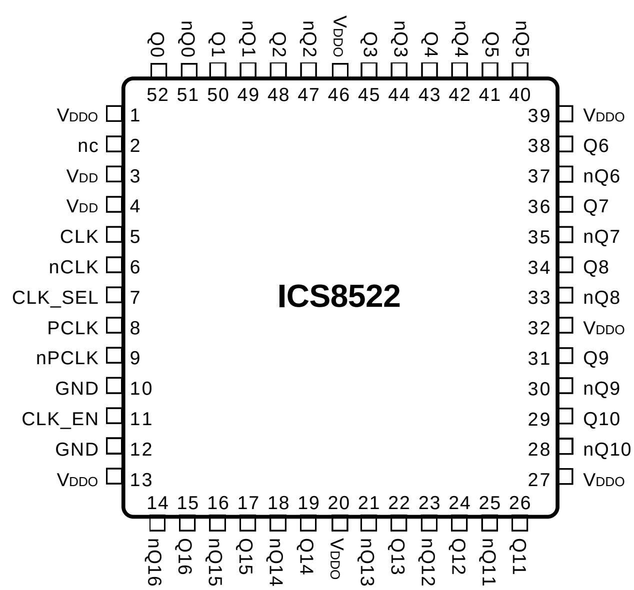
Features

- 17 LVHSTL outputs each with the ability to drive 50Ω to ground
- Selectable differential CLK, nCLK or LVPECL clock inputs
- CLK, nCLK pair can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- PCLK, nPCLK supports the following input types: LVPECL, CML, SSTL
- Maximum output frequency: 500MHz
- Translates any single-ended input signal (LVCMOS, LVTTL, GTL) to LVPECL levels with resistor bias on nCLK input
- Output skew: 50ps (typical)
- Part-to-part skew: 70ps (typical)
- V_{OH} = 1.2V (maximum)
- 3.3V core,1.8V output operating supply voltages
- 0°C to 70°C ambient operating temperature

Block Diagram



Pin Assignment



52-Lead LQFP
10mm x 10mm x 1.4mm body package
Y package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 13, 20, 27, 32, 39, 46	V_{DDO}	Power		Output supply pins.
2	nc	Unused		No connect.
3, 4	V_{DD}	Power		Core supply pins.
5	CLK	Input	Pulldown	Non-inverting differential clock input.
6	nCLK	Input	Pullup	Inverting differential clock input.
7	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK, nCLK inputs. When LOW, selects PCLK, nPCLK inputs. LVCMOS / LVTTL interface levels.
8	PCLK	Input	Pulldown	Non-inverting differential LVPECL clock input.
9	nPCLK	Input	Pullup	Inverting differential LVPECL clock input.
10, 12	GND	Power		Power supply ground.
11	CLK_EN	Input	Pullup	Synchronizing clock enable. When HIGH, clock outputs follows clock input. When LOW, Q outputs are forced low, nQ outputs are forced high. LVCMOS / LVTTL interface levels.
14, 15	nQ16, Q16	Output		Differential clock outputs. LVHSTL interface levels.
16, 17	nQ15, Q15	Output		Differential clock outputs. LVHSTL interface levels.
18, 19	nQ14, Q14	Output		Differential clock outputs. LVHSTL interface levels.
21, 22	nQ13, Q13	Output		Differential clock outputs. LVHSTL interface levels.
23, 24	nQ12, Q12	Output		Differential clock outputs. LVHSTL interface levels.
25, 26	nQ11, Q11	Output		Differential clock outputs. LVHSTL interface levels.
28, 29	nQ10, Q10	Output		Differential clock outputs. LVHSTL interface levels.
30, 31	nQ9, Q9	Output		Differential clock outputs. LVHSTL interface levels.
33, 34	nQ8, Q8	Output		Differential clock outputs. LVHSTL interface levels.
35, 36	nQ7, Q7	Output		Differential clock outputs. LVHSTL interface levels.
37, 38	nQ6, Q6	Output		Differential clock outputs. LVHSTL interface levels.
40, 41	nQ5, Q5	Output		Differential clock outputs. LVHSTL interface levels.
42, 43	nQ4, Q4	Output		Differential clock outputs. LVHSTL interface levels.
44, 45	nQ3, Q3	Output		Differential clock outputs. LVHSTL interface levels.
47, 48	nQ2, Q2	Output		Differential clock outputs. LVHSTL interface levels.
49, 50	nQ1, Q1	Output		Differential clock outputs. LVHSTL interface levels.
51, 52	nQ0, Q0	Output		Differential clock outputs. LVHSTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.
NOTE: Unused output pairs must be terminated.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4	pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ

TABLE 3A. CONTROL INPUT FUNCTION TABLE

Inputs			Outputs	
CLK_EN	**CLK_SEL**	**Selected Source**	**Q0:Q16**	**nQ0:nQ16**
0	X		LOW	HIGH
1	0	CLK, nCLK	CLK	CLK
1	1	PCLK, nPCLK	PCLK	PCLK

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in *Figure 1.*
In the active mode the state of the outputs are a function of the CLK, nCLK and PCLK, nPCLK inputs as described in Table 3B.

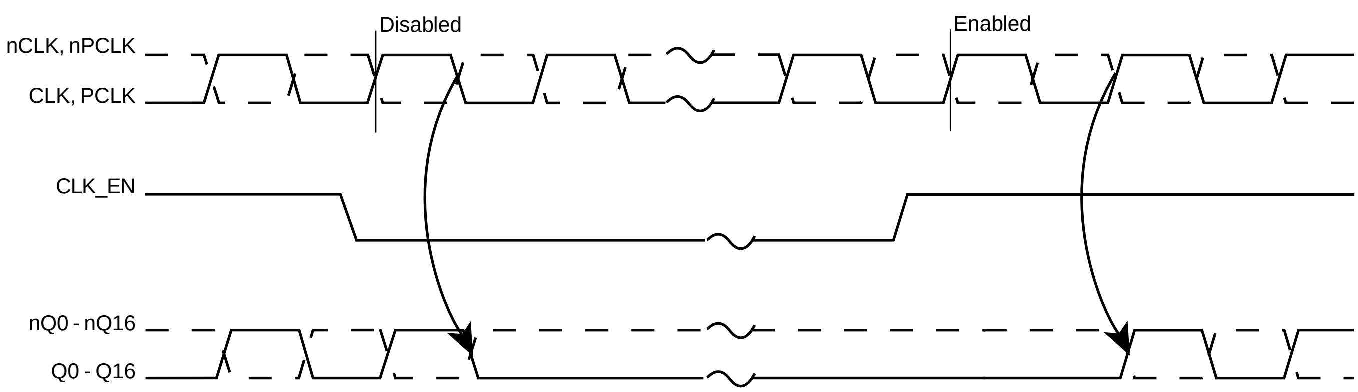


FIGURE 1. CLK_EN TIMING DIAGRAM

TABLE 3B. CLOCK INPUT FUNCTION TABLE

Inputs		Outputs		Input to Output Mode	Polarity
CLK or PCLK	**nCLK or nPCLK**	**Q0:Q16**	**nQ0:nQ16**		
0	0	LOW	HIGH	Differential to Differential	Non Inverting
1	1	HIGH	LOW	Differential to Differential	Non Inverting
0	Biased; NOTE 1	LOW	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	HIGH	LOW	Single Ended to Differential	Non Inverting
Biased; NOTE 1	0	HIGH	LOW	Single Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single Ended to Differential	Inverting

NOTE 1: Please refer to the Application Information section, "Wiring the Differential Input to Accept Single Ended Levels".

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	42.3°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 1.8V±10%, TA=0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Ouptut Power Supply Voltage		1.6	1.8	2.0	V
I_{DD}	Power Supply Current			152	200	mA
I_{DDO}	Output Supply Current			420		mA

TABLE 4B. LVCMOS / LVTTL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 1.8V±10%, TA=0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	CLK_EN				5	µA
		CLK_SEL				150	µA
I_{IL}	Input Low Current	CLK_EN		-150			µA
		CLK_SEL		-5			µA

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 1.8V±10%, TA=0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		nCLK	$V_{DD} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	CLK	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		nCLK	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for CLK and nCLK is V_{DD} + 0.3V.

TABLE 4D. LVPECL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 1.8V±10%, TA=0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		nPCLK	$V_{DD} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	PCLK	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		nPCLK	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.3		1	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 1.5		V_{DD}	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for PCLK and nPCLK is V_{DD} + 0.3V.

TABLE 4E. LVHSTL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 1.8V±10%, TA=0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage NOTE 1		1.0		1.2	V
V_{OL}	Output Low Voltage; NOTE 1		0		0.4	V
V_{OX}	Output Crossover Voltage		40% x (V_{OH}-V_{OL}) + V_{OL}	0.73	60% x (V_{OH}-V_{OL}) + V_{OL}	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.1	V

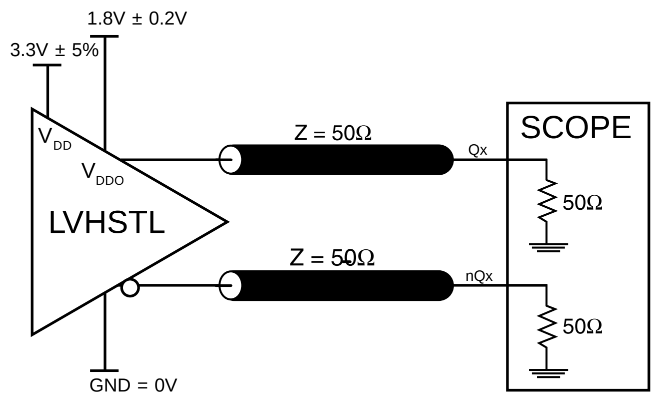
NOTE 1: Outputs terminated with 50Ω to ground.

TABLE 5. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 1.8V±10%, TA=0°C TO 70°C

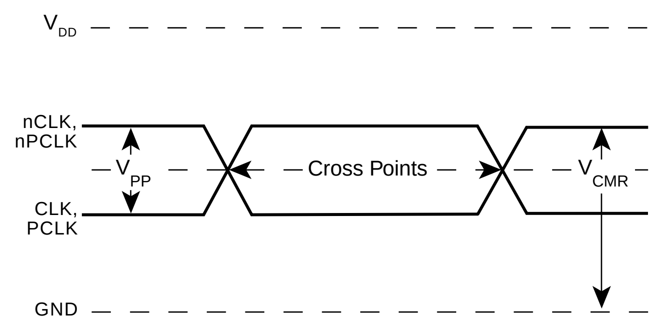
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				500	MHz
tp_{LH}	Propagation Delay, Low-to-High; NOTE 1	f ≤ 500MHz		2.5		ns
tp_{HL}	Propagation Delay, High-to-Low; NOTE 1	f ≤ 500MHz		2.5		ns
*t*sk(o)	Output Skew; NOTE 2, 4			50		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4			70		ps
t_R	Output Rise Time	20% to 80%		530		ps
t_F	Output Fall Time	20% to 80%		530		ps
odc	Output Duty Cycle			50		%

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions at the same temperature. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

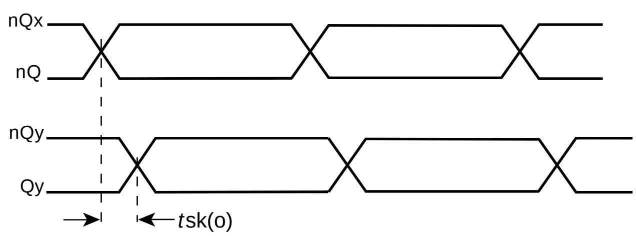
PARAMETER MEASUREMENT INFORMATION



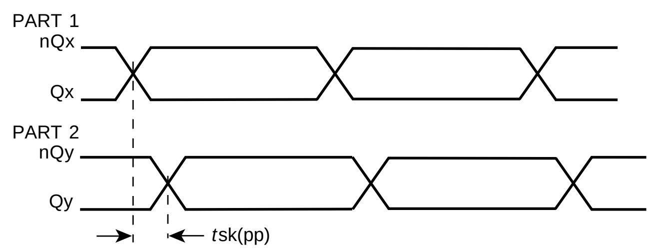
3.3V CORE/1.8V OUTPUT LOAD AC TEST CIRCUIT



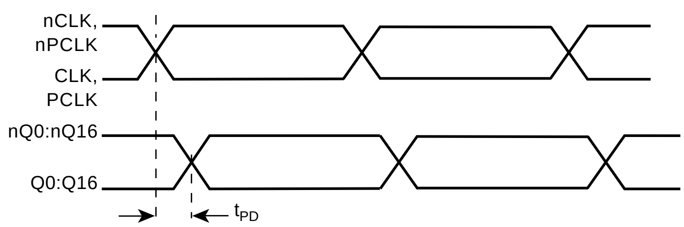
DIFFERENTIAL INPUT LEVEL



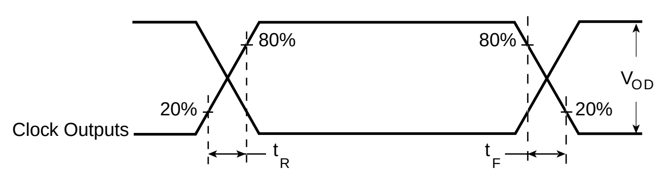
OUTPUT SKEW



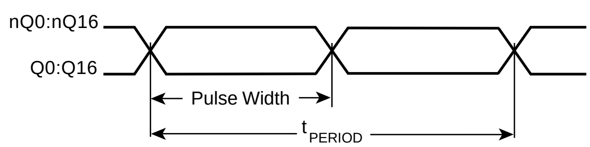
PART-TO-PART SKEW



PROPAGATION DELAY



OUTPUT RISE/FALL TIME



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

odc & t_{PERIOD}

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = $V_{DD}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

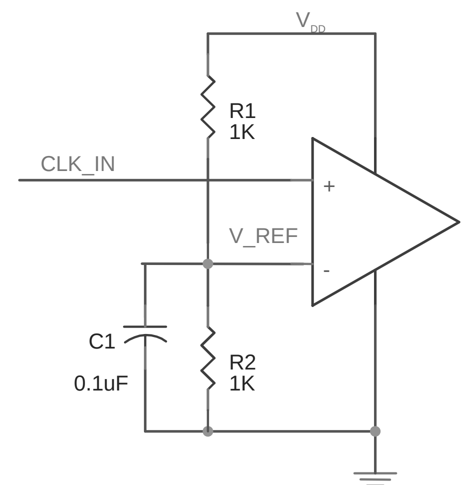


FIGURE 2. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS8522.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS8522 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{DD_MAX} * I_{DD_MAX} = 3.465V * 200mA = **693mW**
- Power (outputs)$_{MAX}$ = **32.8mW/Loaded Output pair**
  If all outputs are loaded, the total power is 17 * 32.8mW = **557.6mW**

Total Power $_{\_MAX}$ (3.465V, with all outputs switching) = 693mW + 557.6mW = **1250.6mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 36.4°C/W per Table 6 below.
Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 1.25W * 36.4°C/W = 115.5°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 52-PIN LQFP, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	58.0°C/W	47.1°C/W	42.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	42.3°C/W	36.4°C/W	34.0°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVHSTL output driver circuit and termination are shown in *Figure 3.*

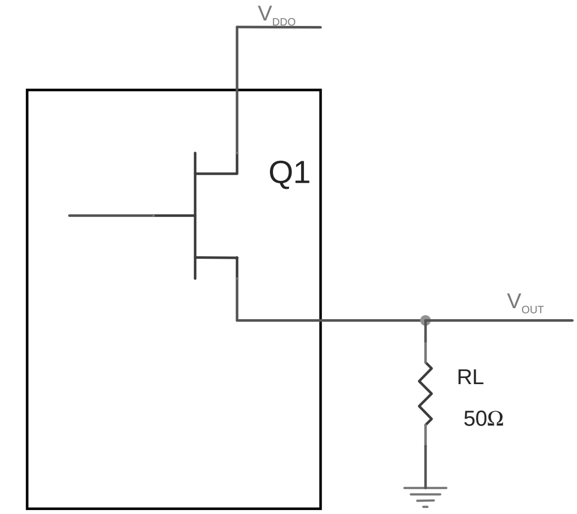


FIGURE 3. LVHSTL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load.

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$$Pd\_H = (V_{OH\_MIN}/R_L) * (V_{DDO\_MAX} - V_{OH\_MIN})$$

$$Pd\_L = (V_{OL\_MAX}/R_L) * (V_{DDO\_MAX} - V_{OL\_MAX})$$

Pd_H = (1V/50Ω) * (2V - 1V) = **20mW**
Pd_L = (0.4V/50Ω) * (2V - 0.4V) = **12.8mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **32.8mW**

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE

θ_{JA} by Velocity (Linear Feet per Minute)

	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	58.0°C/W	47.1°C/W	42.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	42.3°C/W	36.4°C/W	34.0°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS8522 is: 1986

PACKAGE OUTLINE - Y SUFFIX

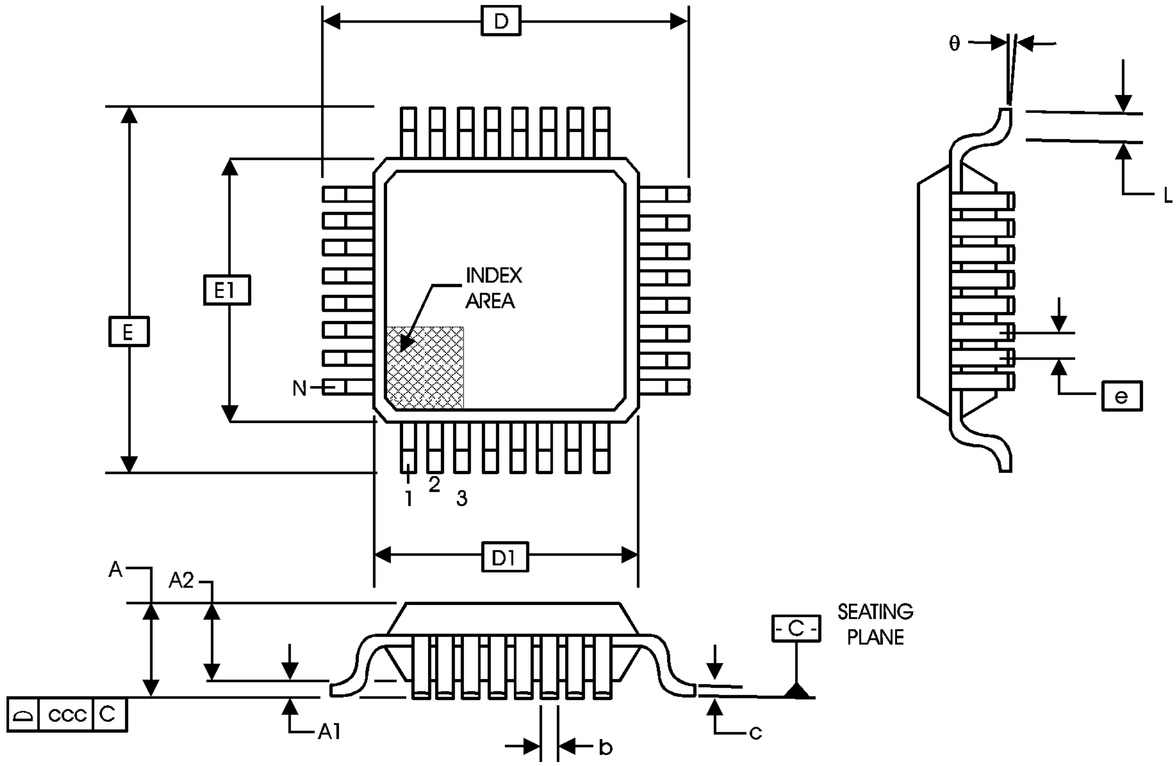


TABLE 8. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BCC		
	MINIMUM	NOMINAL	MAXIMUM
N	52		
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.22	0.32	0.38
c	0.09	--	0.20
D	12.00 BASIC		
D1	10.00 BASIC		
E	12.00 BASIC		
E1	10.00 BASIC		
e	0.65 BASIC		
L	0.45	--	0.75
θ	0°	--	7°
ccc	--	--	0.08

Reference Document: JEDEC Publication 95, MS-026

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8522CY	ICS8522CY	52 lead LQFP	160 per tray	0°C to 70°C
ICS8522CYT	ICS8522CY	52 lead LQFP on Tape and Reel	500	0°C to 70°C