

November 1996

### Features

- Independently Drives 4 N-Channel FET in Half Bridge or Full Bridge Configurations
- Bootstrap Supply Max Voltage to 95V<sub>DC</sub>
- Drives 1000pF Load at 1MHz in Free Air at 50°C with Rise and Fall Times of Typically 10ns
- User-Programmable Dead Time
- On-Chip Charge-Pump and Bootstrap Upper Bias Supplies
- DIS (Disable) Overrides Input Control
- Input Logic Thresholds Compatible with 5V to 15V Logic Levels
- Very Low Power Consumption
- Undervoltage Protection

### Applications

- Medium/Large Voice Coil Motors
- Full Bridge Power Supplies
- Class D Audio Power Amplifiers
- High Performance Motor Controls
- Noise Cancellation Systems
- Battery Powered Vehicles
- Peripherals
- U.P.S.

### Description

The HIP4081A is a high frequency, medium voltage Full Bridge N-Channel FET driver IC, available in 20 lead plastic SOIC and DIP packages. The HIP4081A can drive every possible switch combination except those which would cause a shoot-through condition. The HIP4081A can switch at frequencies up to 1MHz and is well suited to driving Voice Coil Motors, high-frequency Class D audio amplifiers, and power supplies.

For example, the HIP4081A can drive medium voltage brush motors, and two HIP4081As can be used to drive high performance stepper motors, since the short minimum "on-time" can provide fine micro-stepping capability.

Short propagation delays of approximately 55ns maximizes control loop crossover frequencies and dead-times which can be adjusted to near zero to minimize distortion, resulting in rapid, precise control of the driven load.

A similar part, the HIP4080A, includes an on-chip input comparator to create a PWM signal from an external triangle wave and to facilitate "hysteresis mode" switching.

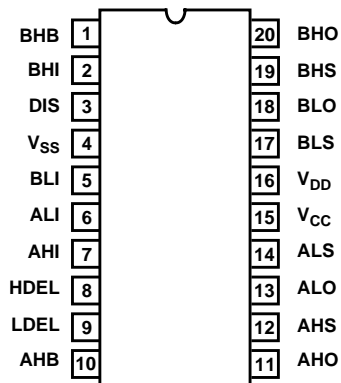
The Application Note for the HIP4081A is the AN9405.

### Ordering Information

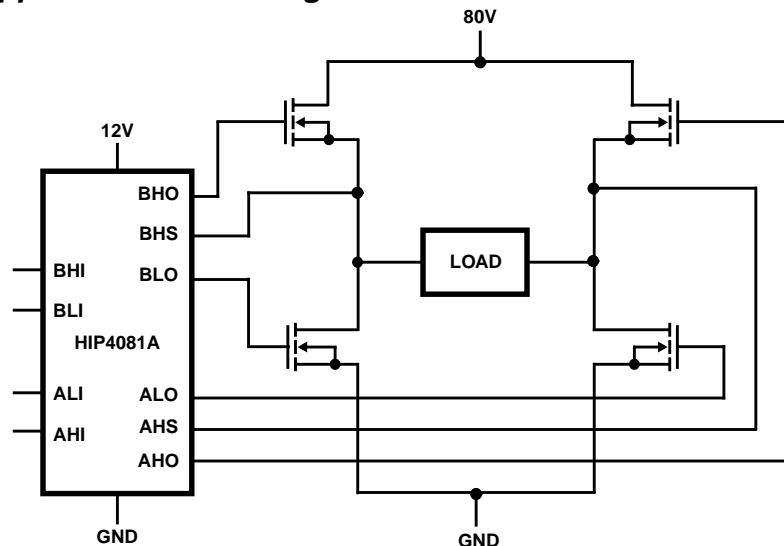
PART NUMBER	TEMP RANGE (°C)	PACKAGE	PKG. NO.
HIP4081AIP	-40 to 85	20 Ld PDIP	E20.3
HIP4081AIB	-40 to 85	20 Ld SOIC (W)	M20.3

### Pinout

HIP4081A (PDIP, SOIC)  
TOP VIEW

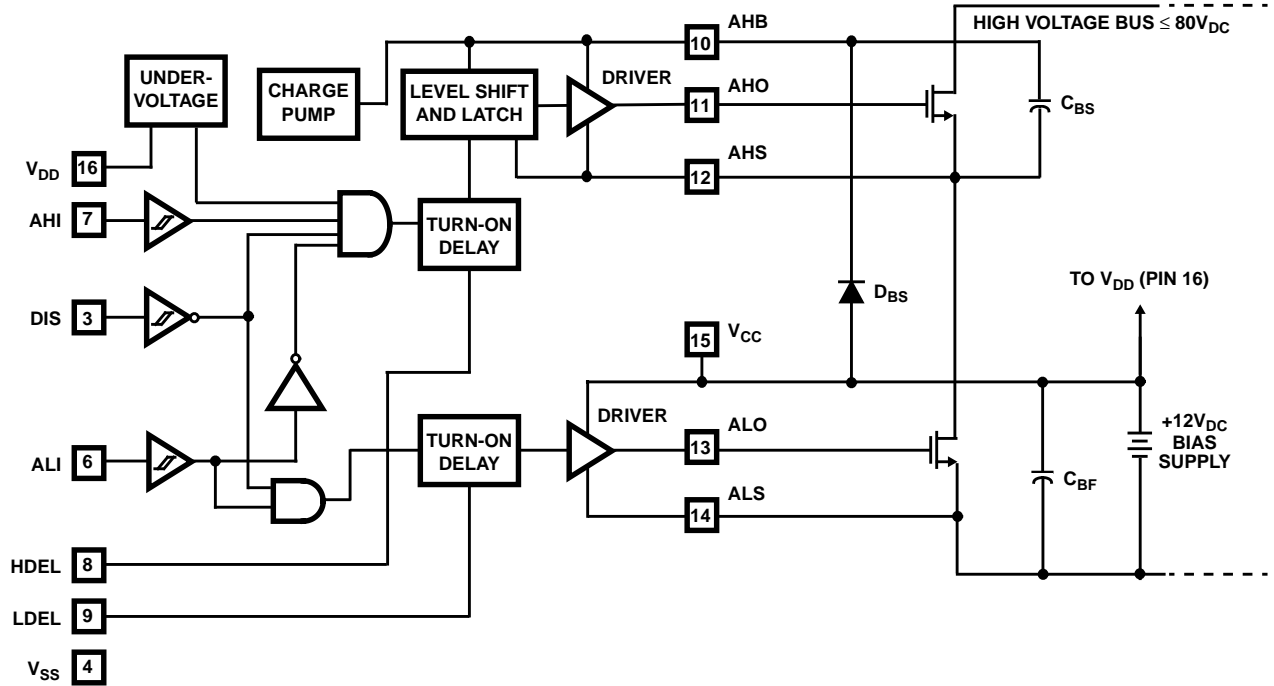


### Application Block Diagram

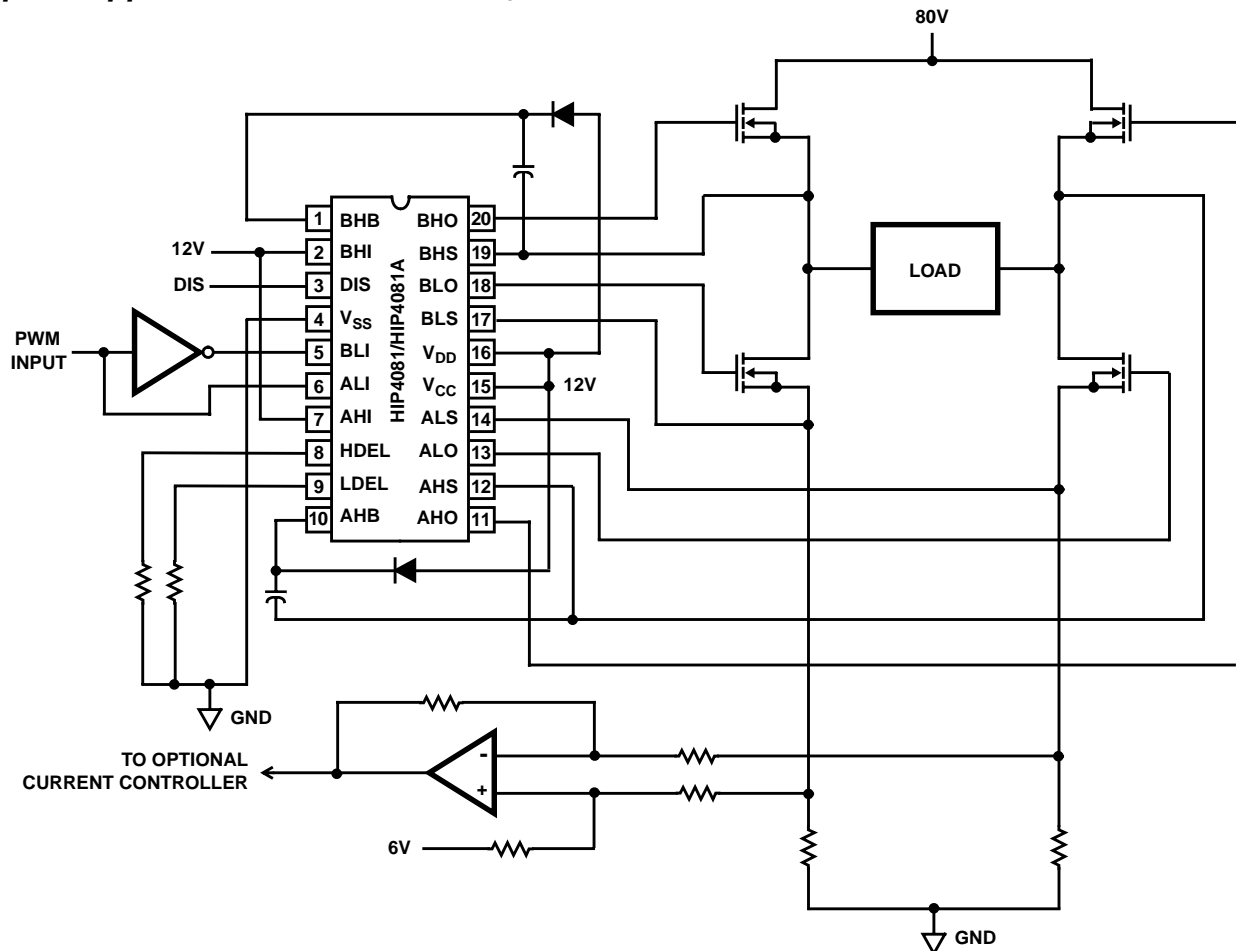


# HIP4081A

## Functional Block Diagram (1/2 HIP4081A)



## Typical Application (PWM Mode Switching)



# HIP4081A

## Absolute Maximum Ratings

Supply Voltage,  $V_{DD}$  and  $V_{CC}$  ..... -0.3V to 16V  
 Logic I/O Voltages ..... -0.3V to  $V_{DD} + 0.3V$   
 Voltage on AHS, BHS ..... -6.0V (Transient) to 80V (25°C to 125°C)  
 Voltage on AHS, BHS ..... -6.0V (Transient) to 70V (-55°C to 125°C)  
 Voltage on ALS, BLS ..... -2.0V (Transient) to +2.0V (Transient)  
 Voltage on AHB, BHB .....  $V_{AHS, BHS} - 0.3V$  to  $V_{AHS, BHS} + V_{DD}$   
 Voltage on ALO, BLO .....  $V_{ALS, BLS} - 0.3V$  to  $V_{CC} + 0.3V$   
 Voltage on AHO, BHO .....  $V_{AHS, BHS} - 0.3V$  to  $V_{AHB, BHB} + 0.3V$   
 Input Current, HDEL and LDEL ..... -5mA to 0mA  
 Phase Slew Rate ..... 20V/ns

NOTE: All Voltages relative to  $V_{SS}$ , unless otherwise specified.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1.  $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

## Thermal Information

Thermal Resistance (Typical, Note 1)  $\theta_{JA}$  (°C/W)  
 SOIC Package ..... 85  
 DIP Package ..... 75  
 Storage Temperature Range ..... -65°C to 150°C  
 Operating Max. Junction Temperature ..... 125°C  
 Lead Temperature (Soldering 10s) ..... 300°C  
 (For SOIC - Lead Tips Only)

## Operating Conditions

Supply Voltage,  $V_{DD}$  and  $V_{CC}$  ..... +9.5V to +15V  
 Voltage on ALS, BLS ..... -1.0V to +1.0V  
 Voltage on AHB, BHB .....  $V_{AHS, BHS} + 5V$  to  $V_{AHS, BHS} + 15V$   
 Input Current, HDEL and LDEL ..... -500µA to -50µA  
 Operating Ambient Temperature Range ..... -40°C to 85°C

## Electrical Specifications

$V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$ ,  $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$ ,  $R_{HDEL} = R_{LDEL} = 100K$  and  $T_A = 25^\circ C$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	$T_J = 25^\circ C$			$T_{JS} = -40^\circ C$ TO $125^\circ C$		UNITS
			MIN	TYP	MAX	MIN	MAX	
<b>SUPPLY CURRENTS AND CHARGE PUMPS</b>								
$V_{DD}$ Quiescent Current	$I_{DD}$	All inputs = 0V	8.5	10.5	14.5	7.5	14.5	mA
$V_{DD}$ Operating Current	$I_{DDO}$	Outputs switching $f = 500kHz$	9.5	12.5	15.5	8.5	15.5	mA
$V_{CC}$ Quiescent Current	$I_{CC}$	All Inputs = 0V, $I_{ALO} = I_{BLO} = 0$	-	0.1	10	-	20	µA
$V_{CC}$ Operating Current	$I_{CCO}$	$f = 500kHz$ , No Load	1	1.25	2.0	0.8	3	mA
AHB, BHB Quiescent Current - Qpump Output Current	$I_{AHB}, I_{BHB}$	All Inputs = 0V, $I_{AHO} = I_{BHO} = 0$ $V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 10V$	-50	-30	-11	-60	-10	µA
AHB, BHB Operating Current	$I_{AHBO}, I_{BHBO}$	$f = 500kHz$ , No Load	0.6	1.2	1.5	0.5	1.9	mA
AHS, BHS, AHB, BHB Leakage Current	$I_{HLK}$	$V_{BHS} = V_{AHS} = 80V$ , $V_{AHB} = V_{BHB} = 93V$	-	0.02	1.0	-	10	µA
AHB-AHS, BHB-BHS Qpump Output Voltage	$V_{AHB-V_{AHS}}$ $V_{BHB-V_{BHS}}$	$I_{AHB} = I_{AHS} = 0$ , No Load	11.5	12.6	14.0	10.5	14.5	V
<b>INPUT PINS: ALI, BLI, AHI, BHI, AND DIS</b>								
Low Level Input Voltage	$V_{IL}$	Full Operating Conditions	-	-	1.0	-	0.8	V
High Level Input Voltage	$V_{IH}$	Full Operating Conditions	2.5	-	-	2.7	-	V
Input Voltage Hysteresis			-	35	-	-	-	mV
Low Level Input Current	$I_{IL}$	$V_{IN} = 0V$ , Full Operating Conditions	-130	-100	-75	-135	-65	µA
High Level Input Current	$I_{IH}$	$V_{IN} = 5V$ , Full Operating Conditions	-1	-	+1	-10	+10	µA
<b>TURN-ON DELAY PINS: LDEL AND HDEL</b>								
LDEL, HDEL Voltage	$V_{HDEL}, V_{LDEL}$	$I_{HDEL} = I_{LDEL} = -100\mu A$	4.9	5.1	5.3	4.8	5.4	V
<b>GATE DRIVER OUTPUT PINS: ALO, BLO, AHO, AND BHO</b>								
Low Level Output Voltage	$V_{OL}$	$I_{OUT} = 100mA$	0.7	0.85	1.0	0.5	1.1	V
High Level Output Voltage	$V_{CC-V_{OH}}$	$I_{OUT} = -100mA$	0.8	0.95	1.1	0.5	1.2	V
Peak Pullup Current	$I_{O+}$	$V_{OUT} = 0V$	1.7	2.6	3.8	1.4	4.1	A
Peak Pulldown Current	$I_{O-}$	$V_{OUT} = 12V$	1.7	2.4	3.3	1.3	3.6	A

# HIP4081A

**Electrical Specifications**  $V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$ ,  $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$ ,  $R_{HDEL} = R_{LDEL} = 100K$  and  $T_A = 25^\circ C$ , Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	$T_J = 25^\circ C$			$T_{JS} = -40^\circ C$ TO $125^\circ C$		UNITS
			MIN	TYP	MAX	MIN	MAX	
Undervoltage, Rising Threshold	UV+		8.1	8.8	9.4	8.0	9.5	V
Undervoltage, Falling Threshold	UV-		7.6	8.3	8.9	7.5	9.0	V
Undervoltage, Hysteresis	HYS		0.25	0.4	0.65	0.2	0.7	V

**Switching Specifications**  $V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$ ,  $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$ ,  $R_{HDEL} = R_{LDEL} = 10K$ ,  $C_L = 1000pF$ .

PARAMETER	SYMBOL	TEST CONDITIONS	$T_J = 25^\circ C$			$T_{JS} = -40^\circ C$ TO $125^\circ C$		UNITS
			MIN	TYP	MAX	MIN	MAX	
Lower Turn-off Propagation Delay (ALI-ALO, BLI-BLO)	$T_{LPHL}$		-	30	60	-	80	ns
Upper Turn-off Propagation Delay (AHI-AHO, BHI-BHO)	$T_{HPHL}$		-	35	70	-	90	ns
Lower Turn-on Propagation Delay (ALI-ALO, BLI-BLO)	$T_{LPLH}$	$R_{HDEL} = R_{LDEL} = 10K$	-	45	70	-	90	ns
Upper Turn-on Propagation Delay (AHI-AHO, BHI-BHO)	$T_{HPLH}$	$R_{HDEL} = R_{LDEL} = 10K$	-	60	90	-	110	ns
Rise Time	$T_R$		-	10	25	-	35	ns
Fall Time	$T_F$		-	10	25	-	35	ns
Turn-on Input Pulse Width	$T_{PWIN-ON}$	$R_{HDEL} = R_{LDEL} = 10K$	50	-	-	50	-	ns
Turn-off Input Pulse Width	$T_{PWIN-OFF}$	$R_{HDEL} = R_{LDEL} = 10K$	40	-	-	40	-	ns
Turn-on Output Pulse Width	$T_{PWOUT-ON}$	$R_{HDEL} = R_{LDEL} = 10K$	40	-	-	40	-	ns
Turn-off Output Pulse Width	$T_{PWOUT-OFF}$	$R_{HDEL} = R_{LDEL} = 10K$	30	-	-	30	-	ns
Disable Turn-off Propagation Delay (DIS - Lower Outputs)	$T_{DISLOW}$		-	45	75	-	95	ns
Disable Turn-off Propagation Delay (DIS - Upper Outputs)	$T_{DISHIGH}$		-	55	85	-	105	ns
Disable to Lower Turn-on Propagation Delay (DIS - ALO and BLO)	$T_{DLPLH}$		-	40	70	-	90	ns
Refresh Pulse Width (ALO and BLO)	$T_{REF-PW}$		240	410	550	200	600	ns
Disable to Upper Enable (DIS - AHO and BHO)	$T_{UEN}$		-	450	620	-	690	ns

## TRUTH TABLE

INPUT				OUTPUT	
ALI, BLI	AHI, BHI	U/V	DIS	ALO, BLO	AHO, BHO
X	X	X	1	0	0
1	X	0	0	1	0
0	1	0	0	0	1
0	0	0	0	0	0
X	X	1	X	0	0

NOTE: X signifies that input can be either a "1" or "0".

## HIP4081A

### Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	BHB	B High-side Bootstrap supply. External bootstrap diode and capacitor are required. Connect cathode of bootstrap diode and positive side of bootstrap capacitor to this pin. Internal charge pump supplies 30 $\mu$ A out of this pin to maintain bootstrap supply. Internal circuitry clamps the bootstrap supply to approximately 12.8V.
2	BHI	B High-side Input. Logic level input that controls BHO driver (Pin 20). BLI (Pin 5) high level input overrides BHI high level input to prevent half-bridge shoot-through, see Truth Table. DIS (Pin 3) high level input overrides BHI high level input. The pin can be driven by signal levels of 0V to 15V (no greater than $V_{DD}$ ). An internal 100 $\mu$ A pull-up to $V_{DD}$ will hold BHI high, so no connection is required if high-side and low-side outputs are to be controlled by the low-side input.
3	DIS	DISable input. Logic level input that when taken high sets all four outputs low. DIS high overrides all other inputs. When DIS is taken low the outputs are controlled by the other inputs. The pin can be driven by signal levels of 0V to 15V (no greater than $V_{DD}$ ). An internal 100 $\mu$ A pull-up to $V_{DD}$ will hold DIS high if this pin is not driven.
4	$V_{SS}$	Chip negative supply, generally will be ground.
5	BLI	B Low-side Input. Logic level input that controls BLO driver (Pin 18). If BHI (Pin 2) is driven high or not connected externally then BLI controls both BLO and BHO drivers, with dead time set by delay currents at HDEL and LDEL (Pin 8 and 9). DIS (Pin 3) high level input overrides BLI high level input. The pin can be driven by signal levels of 0V to 15V (no greater than $V_{DD}$ ). An internal 100 $\mu$ A pull-up to $V_{DD}$ will hold BLI high if this pin is not driven.
6	ALI	A Low-side Input. Logic level input that controls ALO driver (Pin 13). If AHI (Pin 7) is driven high or not connected externally then ALI controls both ALO and AHO drivers, with dead time set by delay currents at HDEL and LDEL (Pin 8 and 9). DIS (Pin 3) high level input overrides ALI high level input. The pin can be driven by signal levels of 0V to 15V (no greater than $V_{DD}$ ). An internal 100 $\mu$ A pull-up to $V_{DD}$ will hold ALI high if this pin is not driven.
7	AHI	A High-side Input. Logic level input that controls AHO driver (Pin 11). ALI (Pin 6) high level input overrides AHI high level input to prevent half-bridge shoot-through, see Truth Table. DIS (Pin 3) high level input overrides AHI high level input. The pin can be driven by signal levels of 0V to 15V (no greater than $V_{DD}$ ). An internal 100 $\mu$ A pull-up to $V_{DD}$ will hold AHI high, so no connection is required if high-side and low-side outputs are to be controlled by the low-side input.
8	HDEL	High-side turn-on DELay. Connect resistor from this pin to $V_{SS}$ to set timing current that defines the turn-on delay of both high-side drivers. The low-side drivers turn-off with no adjustable delay, so the HDEL resistor guarantees no shoot-through by delaying the turn-on of the high-side drivers. HDEL reference voltage is approximately 5.1V.
9	LDEL	Low-side turn-on DELay. Connect resistor from this pin to $V_{SS}$ to set timing current that defines the turn-on delay of both low-side drivers. The high-side drivers turn-off with no adjustable delay, so the LDEL resistor guarantees no shoot-through by delaying the turn-on of the low-side drivers. LDEL reference voltage is approximately 5.1V.
10	AHB	A High-side Bootstrap supply. External bootstrap diode and capacitor are required. Connect cathode of bootstrap diode and positive side of bootstrap capacitor to this pin. Internal charge pump supplies 30 $\mu$ A out of this pin to maintain bootstrap supply. Internal circuitry clamps the bootstrap supply to approximately 12.8V.
11	AHO	A High-side Output. Connect to gate of A High-side power MOSFET.
12	AHS	A High-side Source connection. Connect to source of A High-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
13	ALO	A Low-side Output. Connect to gate of A Low-side power MOSFET.
14	ALS	A Low-side Source connection. Connect to source of A Low-side power MOSFET.
15	$V_{CC}$	Positive supply to gate drivers. Must be same potential as $V_{DD}$ (Pin 16). Connect to anodes of two bootstrap diodes.
16	$V_{DD}$	Positive supply to lower gate drivers. Must be same potential as $V_{CC}$ (Pin 15). De-couple this pin to $V_{SS}$ (Pin 4).
17	BLS	B Low-side Source connection. Connect to source of B Low-side power MOSFET.
18	BLO	B Low-side Output. Connect to gate of B Low-side power MOSFET.
19	BHS	B High-side Source connection. Connect to source of B High-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
20	BHO	B High-side Output. Connect to gate of B High-side power MOSFET.

Timing Diagrams

X = A OR B, A AND B HALVES OF BRIDGE CONTROLLER ARE INDEPENDENT

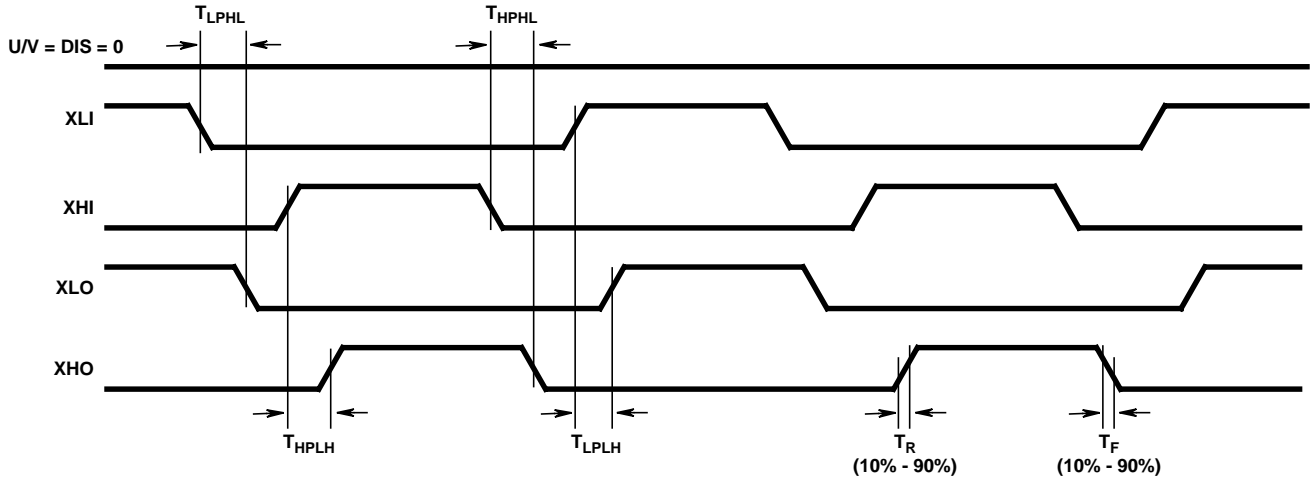


FIGURE 1. INDEPENDENT MODE

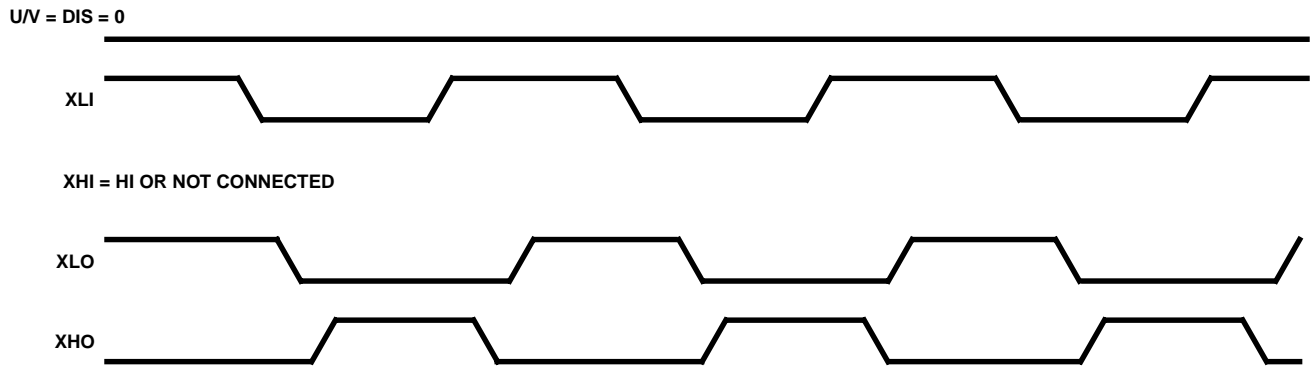


FIGURE 2. BISTATE MODE

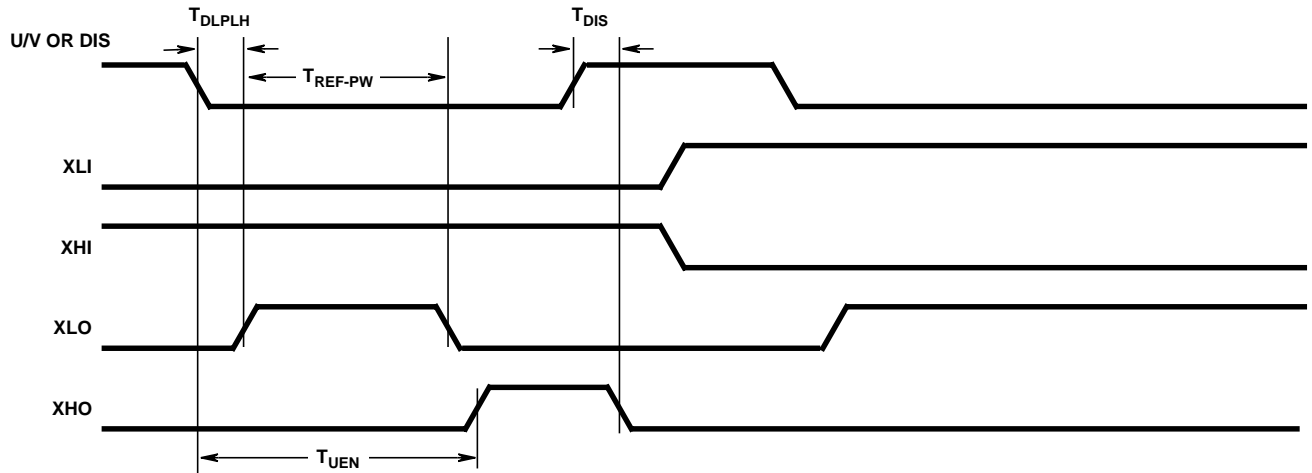


FIGURE 3. DISABLE FUNCTION

# HIP4081A

**Typical Performance Curves**  $V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$ ,  $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$ ,  $R_{HDEL} = R_{LDEL} = 100K$  and  $T_A = 25^\circ C$ , Unless Otherwise Specified

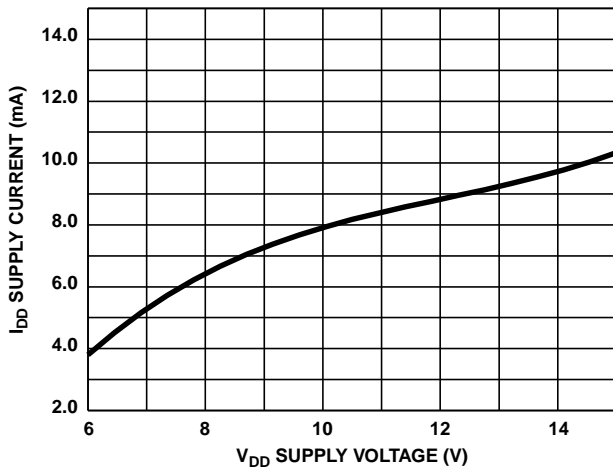


FIGURE 4. QUIESCENT I<sub>DD</sub> SUPPLY CURRENT vs V<sub>DD</sub> SUPPLY VOLTAGE

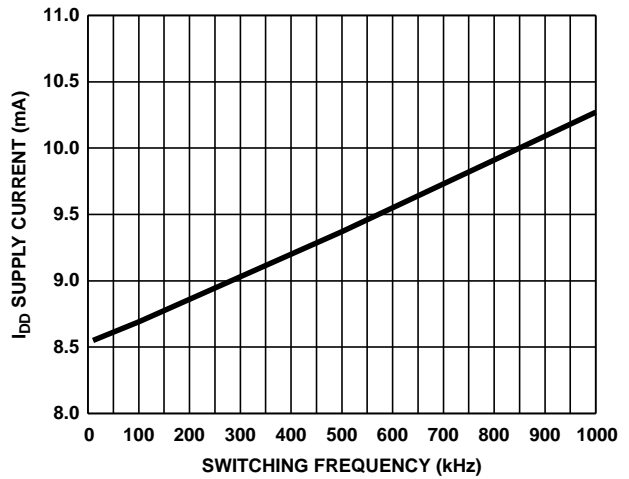


FIGURE 5. I<sub>DD0</sub>, NO-LOAD I<sub>DD</sub> SUPPLY CURRENT vs FREQUENCY (kHz)

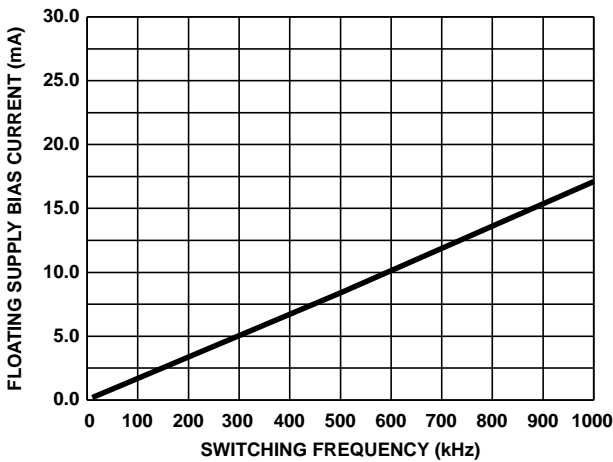


FIGURE 6. SIDE A, B FLOATING SUPPLY BIAS CURRENT vs FREQUENCY (LOAD = 1000pF)

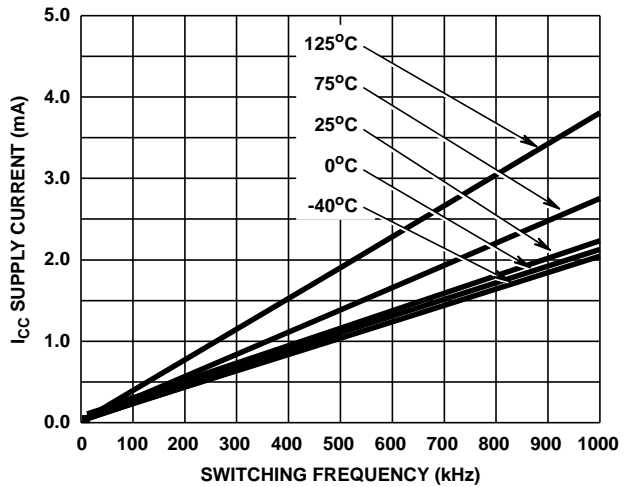


FIGURE 7. I<sub>CC0</sub>, NO-LOAD I<sub>CC</sub> SUPPLY CURRENT vs FREQUENCY (kHz) TEMPERATURE

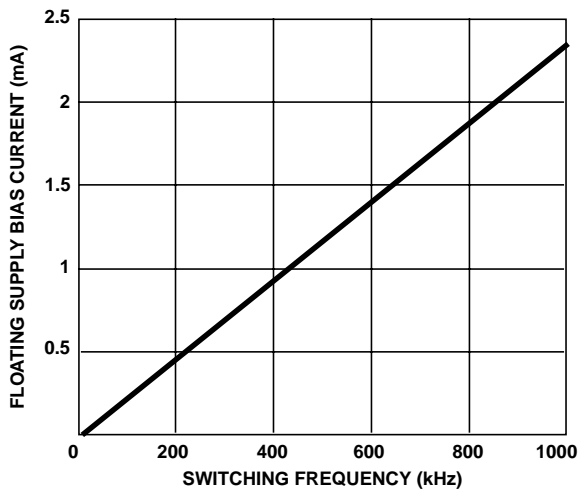


FIGURE 8. I<sub>AHB</sub>, I<sub>BHB</sub>, NO-LOAD FLOATING SUPPLY BIAS CURRENT vs FREQUENCY

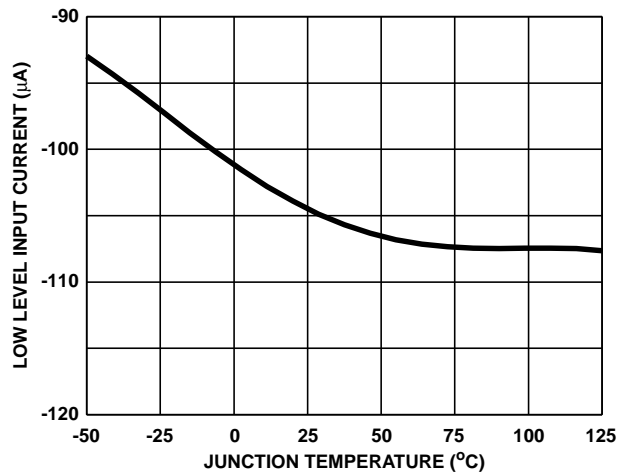


FIGURE 9. ALI, BLI, AHI, BHI LOW LEVEL INPUT CURRENT I<sub>IL</sub> vs TEMPERATURE

# HIP4081A

**Typical Performance Curves**  $V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$ ,  $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$ ,  $R_{HDEL} = R_{LDEL} = 10K$  and  $T_A = 25^{\circ}C$ , Unless Otherwise Specified

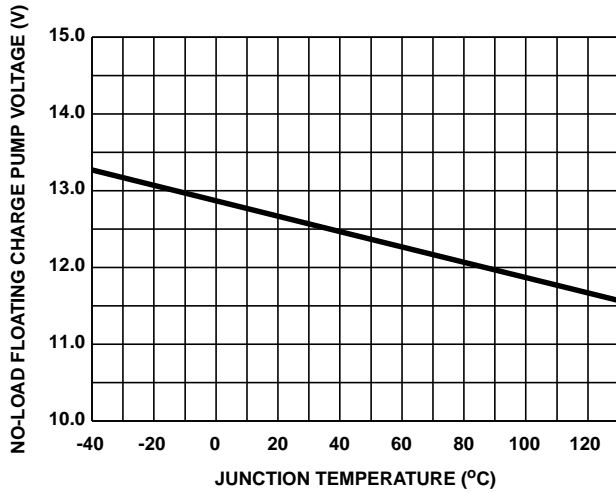


FIGURE 10. AHB - AHS, BHB - BHS NO-LOAD CHARGE PUMP VOLTAGE vs TEMPERATURE

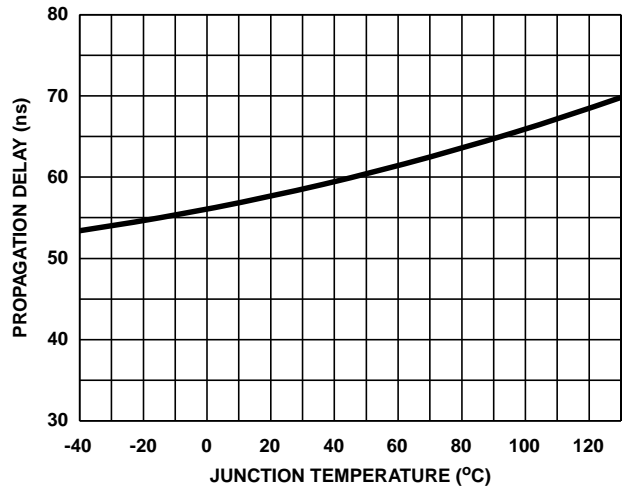


FIGURE 11. UPPER DISABLE TURN-OFF PROPAGATION DELAY  $T_{DISHIGH}$  vs TEMPERATURE

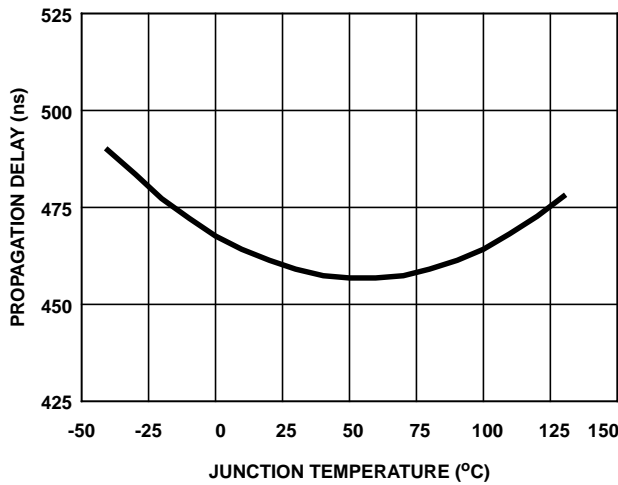


FIGURE 12. DISABLE TO UPPER ENABLE,  $T_{UEN}$ , PROPAGATION DELAY vs TEMPERATURE

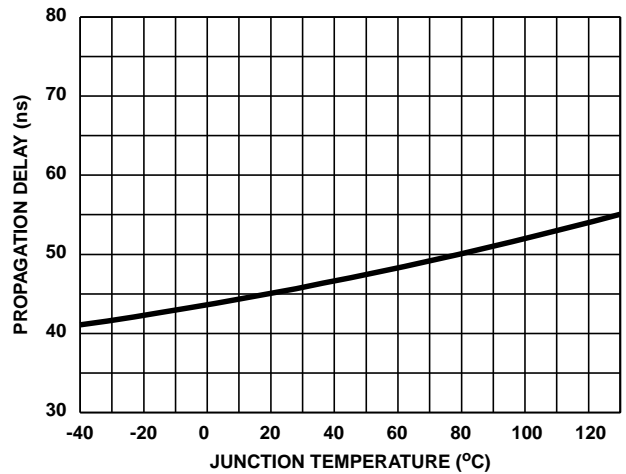


FIGURE 13. LOWER DISABLE TURN-OFF PROPAGATION DELAY  $T_{DISLOW}$  vs TEMPERATURE

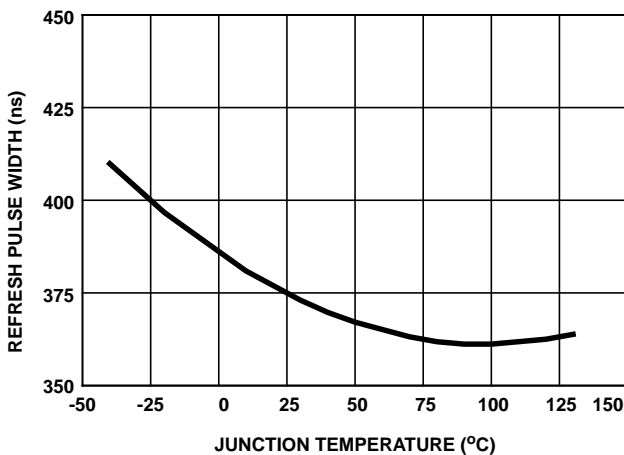


FIGURE 14.  $T_{REF-PW}$  REFRESH PULSE WIDTH vs TEMPERATURE

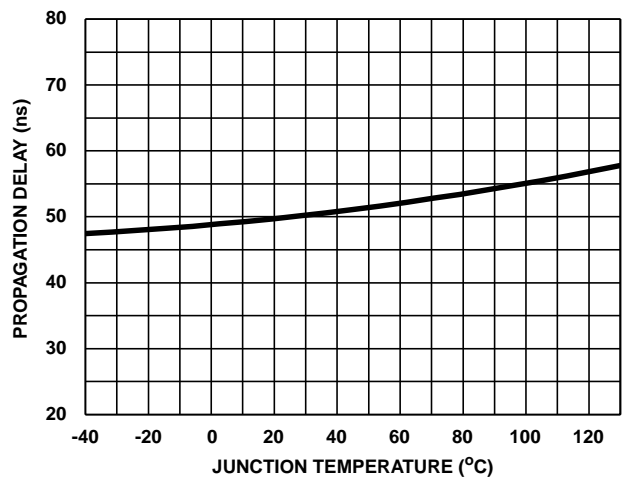


FIGURE 15. DISABLE TO LOWER ENABLE  $T_{DLPLH}$  PROPAGATION DELAY vs TEMPERATURE



# HIP4081A

**Typical Performance Curves**  $V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$ ,  $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$ ,  $R_{HDEL} = R_{LDEL} = 10K$  and  $T_A = 25^\circ C$ , Unless Otherwise Specified **(Continued)**

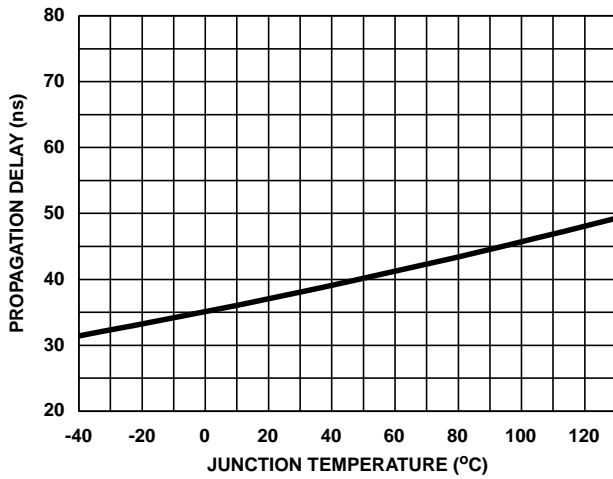


FIGURE 16. UPPER TURN-OFF PROPAGATION DELAY  $T_{HPHL}$  VS TEMPERATURE

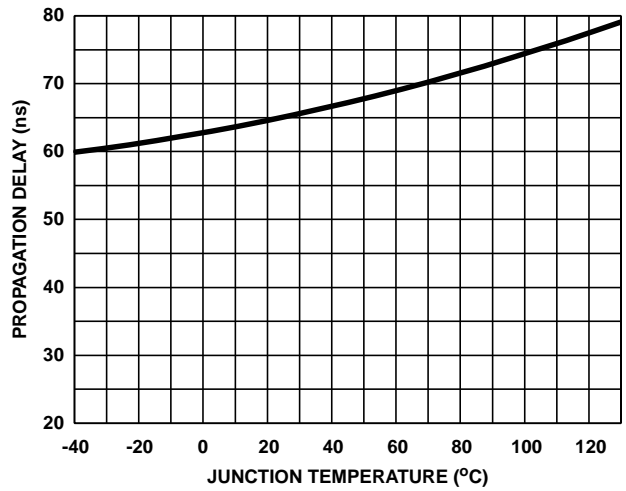


FIGURE 17. UPPER TURN-ON PROPAGATION DELAY  $T_{HPLH}$  VS TEMPERATURE

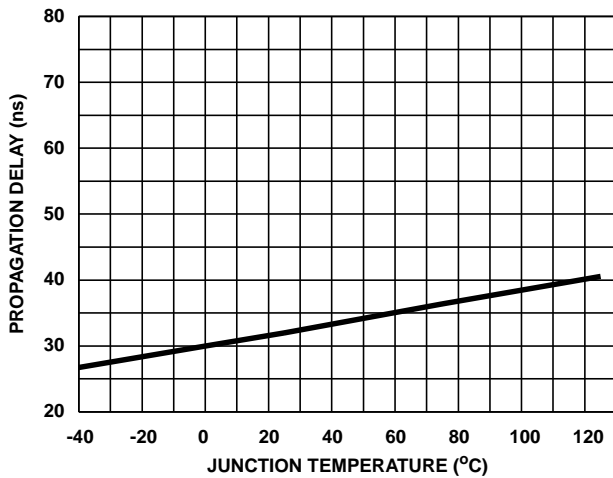


FIGURE 18. LOWER TURN-OFF PROPAGATION DELAY  $T_{LPHL}$  VS TEMPERATURE

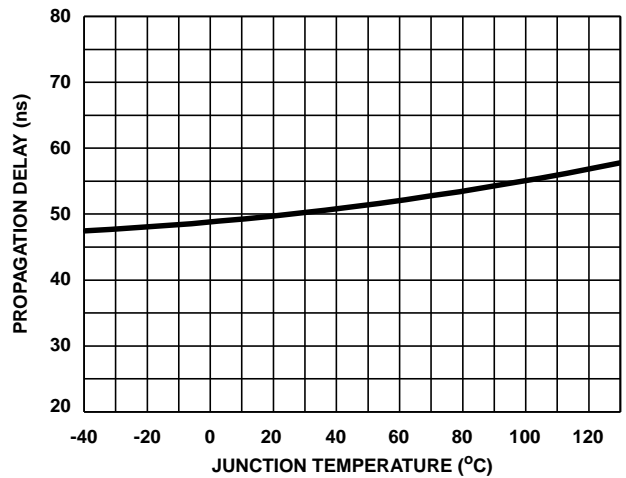


FIGURE 19. LOWER TURN-ON PROPAGATION DELAY  $T_{LPLH}$  VS TEMPERATURE

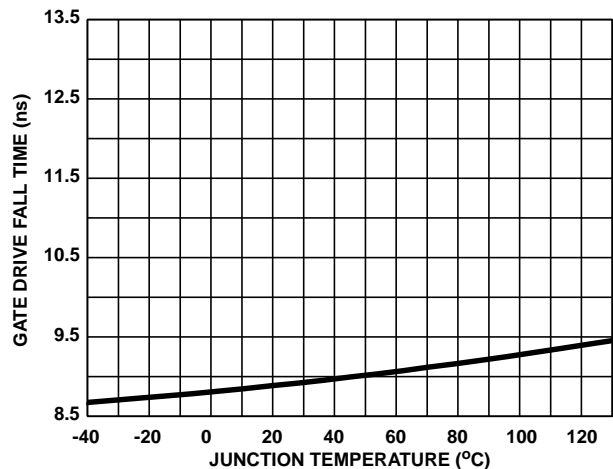


FIGURE 20. GATE DRIVE FALL TIME  $T_F$  VS TEMPERATURE

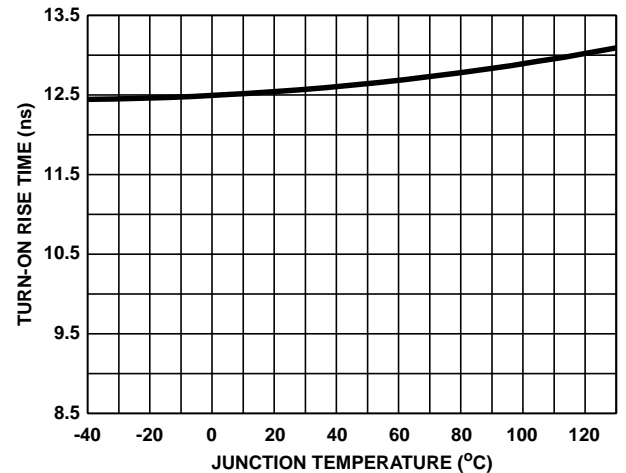


FIGURE 21. GATE DRIVE RISE TIME  $T_R$  VS TEMPERATURE

# HIP4081A

**Typical Performance Curves**  $V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$ ,  $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$ ,  $R_{HDEL} = R_{LDEL} = 100K$  and  $T_A = 25^\circ C$ , Unless Otherwise Specified

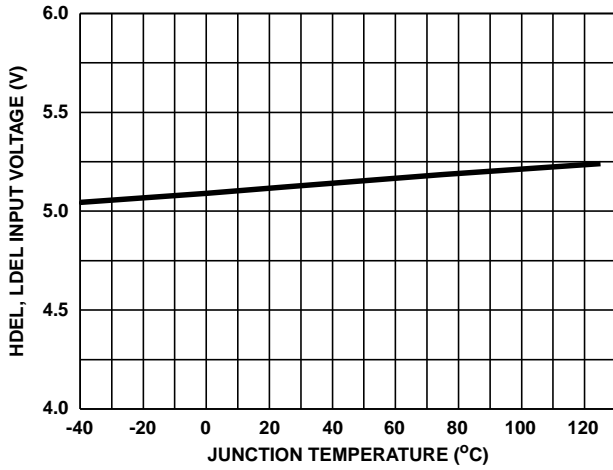


FIGURE 22.  $V_{LDEL}$ ,  $V_{HDEL}$  VOLTAGE vs TEMPERATURE

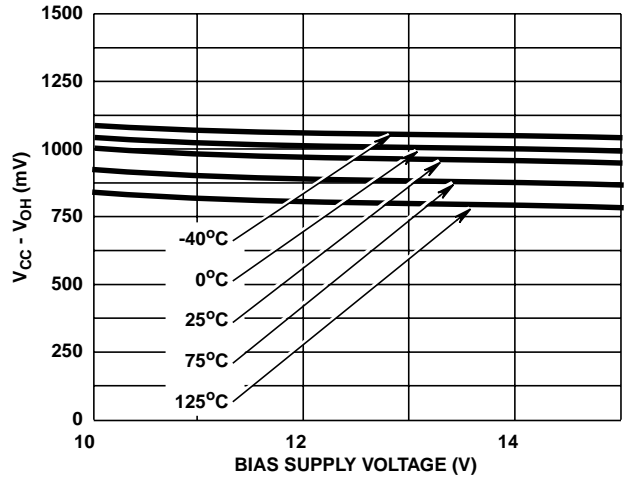


FIGURE 23. HIGH LEVEL OUTPUT VOLTAGE  $V_{CC} - V_{OH}$  vs BIAS SUPPLY AND TEMPERATURE AT 100mA

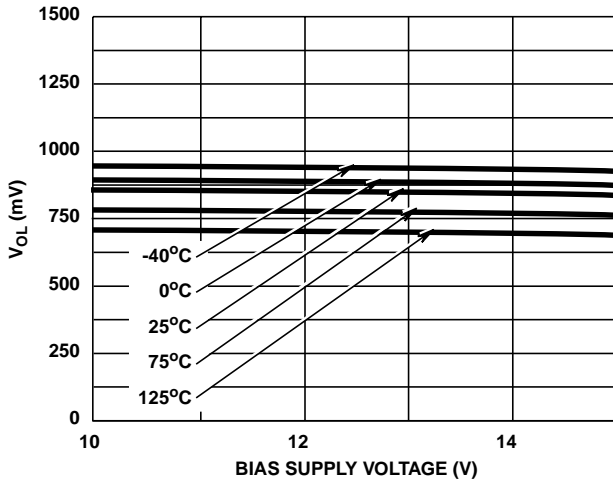


FIGURE 24. LOW LEVEL OUTPUT VOLTAGE  $V_{OL}$  vs BIAS SUPPLY AND TEMPERATURE AT 100mA

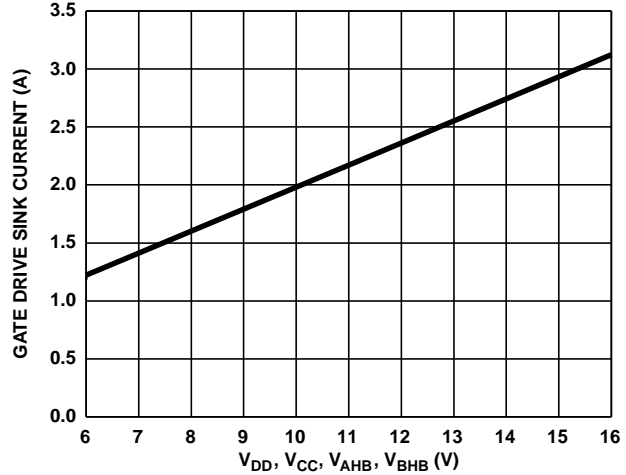


FIGURE 25. PEAK PULLDOWN CURRENT  $I_O$  vs BIAS SUPPLY VOLTAGE

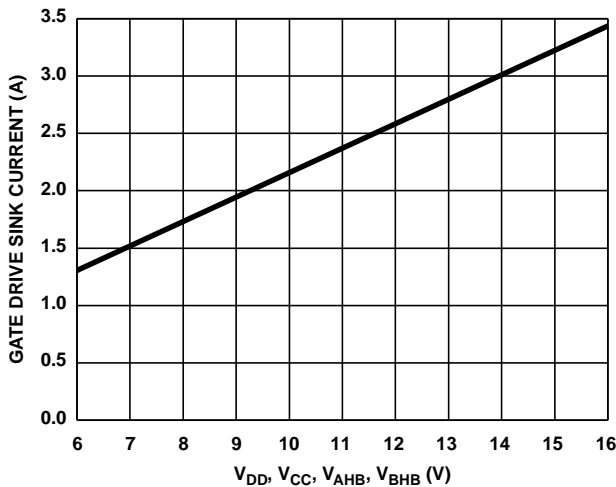


FIGURE 26. PEAK PULLUP CURRENT  $I_{O+}$  vs BIAS SUPPLY VOLTAGE

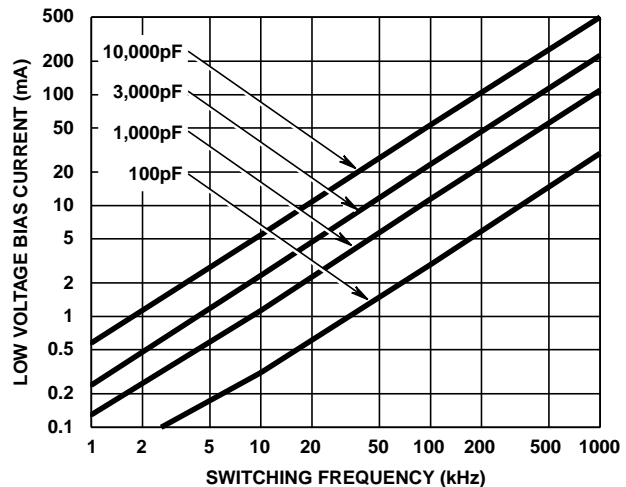


FIGURE 27. LOW VOLTAGE BIAS CURRENT  $I_{DD}$  (LESS QUIESCENT COMPONENT) vs FREQUENCY AND GATE LOAD CAPACITANCE

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**Typical Performance Curves**  $V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$ ,  $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$ ,  $R_{HDEL} = R_{LDEL} = 100K$  and  $T_A = 25^\circ C$ , Unless Otherwise Specified **(Continued)**

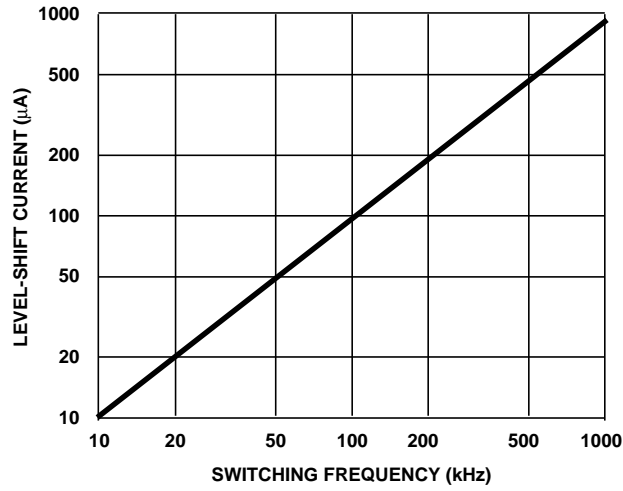


FIGURE 28. HIGH VOLTAGE LEVEL-SHIFT CURRENT vs FREQUENCY AND BUS VOLTAGE

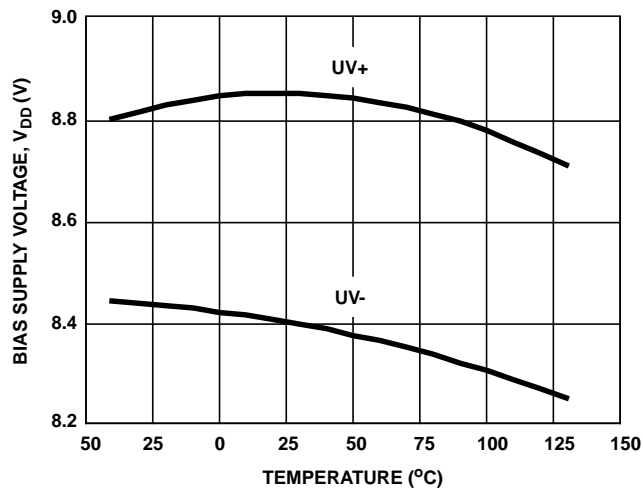


FIGURE 29. UNDERVOLTAGE LOCKOUT vs TEMPERATURE

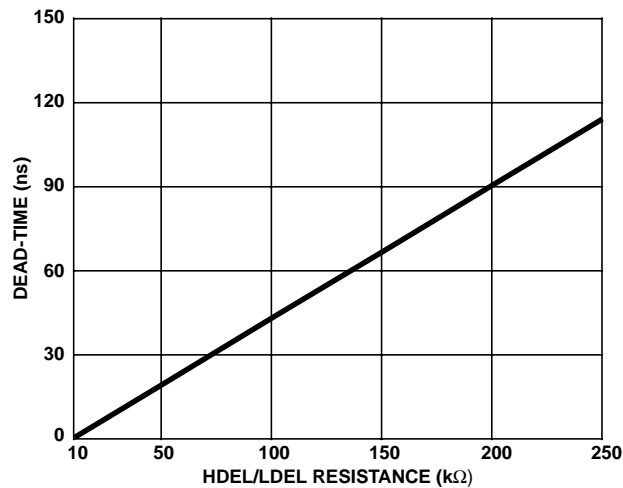


FIGURE 30. MINIMUM DEAD-TIME vs DEL RESISTANCE

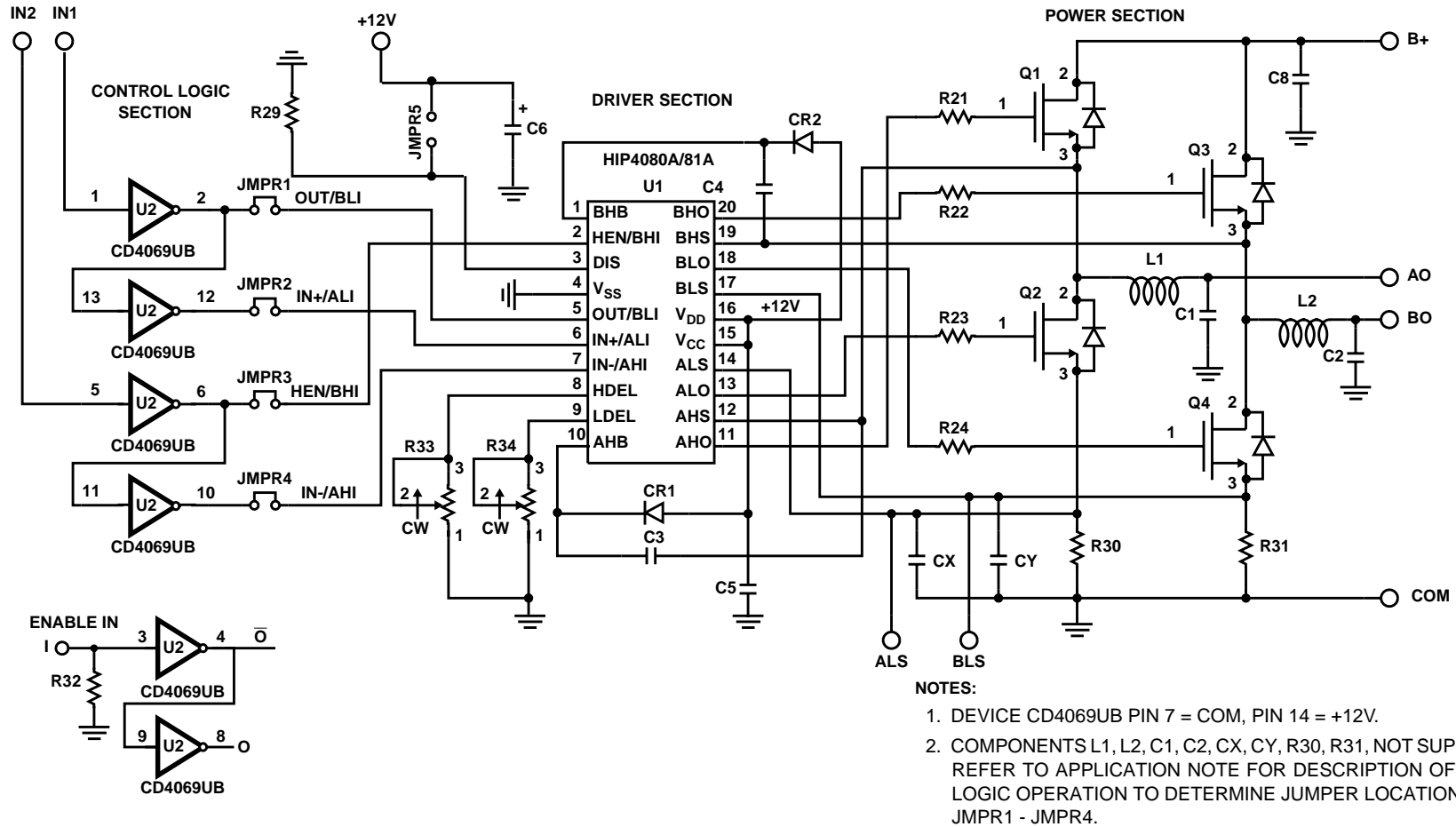


FIGURE 31. HIP4081A EVALUATION PC BOARD SCHEMATIC

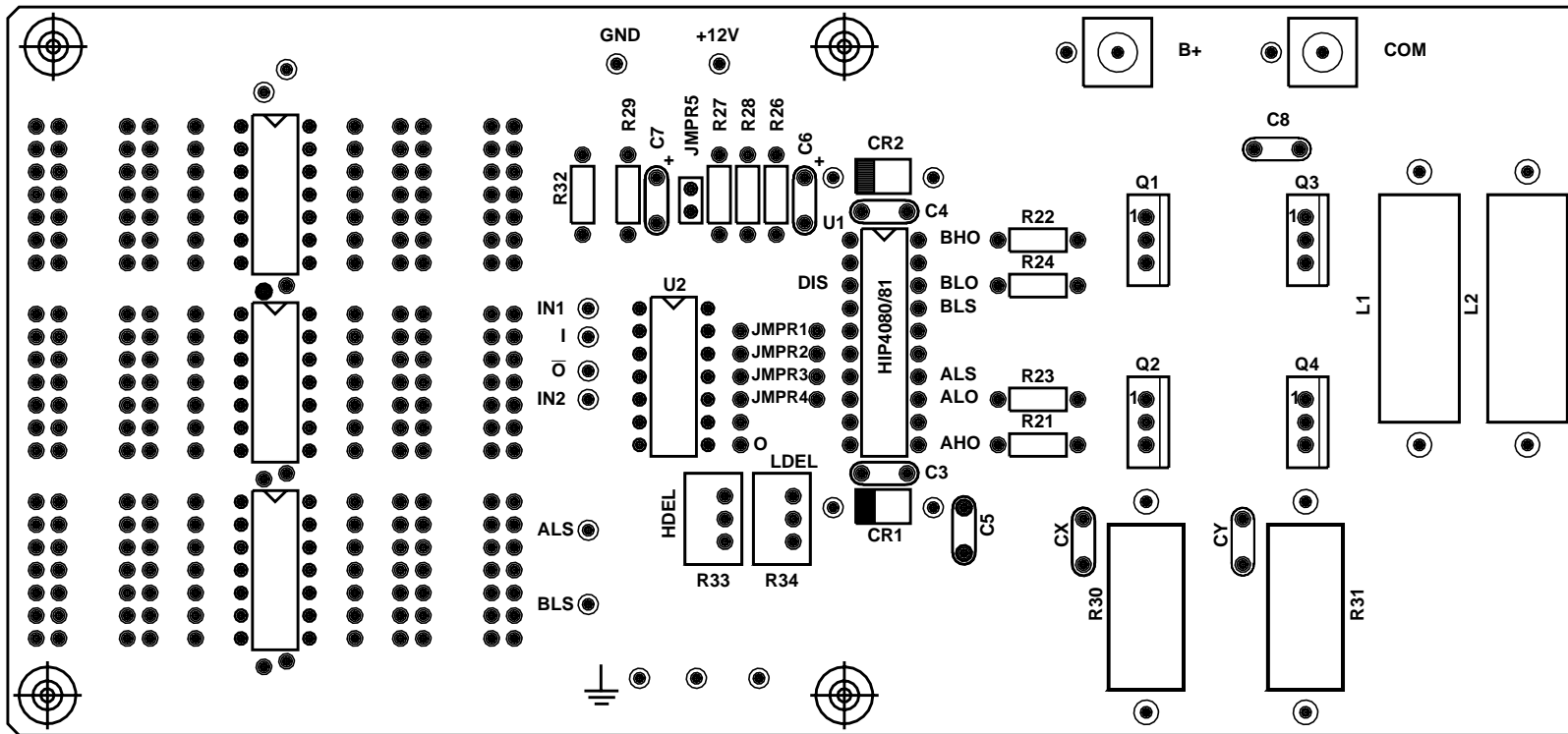
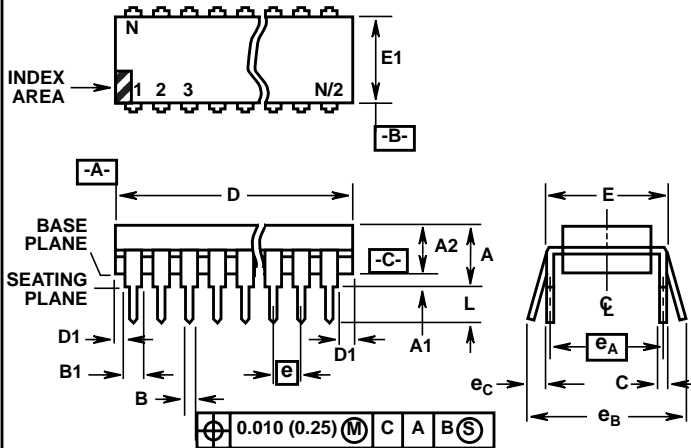


FIGURE 32. HIP4081A EVALUATION BOARD SILKSCREEN

# HIP4081A

## Dual-In-Line Plastic Packages (PDIP)



### NOTES:

- Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
- Dimensioning and tolerancing per ANSI Y14.5M-1982.
- Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
- Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
- D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
- E and  $e_A$  are measured with the leads constrained to be perpendicular to datum  $-C-$ .
- $e_B$  and  $e_C$  are measured at the lead tips with the leads unconstrained.  $e_C$  must be zero or greater.
- B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
- N is the maximum number of terminal positions.
- Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

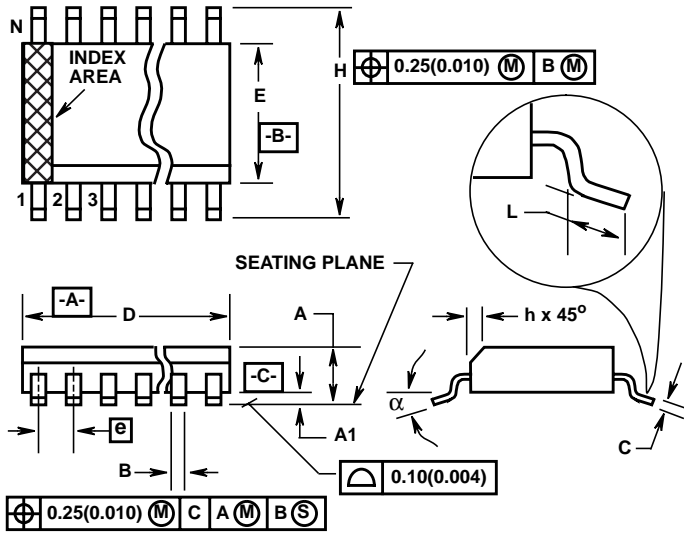
### E20.3 (JEDEC MS-001-AD ISSUE D) 20 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.55	1.77	8
C	0.008	0.014	0.204	0.355	-
D	0.980	1.060	24.89	26.9	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
$e_A$	0.300 BSC		7.62 BSC		6
$e_B$	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	20		20		9

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## Small Outline Plastic Packages (SOIC)



### M20.3 (JEDEC MS-013-AC ISSUE C) 20 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.4961	0.5118	12.60	13.00	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
α	0°	8°	0°	8°	-

#### NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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