FMS7950
Clock Multiplier

Features

- Crystal reference input
- Up to 175 MHz of output frequency
- Nine configurable outputs
- Output enable pin
- 250 pS of output to output skew
- 300 pS of Cycle to Cycle Jitter
- V_{DD} Range of 3.3V ±0.2V
- Commercial temperature range
- Available in 32 pin LQFP

Description

FMS7950 is a high speed clock synthesizer designed for clock multiplication applications. It uses phase locked loop technology to generate frequencies up to 175 MHz. It has four banks of configurable outputs.

Feedback select (FBsel) pin allows for wider range of input frequencies. When connected low, the lower input frequency range is selected. This provides output frequencies of up to eight times the input (see table 3). The higher input range is allowed when FBsel is connected high.

There are four banks of outputs where each bank has a dedicated divide select (DIV_SEL). Depending on the divide selection, the outputs are one half, one quarter, or one eighth of the VCO speed (see table 2 for details).

REF_SEL allows selection between crystal input or a clock driven input. Connecting PLL_EN LOW and REF_SEL HIGH will disable the Phase locked loop when the crystal oscillator is not used. In this mode, FMS7950 will be in clock buffer mode where any clock applied to TCLK will be divided down to the four output banks per Table 2. This is ideal for system diagnostic test.

FMS7950 operates at 3.3 Volts and is available in 32 pin LQFP.

Block Diagram
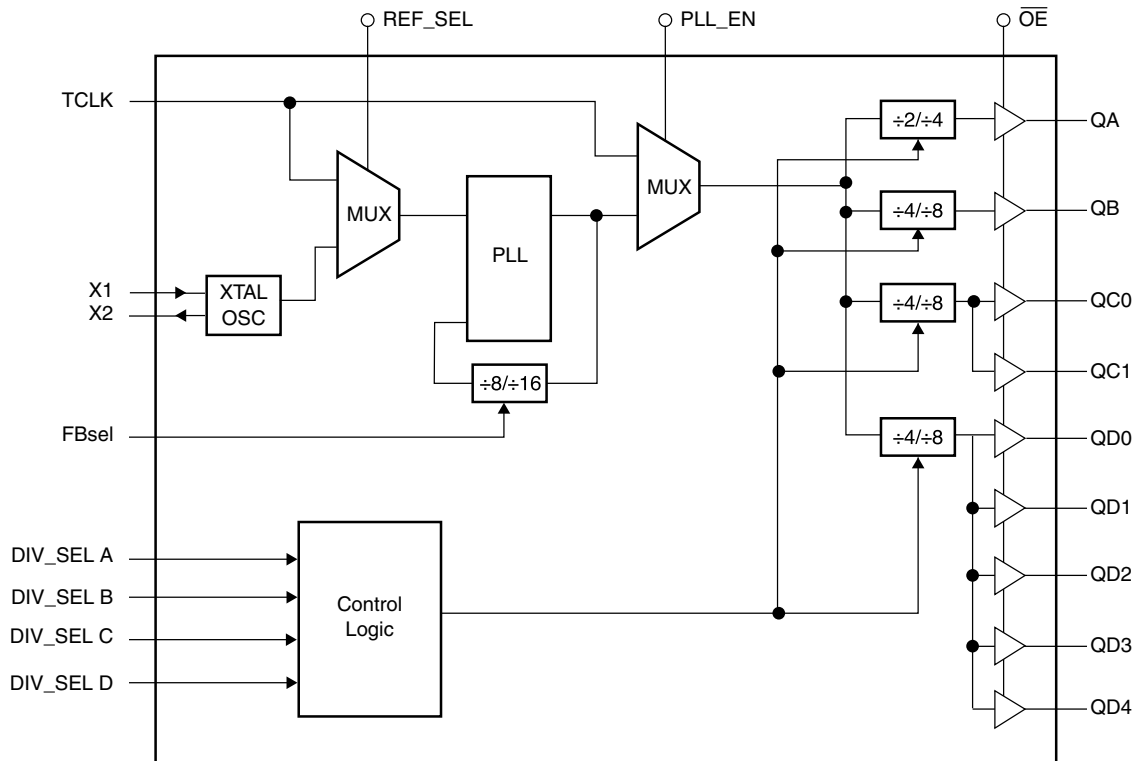
Pin Assignments
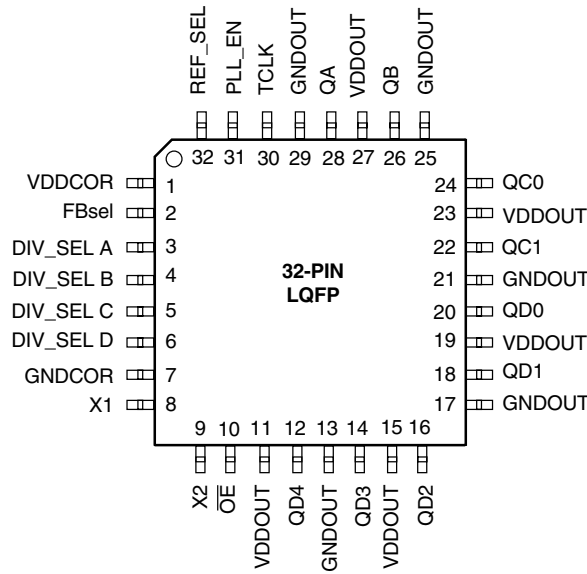
Pin Description

Pin Name	Pin #	Pin Type	Description
VDDCOR	1	PWR	**Power Connection.** Power supply for core logic and PLL circuitry. Connect to 3.3 Volts nominal.
FBsel	2	IN	**Feedback Select.** When high, the feedback divide is 8, and when low, it is 16. It allows for a wider range of input frequencies.
DIV_SEL(A:D)	3, 4, 5, 6	IN	**Divider Select:** It divides the clock to a desirable value. See table 2.
GNDCOR	7	PWR	**Ground Connection.** Ground for core logic and PLL circuitry. Connect to the common system ground plane.
X1	8	IN	**Crystal Connection.** An input connection for an external crystal or oscillator. 18 pF internal cap. It can be used as an external crystal connection or as an external reference frequency input.
X2	9	OUT	**Crystal Connection or External Reference Frequency.** This pin has dual functions.
$\overline{OE}$	10	IN	**Output Enable.** When high, all outputs are in high impedance. Normal operation when asserted low.
VDDOUT	11, 15, 19, 23, 27	PWR	**Power Connection.** Power supply for all the output buffers. Connect to 3.3 Volts nominal.
Q_A; Q_B; $Q_C(0:1)$; $Q_D(0:4)$	12, 14, 16, 18, 20, 22, 24, 26, 28	OUT	**Clock Outputs.** These outputs are multiple of the input.
GNDOUT	13, 17, 21, 25, 29	PWR	**Ground Connection.** Ground for all the outputs. Connect to common system ground plane.
TCLK	30	IN	**Test Clock.** When REF_SEL is high, all outputs are buffer copy of TCLK. When REF_SEL is low, TCLK is disabled.
PLL_EN	31	IN	**PLL Enable.** When low, PLL is bypassed.
REF_SEL	32	IN	**Reference Select.** When low, crystal is used for input. When high, TCLK is used for input.

Table 1. Functionality

REF_SEL	PLL_EN	$\overline{OE}$	PLL	All Outputs	Input
0	0	1	By Pass	Hi-Z	XTAL
0	0	0	By Pass	Running	XTAL
0	1	0	Enabled	Running	XTAL
1	0	1	By Pass	Hi-Z	TCLK
1	0	0	By Pass	Running	TCLK
1	1	0	Enabled	Running	TCLK

Table 2. Input Versus Output Frequency

DIV_SEL A	DIV_SEL B	DIV_SEL C	DIV_SEL D	FBsel = 1				FBsel = 0			
				QA	QB	QC	QD	QA	QB	QC	QD
0	0	0	0	4XRef	2XRef	2XRef	2XRef	8XRef	4XRef	4XRef	4XRef
0	0	0	1	4XRef	2XRef	2XRef	Ref	8XRef	4XRef	4XRef	2XRef
0	0	1	0	4XRef	2XRef	Ref	2XRef	8XRef	4XRef	2XRef	4XRef
0	0	1	1	4XRef	2XRef	Ref	Ref	8XRef	4XRef	2XRef	2XRef
0	1	0	0	4XRef	Ref	2XRef	2XRef	8XRef	2XRef	4XRef	4XRef
0	1	0	1	4XRef	Ref	2XRef	Ref	8XRef	2XRef	4XRef	2XRef
0	1	1	0	4XRef	Ref	Ref	2XRef	8XRef	2XRef	2XRef	4XRef
0	1	1	1	4XRef	Ref	Ref	Ref	8XRef	2XRef	2XRef	2XRef
1	0	0	0	2XRef	2XRef	2XRef	2XRef	4XRef	4XRef	4XRef	4XRef
1	0	0	1	2XRef	2XRef	2XRef	Ref	4XRef	4XRef	4XRef	2XRef
1	0	1	0	2XRef	2XRef	Ref	2XRef	4XRef	4XRef	2XRef	4XRef
1	0	1	1	2XRef	2XRef	Ref	Ref	4XRef	4XRef	2XRef	2XRef
1	1	0	0	2XRef	Ref	2XRef	2XRef	4XRef	2XRef	4XRef	4XRef
1	1	0	1	2XRef	Ref	2XRef	Ref	4XRef	2XRef	4XRef	2XRef
1	1	1	0	2XRef	Ref	Ref	2XRef	4XRef	2XRef	2XRef	4XRef
1	1	1	1	2XRef	Ref	Ref	Ref	4XRef	2XRef	2XRef	2XRef

Note:

1. Reference input could be either crystal input or TCLK input.

Table 3. Divide Select Functionality

DIV_SEL A	DIV_SEL B	DIV_SEL D	DIV_SEL D	QA	QB	QC	QD
0	0	0	0	÷2	÷4	÷4	÷4
1	1	1	1	÷4	÷8	÷8	÷8

Absolute Maximum Ratings

Symbol	Parameter	Ratings	Units
V_{DD}, V_{IN}	Voltage on any pin with respect to ground	-0.5 to 7.0	V
T_{STG}	Storage Temperature	-65 to 150	°C
T_B	Ambient Temperature	-55 to 125	°C
T_A	Operating Temperature	0 to 70	°C

Stresses greater than those listed in the table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may effect reliability.

DC Electrical Characteristics

T_A = 0 to 70°C; Supply Voltage 3.3 V ±0.2V (unless otherwise stated)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Low Voltage	V_{IL}				0.8	V
Input High Voltage	V_{IH}		2.0			V
Input Low Current	I_{IL}	V_{IN}= 0	-10		10	µA
Input High Current	I_{IH}	V_{IN}= V_{DD}	-30		30	µA
Output Low Voltage	V_{OL}	I_{OL}= 40 mA			0.5	V
Output High Voltage	V_{OH}	I_{OH}= −40mA	2.2			V
Input Capacitance[1]	C_{IN}				7.0	pF
Supply Current	I_{DD}	Outputs loaded			200	mA
Clock Stabilization[1]	T_{STAB}	From V_{DD} = 3.3V to 1% Target			10	mS

Note:
1. Guaranteed by design, not subject to 100% production testing.

AC Electrical Characteristics

T_A = 0 to 70°C; Supply Voltage V_{DD} = 3.3V ±0.2V, C_L = 10 pF (unless otherwise stated)

| Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency Range	F_{INPUT}	FBsel = 1	25		43	MHz
		FBsel = 0	12		22	MHz
Output Frequency Range	F_{OUT}	Q_A; DIV_SEL A = 0V			175	MHz
		Q_B, Q_C & Q_D; DIV_SEL B, C, D = 0V			88	MHz
Output to Output Skew	T_{SK1}	V_{TH} = V_{DD}/2; DIV_SEL A = 0		400	750	pS
		V_{TH} = V_{DD}/2; DIV_SEL A = 1	-300	100	300	
Rise Time[1]	T_R	0.8 to 2.0V	0.10		1.0	nS
Fall Time[1]	T_F	2.0 to 0.8V	0.10		1.0	nS
Duty Cycle[1]	D_T	V_{TH} = V_{DD}/2	45		55	%
Jitter (Cycle-Cycle)	T_{JIT}	QA: DIV_SEL A = 0			450	pS
		QA: DIV_SEL A = 1			200	
		QB Output			200	
		QC(0:1) Outputs			300	
		QD(0:4) Outputs			375	

Note:
1. Guaranteed by design, not subject to 100% production testing.

Parameter Measurement Information

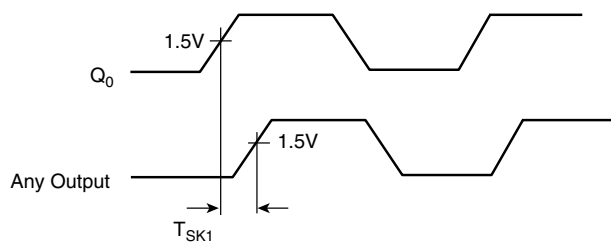### Duty Cycle (D$_T$)

$$D_T = \frac{T_2}{T_1} \times 100$$
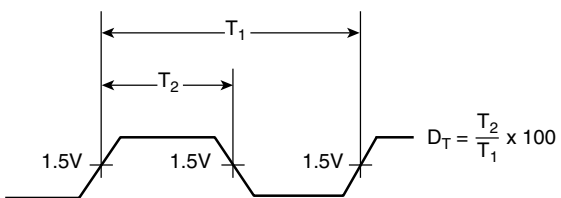
Rise/Fall Time (T$_R$/T$_F$)
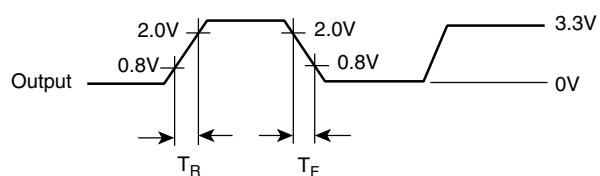
Output to Output Skew (T$_{SK1}$)

Application

FMS7950 is one of the simplest form of frequency synthesizer. It uses phase locked loop technology with a divide of "N" in its feedback path. Its purpose is to generate a large number of different output frequencies, all related to a single, highly stable reference source. To achieve this, a crystal is connected at X1 and X2. No external components are required since the capacitors and oscillator are integrated.
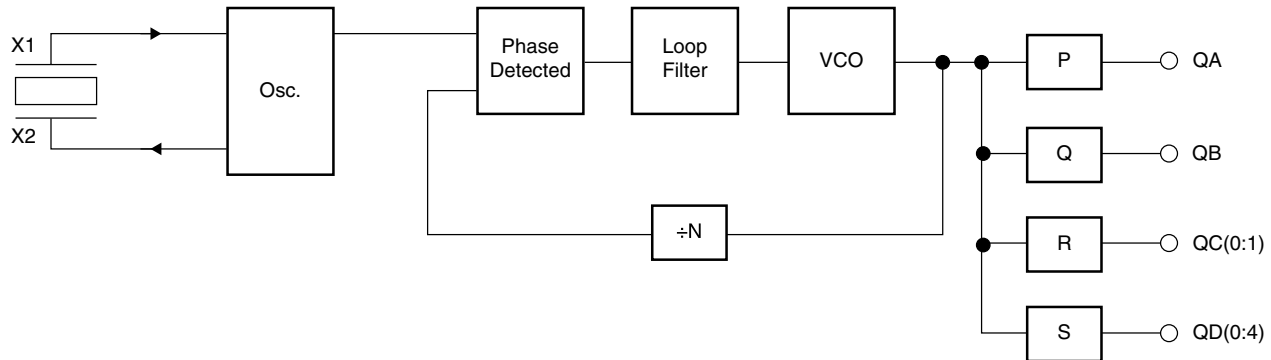
Figure 1 depicts the block diagram for FMS7950.

Figure 1.

In general, phase locked loops are governed by the equation:

$$F_{OUT} = N \bullet F_{REF} \qquad\qquad \text{Equation 1}$$

Equation 1 states that any output can be generated if "N" is varied. In FMS7950, the available dividers are eight or sixteen. These values are selected by connecting FBsel to ground or VDD. To determine the allowable range of input frequencies for each different FBsel setting, the following equation must be used:

$$F_{REF} = F_{VCO} \div N \qquad\qquad \text{Equation 2}$$

If divided by eight is selected, the minimum input range will be:

$$F_{REF\_MIN} = 200 \div 8$$
$$= 25 \text{ MHZ}$$

The maximum input range:

$$F_{REF\_MAX} = 360 \div 8$$
$$= 43.75 \text{ MHZ}$$

If divide by sixteen is selected, a lower range of input frequency is allowed (12.5–22MHZ). This analysis reveals that if lower input frequency is available, FBsel must be connected to GND. On the other hand, higher input frequencies require FBsel to be connected to VDD.

In practical applications, it is always the output frequency that is known and one must work backwards to determine the input and VCO frequencies. The best approach to explain is by an example. Assume an application requires the following output frequencies:

$$\begin{aligned} QA &= 133.33 \text{ MHZ} \\ QB &= 66.66 \text{ MHZ} \\ QC \ \& \ QD &= 33.33 \text{ MHZ} \end{aligned}$$

The following connection is used:

$$DIV\_SEL\ A \quad = 0\ ;\ P = 2$$
$$DIV\_SEL\ B \quad = 0\ ;\ Q = 4$$
$$DIV\_SEL\ C\ \&\ D \ = 1\ ;\ R = S = 8$$

To calculate the VCO frequency, we find the output that requires the highest frequency and used the following equation. In this case, it will be QA output.

$$F_{VCO} = P \bullet QA$$
$$= 2 \bullet 133.33\ MHZ$$
$$= 266.66\ MHZ$$

To determine the input frequency, we will use Equation 2, and set "N" to 16:

$$F_{REF} = 266.66\ MHZ \div 16$$
$$= 16.66\ MHZ$$

Note, divide by eight could also have been used. The only difference is that it would require an input clock of 33.33MHZ rather than 16.66MHZ.

Mechanical Dimensions

32-Pin LQFP

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	–	0.063	–	1.60	
A1	0.002	0.006	0.05	0.15	
A2	0.053	0.057	1.35	1.45	
B	0.012	0.018	0.30	0.45	7
C	–	0.004	–	0.10	
D/E	0.354 BSC		9.00 BSC		
D1/E1	0.276 BSC		7.00 BSC		2
e	0.032 BSC		0.800 BSC		
L	0.018	0.030	0.45	0.75	6
N	32		32		4
ND	8		8		5
α	0°	7°	0°	7°	
ccc	–	0.004	–	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Dimensions "D1" and "E1" do not include mold protrusion.
3. Pin 1 identifier is optional.
4. Dimension N: number of terminals.
5. Dimension ND: Number of terminals per package edge.
6. "L" is the length of terminal for soldering to a substrate.
7. "B" includes lead finish thickness.
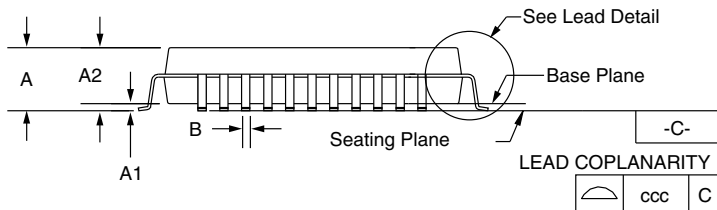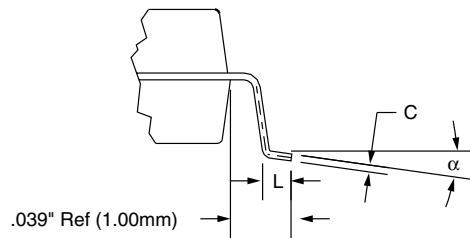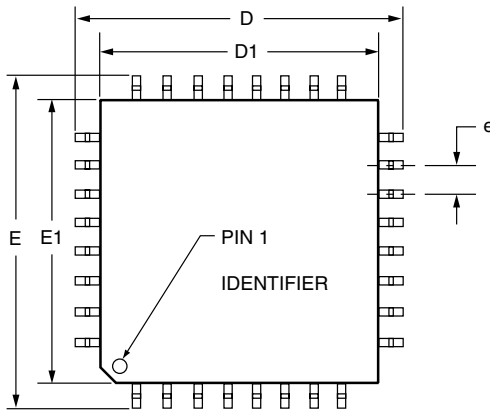
Ordering Information

Product Number	Package Description	Package Marking
FMS7950KWC	LQFP-32	7950KWC
FMS7950KWCX	LQFP-32 w/T+R	7950KWC

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