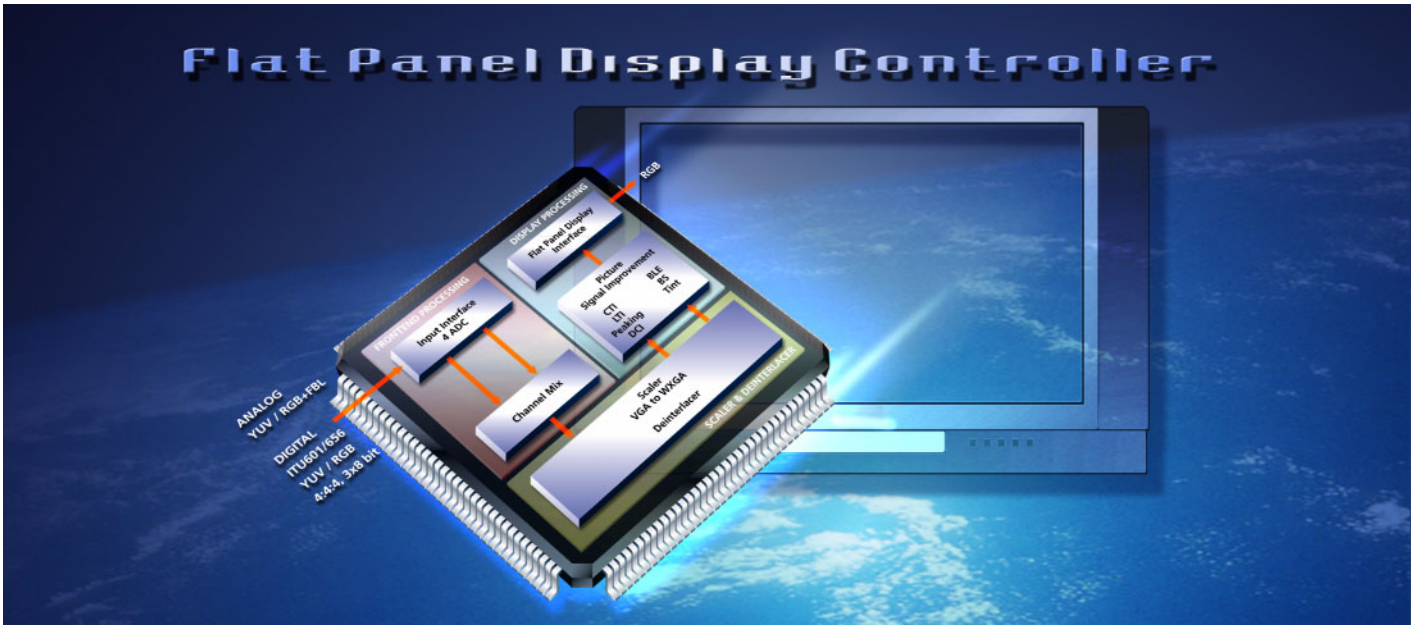
DPS 9455B

Dec/2003



DPS 9455B
Display Processor and Scaler with HDTV and PC Input

The DPS 9455B is a single-chip digital display processor and scaler, especially designed for FPD-TV sets (LCD-TV, PDP-TV) supporting HDTV signal input and de-interlacing as well as PC-signal input. The DPS 9455B is a new member of Micronas' IC family implemented in deep submicron CMOS technology.

Video Inputs

- Digital input for 50/60 I or 50/60 P signals in ITU-656 (8 bit) or ITU-601 (16 bit)
- 3×8 bit YC_rC_b/RGB input
- 2 analog RGB/YC_rC_b inputs for Teletext, graphics, 480p, 576p, 1080i and 720p
- 4 built-in ADCs (8-bit) for RGB + Fast-Blank with 81 MHz sampling rate
- PC input up to XGA at 75 Hz and WXGA at 60 Hz
- Separate HS and VS (2×) inputs

Sync Processing

- 3-level sync-separation for 1080i and 720p
- HS and VS outputs to synchronize
  - the ext. analog RGB/YC_rC_b source in the softmix mode (see display modes)
  - external OSD source

Display Modes

- Digital mode: video from the digital input
- Analog mode: video/graphics/Teletext from the analog RGB/YC_rC_b input
- Softmix mode: soft mixing of the video and component input
- OSD signals can be inserted digitally

Video Processing

- Full 4:4:4 processing
- RGB-to-YC_rC_b conversion
- Brightness, contrast, saturation for analog component input
- Dynamic contrast improvement (DCI)
- Black level expander (BLE)
- Luma & chroma transition improvement
- Dynamic peaking
- Brightness, contrast, saturation, tint
- Programmable YC_rC_b-to-RGB matrix
- Programmable characteristics on R, G, B, for γ-correction, blue-stretch, white-drive
- Dithering for 8 to 6-bit digital outputs

Display Format Processing

- Prescaling of the input signal: horizontal scaling factor: 1.0 to 1/64
- Upscaling of the output signal: horizontal scaling factor: 1 to 4 (5-zone panorama generator)
- Vertical scaling factor: 0.5 to 4
- De-interlacing with line-doubling/ upscaling

OSD

- digital RGB input (6 or 12 bit/pixel)
- 64 entry CLUT with 12-bit colors
- Picture frame and testpattern generation
- Half-contrast switch (0, 25%, 50%, 100%)

Display Resolutions

- 640×480 (VGA; 4:3 panel)
- 852×480 (W-VGA; 16:9 panel)
- 800×600 (SVGA)
- 1024×768 (XGA)
- 1366×768 (W-XGA)

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Output Interface

- 2×18 or 24-bit RGB output: dual-pixel mode
- programmable panel control signals

Miscellaneous

- Up to 2 PWM outputs
- Up to 8 general-purpose I/Os
- I^2C interface (400 kHz)
- JTAG boundary scan interface
- 1.8 V and 3.3 V supply
- PMQFP144 package

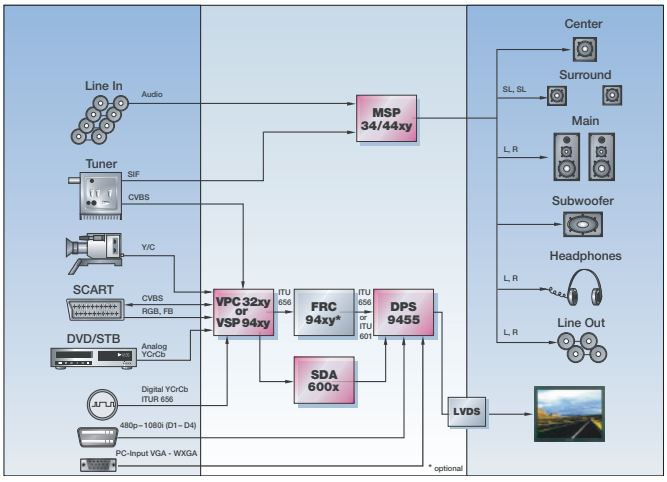

Fig. 1: Application example: LCD-TV with DPS 9455B and HDTV Input

System Architecture

Figure 2 shows the block diagram of the DPS 9455B. The device has digital outputs. In principle, the device comprises three major functional and clock domain parts.

The functional parts are

- Video input processing,
- Scaling, and
- Display processing.

The clock domains are

- ITU domain,
- Input domain, and
- Display domain (compare the block diagram and the different shaded areas).

The input and the output signals of the IC can be chosen in various configurations.

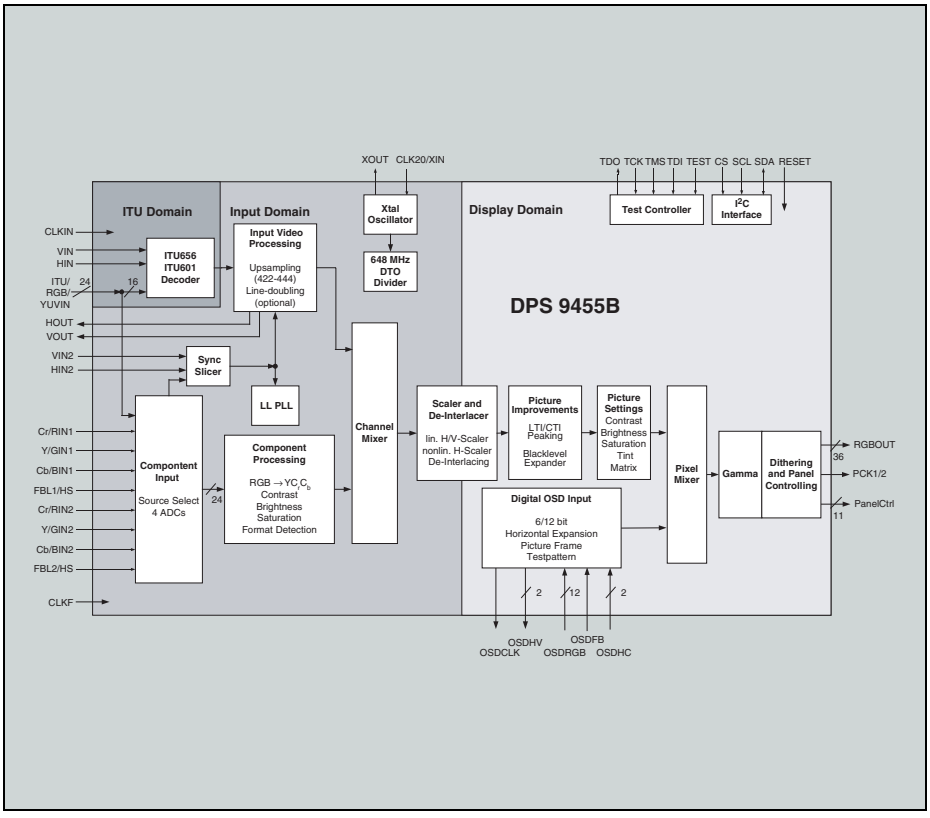

Fig. 2: Block diagram of the DPS 9455B

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