100MHz Pentium®II Clock Synthesizer/Driver with Spread Spectrum for Mobile PCs

Features

- **Mixed 2.5V and 3.3V operation**
- **Complete clock solution for Pentium® II, and other similar processor-based motherboards**
    - **Two CPU clocks at 2.5V up to 100 MHz**
    - **Six synchronous PCI clocks, one free-running**
    - **One 3.3V Ref. clock at 14.318 MHz**
    - **One 3.3V USB clock at 48 MHz (-2S only)**
- **Spread Spectrum clocking for EMI control (-11S, -2S)**
- **1.5–4.0 ns delay between CPU and PCI clocks**
- **Power-down, CPU stop and PCI stop pins**
- **Low skew outputs, $\leq$ 175 ps between CPU clocks**
- **Factory-EPROM programmable output drive and slew rate for EMI customization**
- **Available in space-saving 28-pin SSOP package**

Functional Description

The CY2281 is a clock synthesizer/driver for Pentium II, or other similar processor-based mobile PCs requiring up to 100 MHz support. The CY2281 outputs two CPU clocks at 2.5V. There are six PCI clocks, running at one-half or one-third the CPU clock frequency of 66.6 MHz and 100 MHz respectively. One of the PCI clocks is free-running. Additionally, the part outputs one 3.3V reference clock at 14.318 MHz. The CY2281-2S also provides one 3.3V USB clock at 48 MHz.

The CY2281-11S and CY2281-2S incorporate the Intel®-defined spread spectrum feature. They provide a –0.6% downspread on the CPU and PCI clocks, which can help reduce EMI in certain high-speed systems. A summary of clock outputs for both devices is shown below.

The part possesses power-down, CPU stop, and PCI stop pins for power management control. The signals are synchronized on-chip, and ensure glitch-free transitions on the outputs. When the $\overline{\text{CPU\_STOP}}$ input is asserted, the CPU clock outputs are driven LOW. When the $\overline{\text{PCI\_STOP}}$ input is asserted, the PCI clock outputs (except the free-running PCI clock) are driven LOW. When the $\overline{\text{PWR\_DWN}}$ pin is asserted, the reference oscillator and PLLs are shut down, and all outputs are driven LOW.

The CY2281 clock outputs are designed for low EMI emissions. Controlled rise and fall times, unique output driver circuits, and innovative circuit layout techniques enable the CY2281 to have lower EMI than clock devices from other manufacturers. Additionally, factory-EPROM programmable output drive and slew-rate control enable optimal configurations.
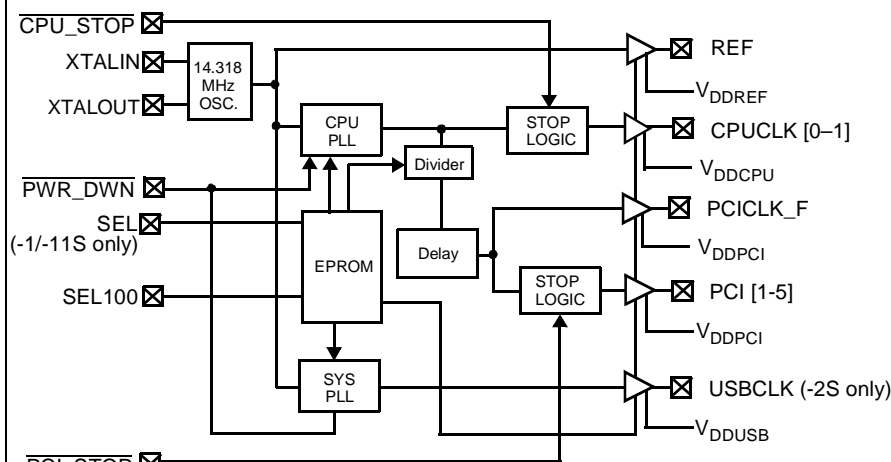
CY2281 Selector Guide

Clock Outputs	-1	-11S	-2S
CPU (66, 100 MHz)	2	2	2
PCI (CPU/2, CPU/3)	6[1]	6[1]	6[1]
REF (14.318 MHz)	1	1	1
USB (48 MHz)	N/A	N/A	1
CPU-PCI delay	1.5–4.0 ns	1.5–4.0 ns	1.5–4.0 ns
Spread Spectrum	None	–0.6%	–0.6%

Note:
1. One free-running PCI clock.

Logic Block Diagram

Pin Configuration

28-Pin SSOP
Top View

XTALIN	1	28	V_{SS}
XTALOUT	2	27	V_{DDREF}
V_{SS}	3	26	REF
PCICLK_F	4	25	V_{DDCPU}
PCICLK1	5	24	CPUCLK0
V_{DDPCI}	6	23	CPUCLK1
PCICLK2	7	22	V_{SS}
PCICLK3	8	21	AV_{DD}
V_{DDPCI}	9	20	V_{SS}
PCICLK4	10	19	$\overline{\text{PCI\_STOP}}$
PCICLK5	11	18	$\overline{\text{CPU\_STOP}}$
V_{SS}	12	17	$\overline{\text{PWR\_DWN}}$
V_{DDUSB}	13	16	SEE CHART BELOW
V_{SS}	14	15	SEL100
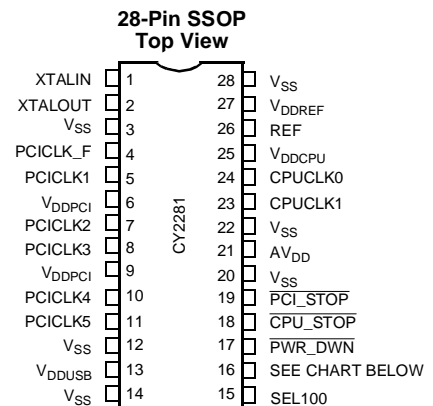
Option	Pin 16
-1,-11S	SEL
-2S	USBCLK

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Pin Summary

Name	Pins	Description
V_{DDPCI}	6, 9	3.3V Digital voltage supply for PCI clocks
V_{DDREF}	27	3.3V Digital voltage supply for REF clocks
V_{DDCPU}	25	2.5V Digital voltage supply for CPU clocks
V_{DDUSB}	13	3.3V Digital voltage supply for USB clock
AV_{DD}	21	Analog voltage supply, 3.3V
V_{SS}	3, 12, 14, 20, 22, 28	Ground
XTALIN[2]	1	Reference crystal input
XTALOUT[2]	2	Reference crystal feedback
$\overline{PCI\_STOP}$	19	Active LOW control input to stop PCI clocks
$\overline{CPU\_STOP}$	18	Active LOW control input to stop CPU clocks
$\overline{PWR\_DWN}$	17	Active LOW control input to power down device
SEL	16	CPU frequency select input (-1 and -11S options only)
USBCLK	16	USB clock output, 48 MHz fixed (-2S option only)
SEL100	15	CPU frequency select input, selects between 100 MHz and 66.6 MHz (see table below)
CPUCLK[0:1]	23, 24	CPU clock outputs
PCICLK[1:5]	5, 7, 8, 10, 11	PCI clock outputs, at one-half or one-third the CPU frequency of 66.6 MHz or 100 MHz respectively
PCICLK_F	4	Free-running PCI clock output
REF	26	3.3V Reference clock output

Function Table

SEL100	SEL[4]	CPU/PCI Ratio	CPUCLK	PCICLK_F PCICLK	USBCLK[5]	REF
0	0	2	Hi-Z	Hi-Z		Hi-Z
0	1	2	66.66 MHz	33.33 MHz	48 MHz	14.318 MHz
1	0	3	TCLK/2	TCLK/6		TCLK[3]
1	1	3	100 MHz	33.33 MHz	48 MHz	14.318 MHz

Notes:
2. For best accuracy, use a parallel-resonant crystal, C_{LOAD} = 18 pF.
3. TCLK supplied on the XTALIN pin in Test Mode.
4. SEL available on options -1 and -11S only. SEL tied HIGH internally on option -2S
5. USBCLK available on option -2S only.

Actual Clock Frequency Values

Clock Output	Target Frequency (MHz)	Actual Frequency (MHz)	PPM
CPUCLK	66.67	66.654	−195
CPUCLK	100	99.77	−2346
USB	48	48.008	167

Power Management Logic

$\overline{CPU\_STOP}$	$\overline{PCI\_STOP}$	$\overline{PWR\_DWN}$	CPUCLK	PCICLK	PCICLK_F	Other Clocks	Osc.	PLLs
X	X	0	Low	Low	Low	Low	Off	Off
0	0	1	Low	Low	Running	Running	Running	Running
0	1	1	Low	Running	Running	Running	Running	Running
1	0	1	Running	Low	Running	Running	Running	Running
1	1	1	Running	Running	Running	Running	Running	Running

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage .... −0.5V to +7.0V

Input Voltage .... −0.5V to V_{DD}+0.5

Storage Temperature (Non-Condensing) ... −65°C to +150°C

Max. Soldering Temperature (10 sec) .... +260°C

Junction Temperature .... +150°C

Static Discharge Voltage .... ≥1700V
(per MIL-STD-883, Method 3015, like V_{DD} pins tied together)

Operating Conditions[6]

Parameter	Description	Min.	Max.	Unit
AV_{DD}, V_{DDPCI}, V_{DDREF}, V_{DDUSB}	Analog and Digital Supply Voltage	3.135	3.465	V
V_{DDCPU}	CPU Supply Voltage	2.375	2.625	V
T_A	Operating Temperature, Ambient	0	70	°C

C_L	Max. Capacitive Load on
	    CPUCLK
	    PCICLK
	    REF
			
			20
			30
			20
				pF

$f_{(REF)}$	Reference Frequency, Oscillator Nominal Value	14.318	14.318	MHz

Electrical Characteristics Over the Operating Range

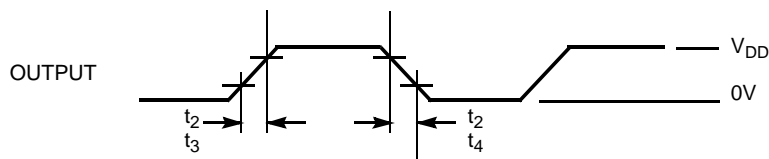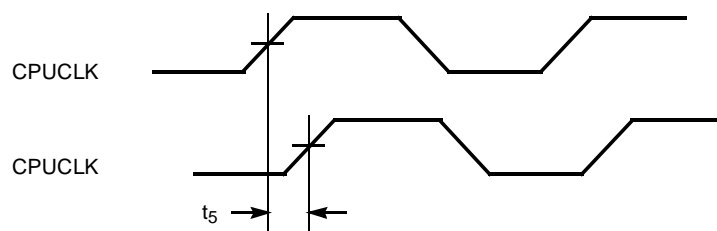| Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{IH}	High-level Input Voltage	Except Crystal Inputs[7]			2.0		V
V_{IL}	Low-level Input Voltage	Except Crystal Inputs[7]				0.8	V
V_{OH}	High-level Output Voltage	V_{DDCPU} = 2.375V	I_{OH} = 12 mA	CPUCLK	2.0		V
V_{OL}	Low-level Output Voltage	V_{DDCPU} = 2.375V	I_{OL} = 12 mA	CPUCLK		0.4	V
V_{OH}	High-level Output Voltage	V_{DDPCI}, AV_{DD}, V_{DDREF} = 3.135V	I_{OH} = 14.5 mA	PCICLK	2.4		V
			I_{OH} = 16 mA	REF, USB			
V_{OL}	Low-level Output Voltage	V_{DDPCI}, AV_{DD}, V_{DDREF} = 3.135V	I_{OL} = 9.4 mA	PCICLK		0.4V	V
			I_{OL} = 9 mA	REF, USB			
I_{IH}	Input High Current	V_{IH} = V_{DD}			−10	+10	μA
I_{IL}	Input Low Current	V_{IL} = 0V				10	μA
I_{OZ}	Output Leakage Current	Three-state			−10	+10	μA
I_{DD25}	Power Supply Current for 2.5V Clocks	V_{DDCPU} = 2.625V, V_{IN} = 0 or V_{DD}, Loaded Outputs, CPU = 66.6 MHz				70	mA
I_{DD25}	Power Supply Current for 2.5V Clocks	V_{DDCPU} = 2.625V, V_{IN} = 0 or V_{DD}, Loaded Outputs, CPU = 100 MHz				100	mA
I_{DD33}	Power Supply Current for 3.3V Clocks	V_{DD} = 3.465V, V_{IN} = 0 or V_{DD}, Loaded Outputs				170	mA
I_{DDS}	Powerdown Current	Current draw in powerdown state				500	μA

Notes:
6. Electrical parameters are guaranteed with these operating conditions.
7. Crystal Inputs have CMOS thresholds.

Switching Characteristics[8] Over the Operating Range
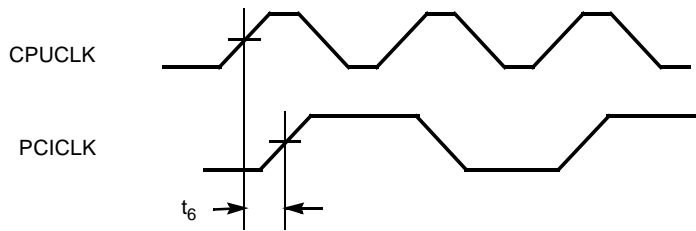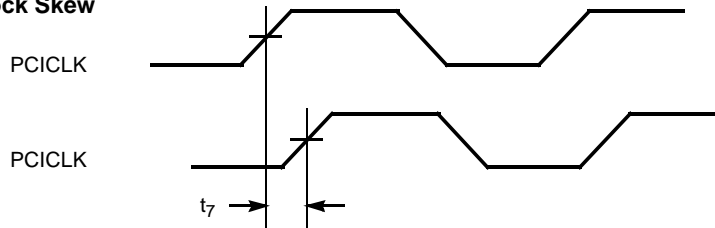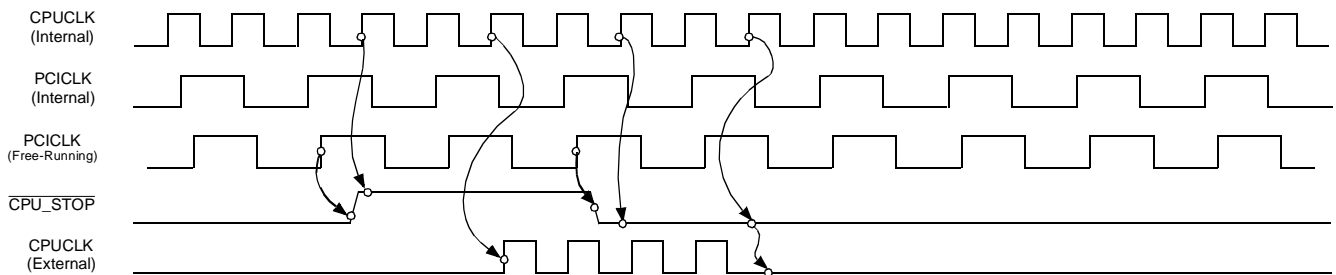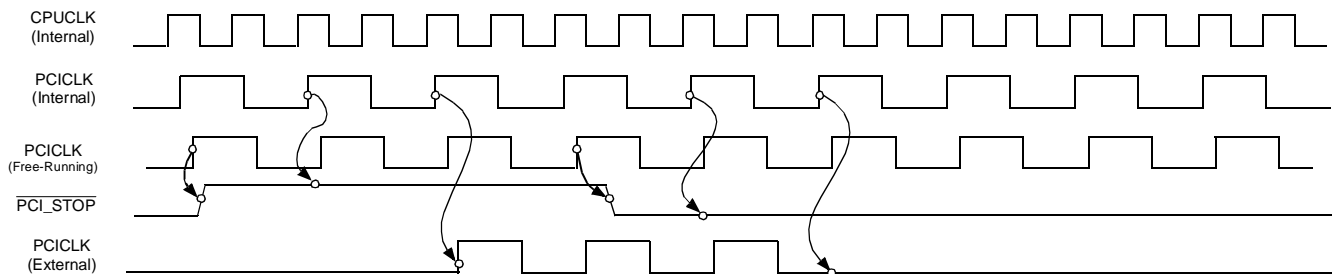
Parameter	Output	Description	Test Conditions	Min.	Typ.	Max.	Unit
t_1	All	Output Duty Cycle[9]	$t_1 = t_{1A} \div t_{1B}$	45	50	55	%
t_2	CPUCLK	CPU Clock Rising and Falling Edge Rate	Between 0.4V and 2.0V	0.85		4.0	V/ns
t_2	PCICLK	PCI Clock Rising and Falling Edge Rate	Between 0.4V and 2.4V	1.0		4.0	V/ns
t_2	REF, USB	REF Clock Rising and Falling Edge Rate	Between 0.4V and 2.4V	0.5		2.0	V/ns
t_3	CPUCLK	CPU Clock Rise Time	Between 0.4V and 2.0V	0.4		1.6	ns
t_4	CPUCLK	CPU Clock Fall Time	Between 2.0V and 0.4V	0.4		1.6	ns
t_5	CPUCLK	CPU-CPU Clock Skew	Measured at 1.25V		100	175	ps
t_6	CPUCLK, PCICLK	CPU-PCI Clock Skew	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks	1.5		4.0	ns
t_7	PCICLK, PCICLK	PCI-PCI Clock Skew	Measured at 1.5V			250	ps
t_{10}	CPUCLK	Cycle-Cycle Clock Jitter	Measured at 1.25V			550	ps
t_{11}	PCICLK	Cycle-Cycle Clock Jitter	Measured at 1.5V			550	ps
t_{12}	CPUCLK, PCICLK	Power-up Time	CPU and PCI clock stabilization from power-up			3	ms

Notes:
8.   All parameters specified with loaded outputs.
9.   Duty cycle is measured at 1.5V when V_{DD} = 3.3V. When V_{DD} = 2.5V, duty cycle is measured at 1.25V.

Switching Waveforms

Duty Cycle Timing
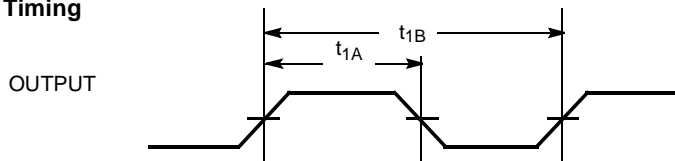
**All Outputs Rise/Fall Time**

CPU-CPU Clock Skew

Switching Waveforms (continued)

CPU-PCI Clock Skew

CPUCLK

PCICLK

t_6

PCI-PCI Clock Skew

PCICLK

PCICLK

t_7

$\overline{CPU\_STOP}$

CPUCLK
(Internal)

PCICLK
(Internal)

PCICLK
(Free-Running)

$\overline{CPU\_STOP}$

CPUCLK
(External)

$\overline{PCI\_STOP}$

CPUCLK
(Internal)

PCICLK
(Internal)

PCICLK
(Free-Running)

$\overline{PCI\_STOP}$

PCICLK
(External)

PWR_DOWN

CPUCLK
(Internal)

PCICLK
(Internal)

PWR_DWN

CPUCLK
(External)

PCICLK
(External)

VCO
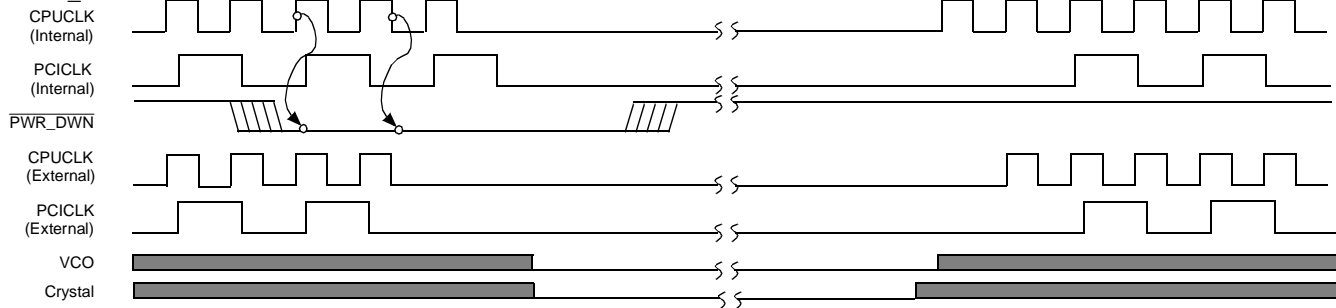
Crystal

Shaded section on the VCO and Crystal waveforms indicates that the VCO and crystal oscillator are active, and there is a valid clock.

Application Information

Clock traces must be terminated with either series or parallel termination, as they are normally done.

Application Circuit

CY2281 28-PIN SSOP
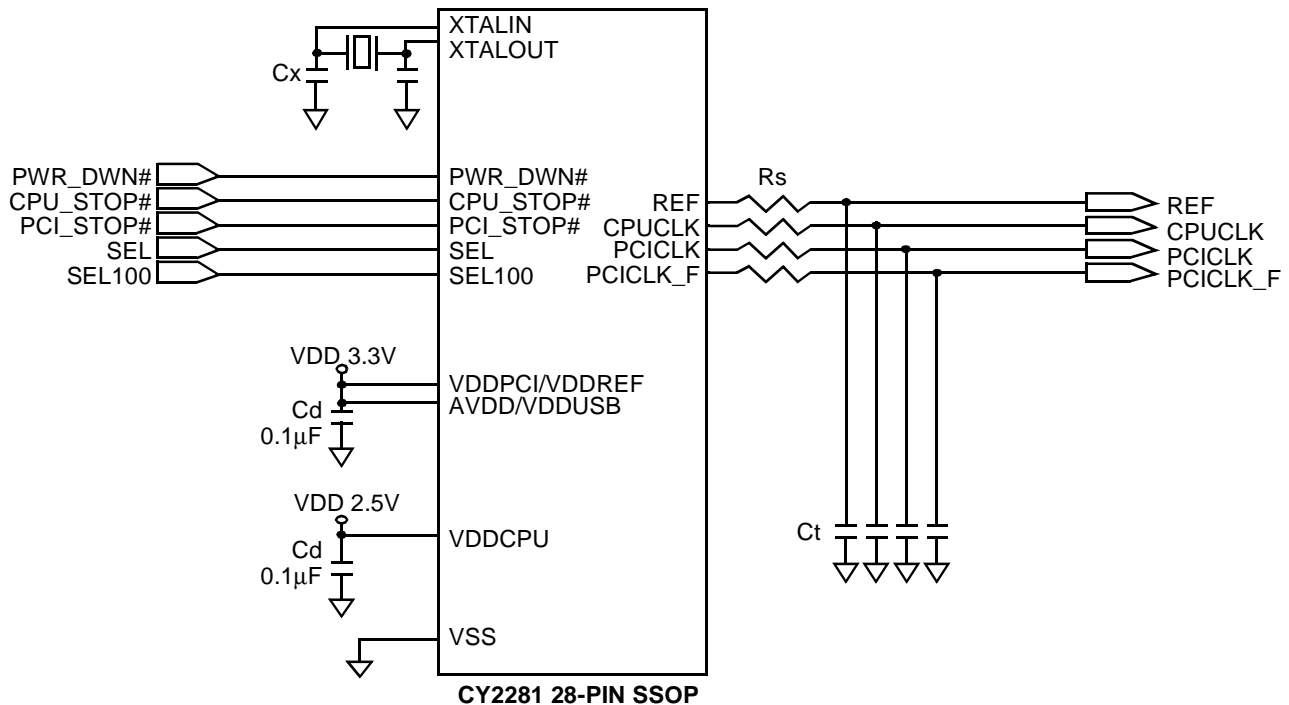
Cd = DECOUPLING CAPACITORS
Ct = OPTIONAL EMI-REDUCING CAPACITORS
Cx = OPTIONAL LOAD MATCHING CAPACITOR
Rs = SERIES TERMINATING RESISTORS

Summary

- A parallel-resonant crystal should be used as the reference to the clock generator. The operating frequency and C_{LOAD} of this crystal should be as specified in the data sheet. Optional trimming capacitors may be needed if a crystal with a different C_{LOAD} is used. Footprints must be laid out for flexibility.

- Surface mount, low-ESR, ceramic capacitors should be used for filtering. Typically, these capacitors have a value of 0.1 μF. In some cases, smaller value capacitors may be required.

- The value of the series terminating resistor satisfies the following equation, where Rtrace is the loaded characteristic impedance of the trace, Rout is the output impedance of the clock generator (specified in the data sheet), and Rseries is the series terminating resistor.

    Rseries > Rtrace – Rout

- Footprints must be laid out for optional EMI-reducing capacitors, which should be placed as close to the terminating resistor as is physically possible. Typical values of these capacitors range from 4.7 pF to 22 pF.

- A Ferrite Bead **may** be used to isolate the Board VDD from the clock generator VDD island. Ensure that the Ferrite Bead offers greater than 50Ω impedance at the clock frequency, under loaded DC conditions. Please refer to the application note "Layout and Termination Techniques for Cypress Clock Generators" for more details.

- If a Ferrite Bead is used, a 10 μF–22 μF tantalum bypass capacitor should be placed close to the Ferrite Bead. This capacitor prevents power supply droop during current surges.

Test Circuit
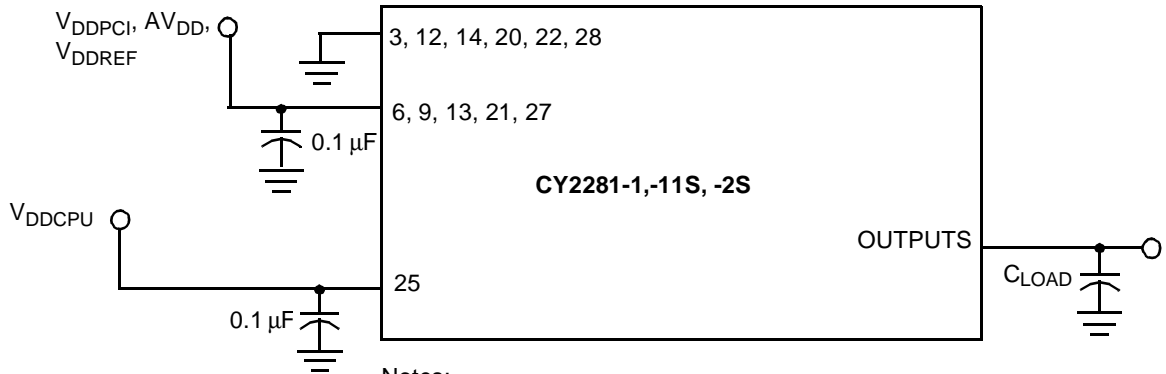
Notes:
Each supply pin must have an individual decoupling capacitor
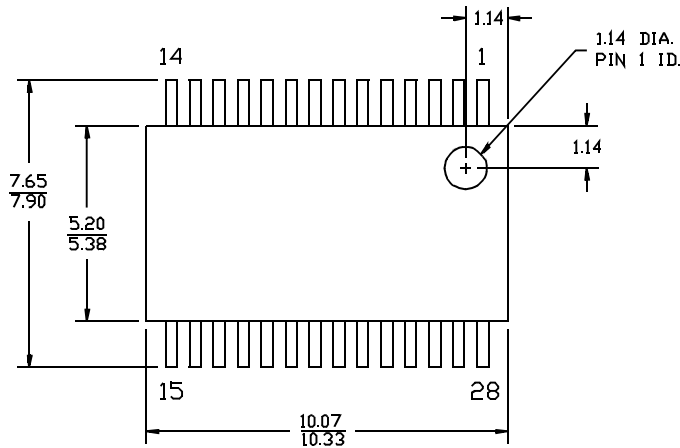All capacitors must be placed as close to the pins as is possible.

Ordering Information

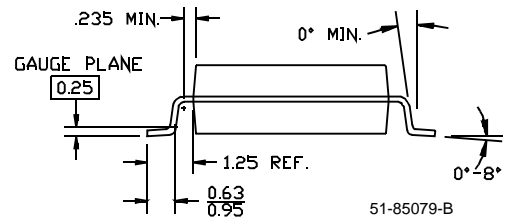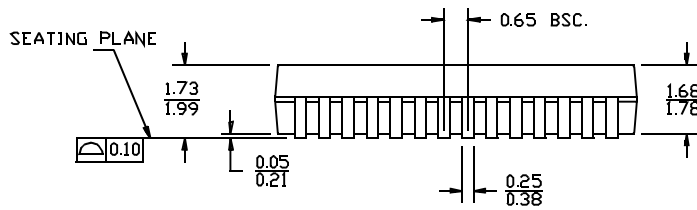| Ordering Code	Package Name	Package Type	Operating Range
CY2281PVC-1	O28	28-Pin SSOP	Commercial
CY2281PVC-11S	O28	28-Pin SSOP	Commercial
CY2281PVC-2S	O28	28-Pin SSOP	Commercial

Document #: 38-00660-C

Package Diagram

28-Lead (210-Mil) Shrunk Small Outline Package O28

DIMENSIONS IN MILLIMETERS $\frac{\text{MIN.}}{\text{MAX.}}$

51-85079-B