

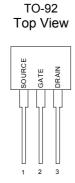
# **GENERAL DESCRIPTION**

This N-Channel enhancement mode field effect transistor is produced using high cell density, DMOS technology. These products have been designed to minimize on-state resistance while provide rugged, reliable, and fast switching performance. It can be used in most applications requiring up to 200mA DC and can deliver pulsed currents up to 500mA. This product is particularly suited for low voltage, low current applications such as small servo motor control, power MOSFET gate drivers, and other switching applications.

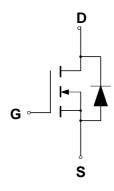
### **FEATURES**

- High Density Cell Design for Low R<sub>DS(ON)</sub>
- ◆ Voltage Controlled Small Signal Switch
- Rugged and Reliable
- ♦ High Saturation Current Capability

### PIN CONFIGURATION



# **SYMBOL**



N-Channel MOSFET

#### ORDERING INFORMATION

Part Number	Package
CMT2N7000	TO-92

# **ABSOLUTE MAXIMUM RATINGS**

Rating		Value	Unit
Drain Source Voltage	$V_{DSS}$	60	V
Drain-Gate Voltage ( $R_{GS}$ = 1.0M $\Omega$ )		60	V
Drain to Current — Continuous		200	mA
- Pulsed	I <sub>DM</sub>	500	
Gate-to-Source Voltage — Continue	$V_{GS}$	±20	V
Non-repetitive	$V_{GSM}$	±40	V
Total Power Dissipation	P <sub>D</sub>	350	mW
Derate above 25℃		2.8	mW/°C
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to 150	$^{\circ}\!\mathbb{C}$
Thermal Resistance — Junction to Ambient	$\theta_{JA}$	357	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds		300	$^{\circ}\!\mathbb{C}$



# **ELECTRICAL CHARACTERISTICS**

Unless otherwise specified,  $T_J = 25^{\circ}C$ .

			CMT2N7000			
Characteristic		Symbol	Min	Тур	Max	Units
Drain-Source Breakdown Voltage		V <sub>(BR)DSS</sub>	60			V
$(V_{GS} = 0 \text{ V}, I_D = 10 \ \mu \text{ A})$						
Drain-Source Leakage Current		I <sub>DSS</sub>				
$(V_{DS} = 48 \text{ V}, V_{GS} = 0 \text{ V})$					1.0	$\mu \mathbf{A}$
$(V_{DS} = 48 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 125^{\circ}\text{C})$					1.0	mA
Gate-Source Leakage Current-Forward		I <sub>GSSF</sub>			-10	nA
$(V_{gsf} = 15 \text{ V}, V_{DS} = 0 \text{ V})$						
Gate Threshold Voltage *		$V_{GS(th)}$	0.8		3.0	V
$(V_{DS} = V_{GS}, I_D = 1.0 \text{ mA})$						
Static Drain-Source On-Resistance *		R <sub>DS(on)</sub>				Ω
$(V_{GS} = 10 \text{ V}, I_D = 0.5\text{A})$					5.0	
Drain-Source On-Voltage *		$V_{DS(on)}$				V
$(V_{GS} = 10 \text{ V}, I_D = 0.5\text{A})$					2.5	
On-State Drain Current *		$I_{d(on)}$	60			mA
$(V_{GS} = 5 \text{ V}, V_{DS} = 10 \text{ V})$						
Forward Transconductance ( $V_{DS} = 10$	) V, I <sub>D</sub> = 200mA) *	<b>g</b> FS	100			mmhos
Input Capacitance	(V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz)	$C_{iss}$			60	pF
Output Capacitance		C <sub>oss</sub>			25	pF
Reverse Transfer Capacitance		C <sub>rss</sub>			5.0	pF
Turn-On Delay Time	$(V_{DD} = 15 \text{ V}, I_D = 500 \text{ mA},$	t <sub>d(on)</sub>			10	ns
Turn-Off Delay Time	$V_{gen}$ = 10 V, $R_{G}$ = 25 $\Omega$ , $R_{L}$ = 30 $\Omega$ ) *	t <sub>d(off)</sub>			10	ns

<sup>\*</sup> Pulse Test: Pulse Width  $\leq$ 300 $\mu$ s, Duty Cycle  $\leq$ 2%



# TYPICAL ELECTRICAL CHARACTERISTICS

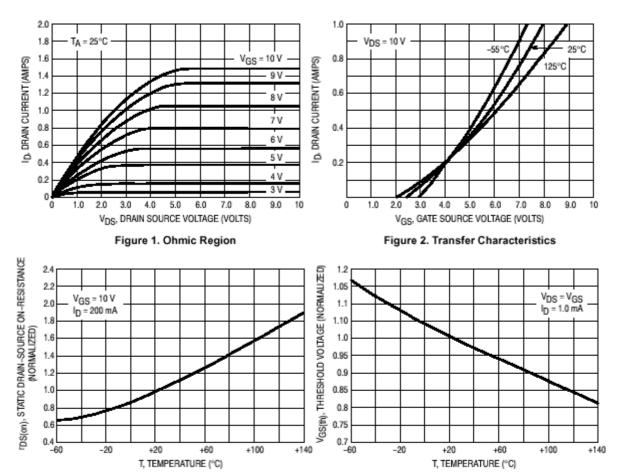
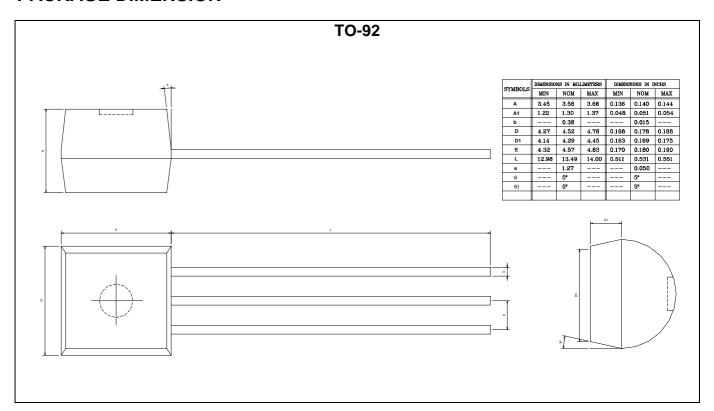


Figure 3. Temperature versus Static Drain-Source On-Resistance

Figure 4. Temperature versus Gate Threshold Voltage



# **PACKAGE DIMENSION**





### **IMPORTANT NOTICE**

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# **HsinChu Headquarter**

# Sales & Marketing

5F, No. 11, Park Avenue II,	11F, No. 306-3, SEC. 1, Ta Tung Road,
Science-Based Industrial Park,	Hsichih, Taipei Hsien 221, Taiwan
HsinChu City, Taiwan	
TEL: +886-3-567 9979	TEL: +886-2-8692 1591
FAX: +886-3-567 9909	FAX: +886-2-8692 1596