

# 2N5060 Series

Preferred Device

## Sensitive Gate Silicon Controlled Rectifiers

### Reverse Blocking Thyristors

Annular PNP devices designed for high volume consumer applications such as relay and lamp drivers, small motor controls, gate drivers for larger thyristors, and sensing and detection circuits. Supplied in an inexpensive plastic TO-226AA (TO-92) package which is readily adaptable for use in automatic insertion equipment.

- Sensitive Gate Trigger Current — 200  $\mu$ A Maximum
- Low Reverse and Forward Blocking Current — 50  $\mu$ A Maximum,  $T_C = 110^\circ\text{C}$
- Low Holding Current — 5 mA Maximum
- Passivated Surface for Reliability and Uniformity
- Device Marking: Logo, Device Type, e.g., 2N5060, Date Code

**MAXIMUM RATINGS** ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage <sup>(1)</sup> ( $T_J = -40$ to $110^\circ\text{C}$ , Sine Wave, 50 to 60 Hz, Gate Open)	$V_{DRM}$ , $V_{RRM}$	30 60 100 200	Volts
On-State Current RMS ( $180^\circ$ Conduction Angles; $T_C = 80^\circ\text{C}$ )	$I_T(\text{RMS})$	0.8	Amp
*Average On-State Current ( $180^\circ$ Conduction Angles) ( $T_C = 67^\circ\text{C}$ ) ( $T_C = 102^\circ\text{C}$ )	$I_T(\text{AV})$	0.51 0.255	Amp
*Peak Non-repetitive Surge Current, $T_A = 25^\circ\text{C}$ (1/2 cycle, Sine Wave, 60 Hz)	$I_{TSM}$	10	Amps
Circuit Fusing Considerations ( $t = 8.3$ ms)	$I^2t$	0.4	$\text{A}^2\text{s}$
*Forward Peak Gate Power (Pulse Width $\leq 1.0$ $\mu\text{sec}$ ; $T_A = 25^\circ\text{C}$ )	$P_{GM}$	0.1	Watt
*Forward Average Gate Power ( $T_A = 25^\circ\text{C}$ , $t = 8.3$ ms)	$P_{G(\text{AV})}$	0.01	Watt
*Forward Peak Gate Current (Pulse Width $\leq 1.0$ $\mu\text{sec}$ ; $T_A = 25^\circ\text{C}$ )	$I_{GM}$	1.0	Amp
*Reverse Peak Gate Voltage (Pulse Width $\leq 1.0$ $\mu\text{sec}$ ; $T_A = 25^\circ\text{C}$ )	$V_{RGM}$	5.0	Volts
*Operating Junction Temperature Range	$T_J$	-40 to +110	$^\circ\text{C}$
*Storage Temperature Range	$T_{\text{stg}}$	-40 to +150	$^\circ\text{C}$

\*Indicates JEDEC Registered Data.

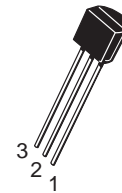
(1)  $V_{DRM}$  and  $V_{RRM}$  for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; however, positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.



**ON Semiconductor**

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**SCRs**  
**0.8 AMPERES RMS**  
**30 thru 200 VOLTS**



TO-92 (TO-226AA)  
CASE 029  
STYLE 10

PIN ASSIGNMENT	
1	Cathode
2	Gate
3	Anode

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

**Preferred** devices are recommended choices for future use and best overall value.

## 2N5060 Series

### THEMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case <sup>(1)</sup>	$R_{\theta JC}$	75	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W
*Lead Solder Temperature (Lead Length $\geq$ 1/16" from case, 10 s Max)	—	+230*	°C

### ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

*Peak Repetitive Forward or Reverse Blocking Current <sup>(2)</sup> ( $V_{AK} = \text{Rated } V_{DRM} \text{ or } V_{RRM}$ )	$I_{DRM}, I_{RRM}$	—	—	10	$\mu\text{A}$
$T_C = 25^\circ\text{C}$		—	—	50	$\mu\text{A}$
$T_C = 110^\circ\text{C}$		—	—	—	—

### ON CHARACTERISTICS

*Peak Forward On-State Voltage <sup>(3)</sup> ( $I_{TM} = 1.2 \text{ A peak @ } T_A = 25^\circ\text{C}$ )	$V_{TM}$	—	—	1.7	Volts
Gate Trigger Current (Continuous dc) <sup>(4)</sup> *( $V_{AK} = 7 \text{ Vdc}, R_L = 100 \text{ Ohms}$ )	$I_{GT}$	—	—	200	$\mu\text{A}$
$T_C = 25^\circ\text{C}$		—	—	350	
$T_C = -40^\circ\text{C}$		—	—	—	—
Gate Trigger Voltage (Continuous dc) <sup>(4)</sup> *( $V_{AK} = 7 \text{ Vdc}, R_L = 100 \text{ Ohms}$ )	$V_{GT}$	—	—	0.8	Volts
$T_C = 25^\circ\text{C}$		—	—	1.2	
$T_C = -40^\circ\text{C}$		—	—	—	—
*Gate Non-Trigger Voltage ( $V_{AK} = \text{Rated } V_{DRM}, R_L = 100 \text{ Ohms}$ )	$V_{GD}$	0.1	—	—	Volts
$T_C = 110^\circ\text{C}$		—	—	—	—
Holding Current <sup>(4)</sup> *( $V_{AK} = 7 \text{ Vdc}, \text{ initiating current} = 20 \text{ mA}$ )	$I_H$	—	—	5.0	mA
$T_C = 25^\circ\text{C}$		—	—	10	
$T_C = -40^\circ\text{C}$		—	—	—	—
Turn-On Time Delay Time	$t_d$	—	3.0	—	$\mu\text{s}$
Rise Time	$t_r$	—	0.2	—	
( $I_{GT} = 1 \text{ mA}, V_D = \text{Rated } V_{DRM},$ Forward Current = 1 A, $di/dt = 6 \text{ A}/\mu\text{s}$ )					
Turn-Off Time (Forward Current = 1 A pulse, Pulse Width = 50 $\mu\text{s}$ , 0.1% Duty Cycle, $di/dt = 6 \text{ A}/\mu\text{s}$ , $dv/dt = 20 \text{ V}/\mu\text{s}, I_{GT} = 1 \text{ mA}$ )	$t_q$	—	10	—	$\mu\text{s}$
2N5060, 2N5061		—	30	—	
2N5062, 2N5064		—	—	—	—

### DYNAMIC CHARACTERISTICS

Critical Rate of Rise of Off-State Voltage (Rated $V_{DRM}$ , Exponential)	$dv/dt$	—	30	—	$\text{V}/\mu\text{s}$
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\*Indicates JEDEC Registered Data.

(1) This measurement is made with the case mounted "flat side down" on a heat sink and held in position by means of a metal clamp over the curved surface.

(2)  $R_{GK} = 1000 \Omega$  is included in measurement.

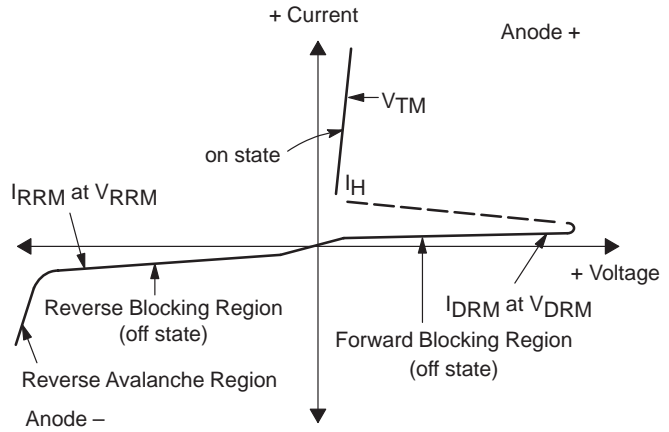
(3) Forward current applied for 1 ms maximum duration, duty cycle  $\leq$  1%.

(4)  $R_{GK}$  current is not included in measurement.

# 2N5060 Series

## Voltage Current Characteristic of SCR

Symbol	Parameter
$V_{DRM}$	Peak Repetitive Off State Forward Voltage
$I_{DRM}$	Peak Forward Blocking Current
$V_{RRM}$	Peak Repetitive Off State Reverse Voltage
$I_{RRM}$	Peak Reverse Blocking Current
$V_{TM}$	Peak on State Voltage
$I_H$	Holding Current



## CURRENT DERATING

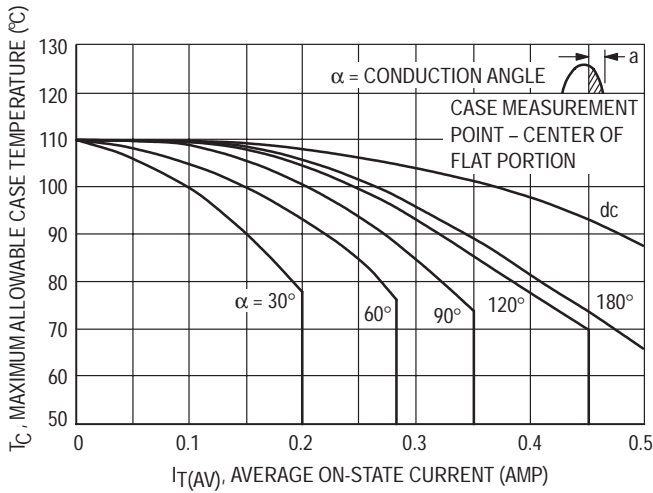


Figure 1. Maximum Case Temperature

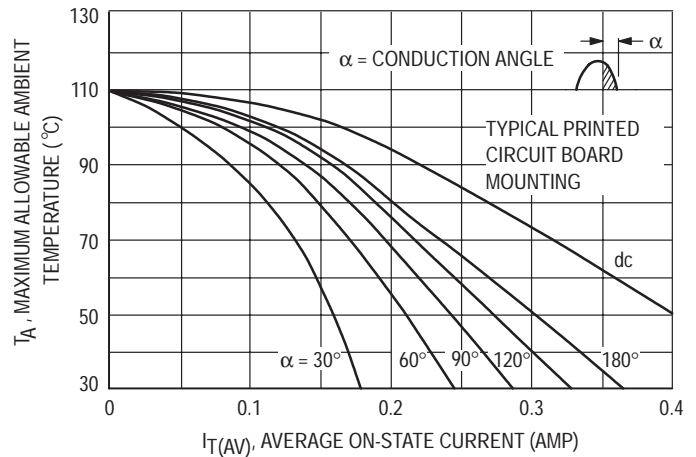


Figure 2. Maximum Ambient Temperature

# 2N5060 Series

## CURRENT DERATING

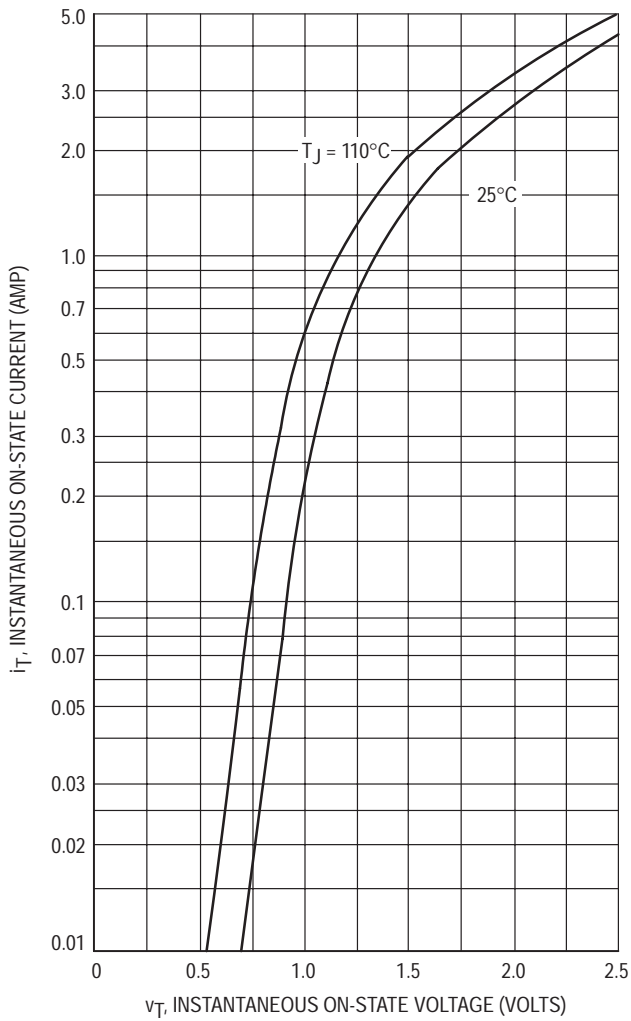


Figure 3. Typical Forward Voltage

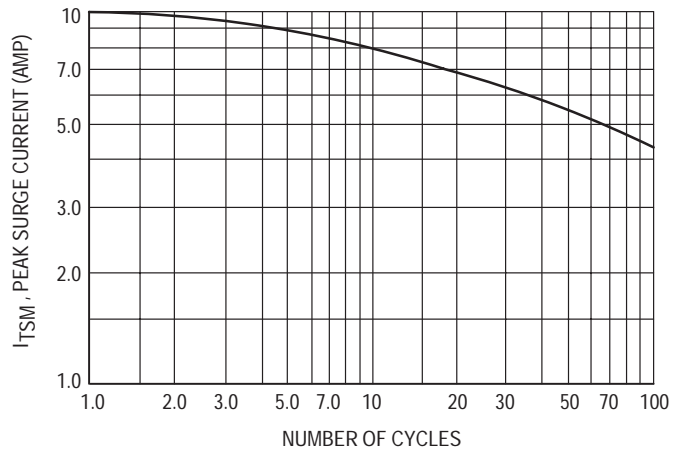


Figure 4. Maximum Non-Repetitive Surge Current

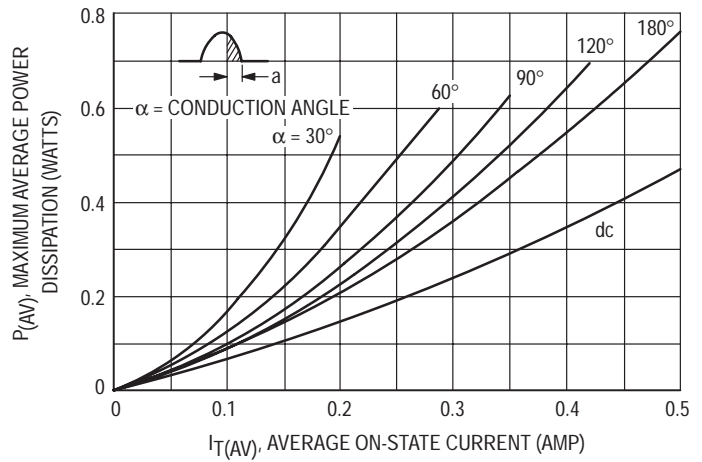


Figure 5. Power Dissipation

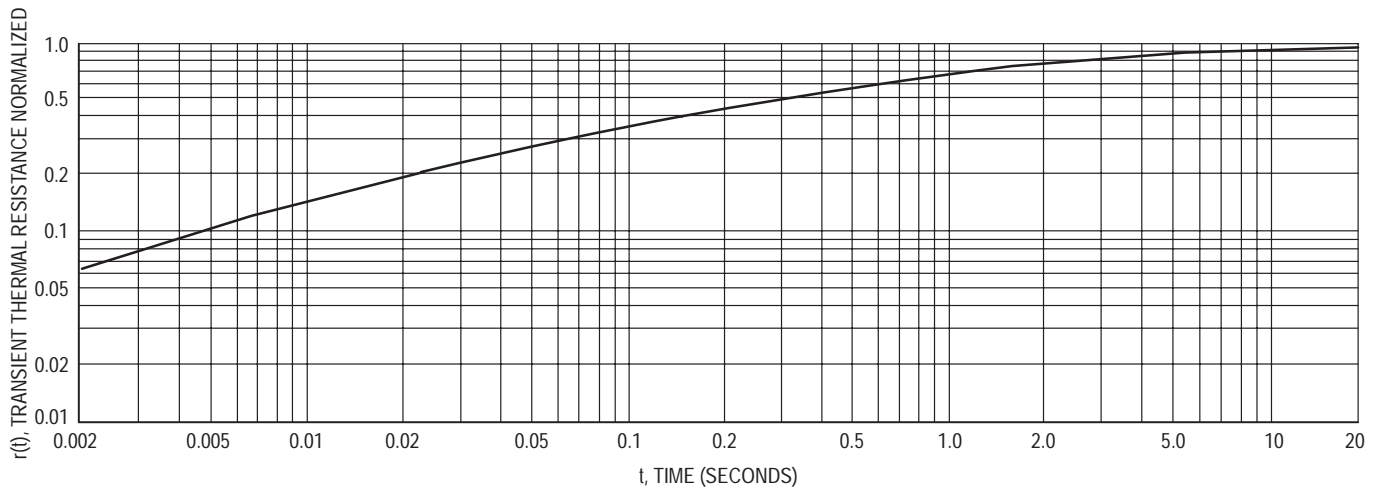


Figure 6. Thermal Response

# 2N5060 Series

## TYPICAL CHARACTERISTICS

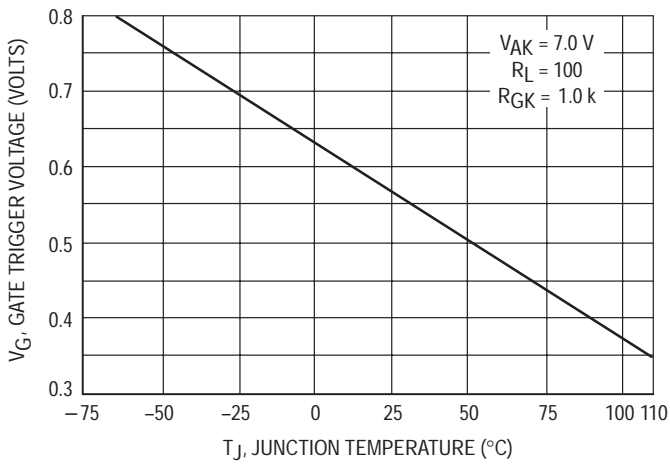


Figure 7. Typical Gate Trigger Voltage

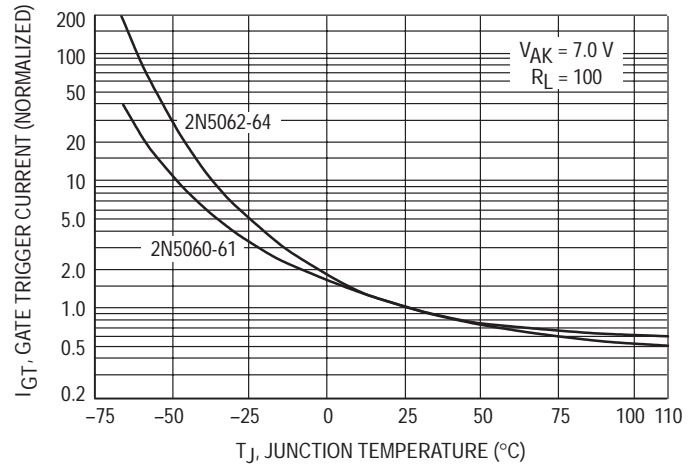


Figure 8. Typical Gate Trigger Current

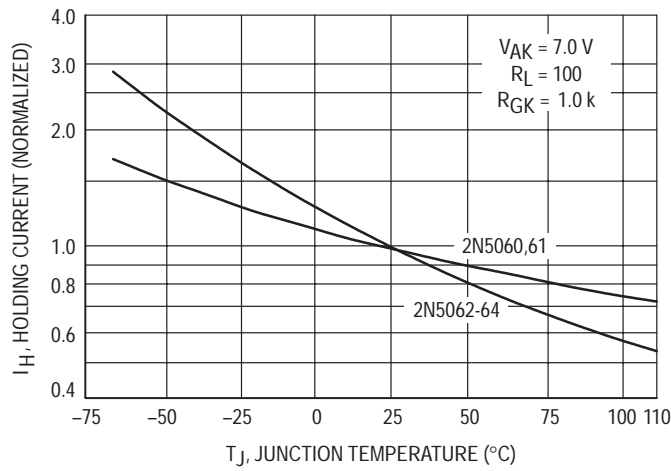


Figure 9. Typical Holding Current

## 2N5060 Series

### TO-92 EIA RADIAL TAPE IN FAN FOLD BOX OR ON REEL

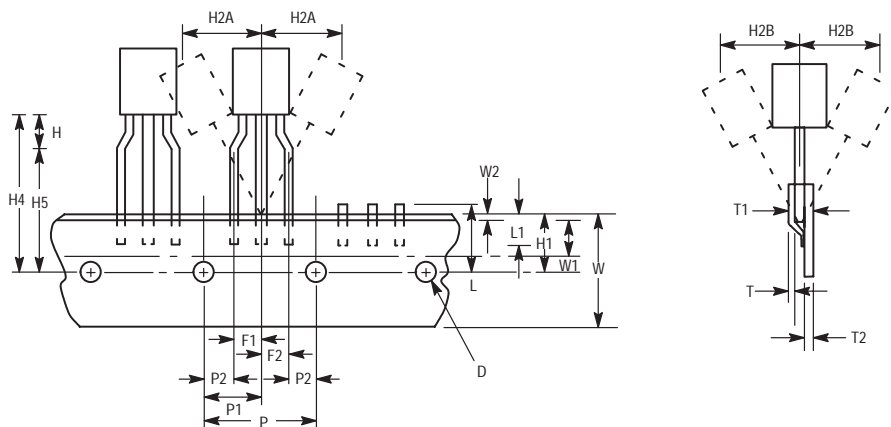


Figure 10. Device Positioning on Tape

Symbol	Item	Specification			
		Inches		Millimeter	
		Min	Max	Min	Max
D	Tape Feedhole Diameter	0.1496	0.1653	3.8	4.2
D2	Component Lead Thickness Dimension	0.015	0.020	0.38	0.51
F1, F2	Component Lead Pitch	0.0945	0.110	2.4	2.8
H	Bottom of Component to Seating Plane	.059	.156	1.5	4.0
H1	Feedhole Location	0.3346	0.3741	8.5	9.5
H2A	Deflection Left or Right	0	0.039	0	1.0
H2B	Deflection Front or Rear	0	0.051	0	1.0
H4	Feedhole to Bottom of Component	0.7086	0.768	18	19.5
H5	Feedhole to Seating Plane	0.610	0.649	15.5	16.5
L	Defective Unit Clipped Dimension	0.3346	0.433	8.5	11
L1	Lead Wire Enclosure	0.09842	—	2.5	—
P	Feedhole Pitch	0.4921	0.5079	12.5	12.9
P1	Feedhole Center to Center Lead	0.2342	0.2658	5.95	6.75
P2	First Lead Spacing Dimension	0.1397	0.1556	3.55	3.95
T	Adhesive Tape Thickness	0.06	0.08	0.15	0.20
T1	Overall Taped Package Thickness	—	0.0567	—	1.44
T2	Carrier Strip Thickness	0.014	0.027	0.35	0.65
W	Carrier Strip Width	0.6889	0.7481	17.5	19
W1	Adhesive Tape Width	0.2165	0.2841	5.5	6.3
W2	Adhesive Tape Position	.0059	0.01968	.15	0.5

NOTES:

1. Maximum alignment deviation between leads not to be greater than 0.2 mm.
2. Defective components shall be clipped from the carrier tape such that the remaining protrusion (L) does not exceed a maximum of 11 mm.
3. Component lead to tape adhesion must meet the pull test requirements.
4. Maximum non-cumulative variation between tape feed holes shall not exceed 1 mm in 20 pitches.
5. Holddown tape not to extend beyond the edge(s) of carrier tape and there shall be no exposure of adhesive.
6. No more than 1 consecutive missing component is permitted.
7. A tape trailer and leader, having at least three feed holes is required before the first and after the last component.
8. Splices will not interfere with the sprocket feed holes.

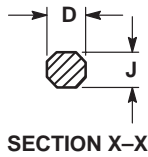
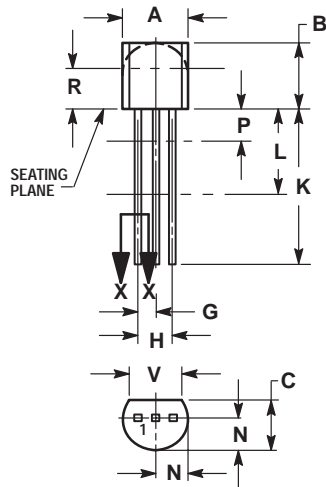
# 2N5060 Series

## ORDERING & SHIPPING INFORMATION: 2N5060 Series packaging options, Device Suffix

U.S.	Europe Equivalent	Shipping	Description of TO92 Tape Orientation
2N5060,61,62,64 2N5060,61,62,64RLRA 2N5060,64RLRM	2N5060RL1	Bulk in Box (5K/Box) Radial Tape and Reel (2K/Reel) Radial Tape and Fan Fold Box (2K/Box)	N/A, Bulk Round side of TO92 and adhesive tape visible Flat side of TO92 and adhesive tape visible

## PACKAGE DIMENSIONS

### TO-92 (TO-226AA) CASE 029-11 ISSUE AJ



#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.115	---	2.93	---
V	0.135	---	3.43	---

#### STYLE 10:

- PIN 1. CATHODE
- GATE
- ANODE

## 2N5060 Series

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