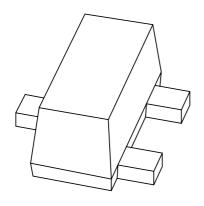
DISCRETE SEMICONDUCTORS

DATA SHEET



PDTA143TEF

PNP resistor-equipped transistor; R1 = 4.7 k Ω , R2 = open

Product specification

2002 Jan 15





PNP resistor-equipped transistor; R1 = 4.7 k Ω , R2 = open

PDTA143TEF

FEATURES

- Built-in bias resistors
- · Simplification of circuit design
- Reduces number of components and required PCB area.

APPLICATIONS

- Especially suitable for space reduction in interface and driver circuits
- Inverter configurations without use of external resistors.

DESCRIPTION

PNP resistor equipped transistor in a SOT490 (SC-89) plastic package.

MARKING

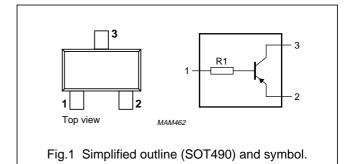
TYPE NUMBER	MARKING CODE		
PDTA143TEF	10		

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V _{CEO}	collector-emitter voltage	-50	V
Io	output current (DC)	-100	mA
R1	bias resistor	4.7	kΩ
R2	open	_	_

PINNING

PIN	DESCRIPTION	
1	base/input	
2	emitter/ground (+)	
3	collector/output	



1 — 3

MGA893 - 1

Fig.2 Equivalent inverter symbol.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CBO}	collector-base voltage	open emitter	_	-50	V
V _{CEO}	collector-emitter voltage	open base	_	-50	V
V _{EBO}	emitter-base voltage	open collector	_	-10	V
Vi	input voltage				
	positive		_	+10	V
	negative		_	-40	V
Io	output current (DC)		_	-100	mA
I _{CM}	peak collector current		_	-100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C; note 1	_	250	mW
T _{stg}	storage temperature		-65	+150	°C
Tj	junction temperature		_	150	°C
T _{amb}	operating ambient temperature		-65	+150	°C

Note

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th j-a}	thermal resistance from junction to ambient	in free air; note 1	500	K/W

Note

1. For mounting conditions, see "Thermal considerations and footprint design for SOT490 in the SC18 Data Handbook".

^{1.} For mounting conditions, see "Thermal considerations and footprint design for SOT490 in the SC18 Data Handbook".

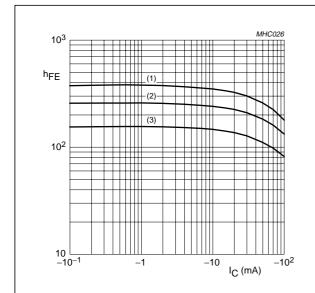
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CHARACTERISTICS

 T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I _{CBO}	collector-base cut-off current	$V_{CB} = -50 \text{ V}; I_E = 0$	_	_	-100	nA
I _{CEO}	collector-emitter cut-off current	$V_{CE} = -30 \text{ V}; I_{B} = 0$	_	_	-1	μΑ
		$V_{CE} = -30 \text{ V}; I_{B} = 0; T_{j} = 150 ^{\circ}\text{C}$	_	_	-50	μΑ
I _{EBO}	emitter-base cut-off current	$V_{EB} = -5 \text{ V}; I_C = 0$	_	_	-100	nA
h _{FE}	DC current gain	$V_{CE} = -5 \text{ V}; I_{C} = -1 \text{ mA}$	200	_	_	
V _{CEsat}	collector-emitter saturation voltage	$I_C = -5 \text{ mA}; I_B = -0.25 \text{ mA}$	_	_	-100	mV
R1	input resistor		3.3	4.7	6.1	kΩ
C _c	collector capacitance	$I_E = i_e = 0$; $V_{CB} = -10 \text{ V}$; $f = 1 \text{ MHz}$	_	_	3	рF



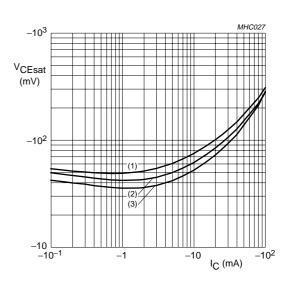
 $V_{CE} = -5 \text{ V}.$

(1) $T_{amb} = 100 \, ^{\circ}C$.

(2) $T_{amb} = 25 \, ^{\circ}C$.

(3) $T_{amb} = -40 \, ^{\circ}C$.

Fig.3 DC current gain as a function of collector current; typical values.



 $I_{\rm C}/I_{\rm B}=20.$

(1) $T_{amb} = 100 \, ^{\circ}C$.

(2) $T_{amb} = 25 \, ^{\circ}C$.

(3) $T_{amb} = -40 \, ^{\circ}C$.

Fig.4 Collector-emitter saturation voltage as a function of collector current; typical values.

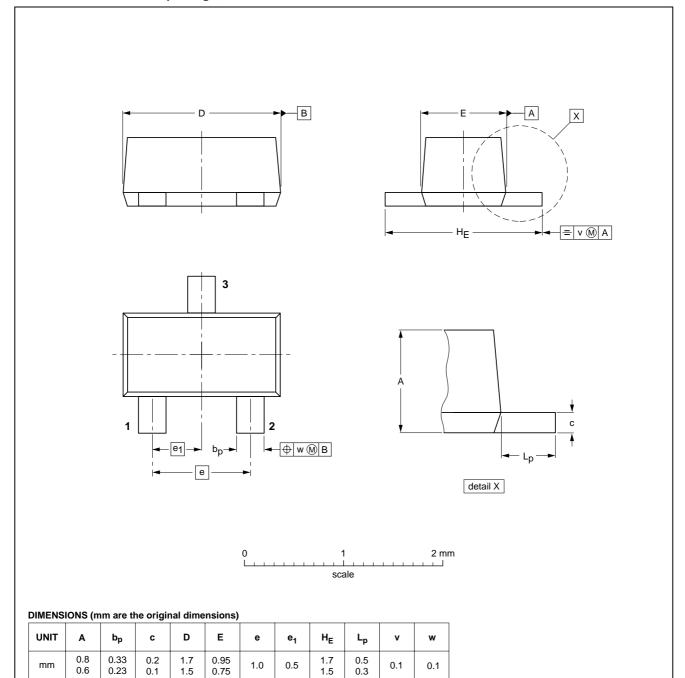
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PACKAGE OUTLINE

Plastic surface mounted package; 3 leads

SOT490



OUTLINE	REFERENCES		EUROPEAN	ICCUE DATE		
VERSION	IEC	JEDEC	EIAJ		PROJECTION ISSUE DAT	
SOT490			SC-89			98-10-23

PNP resistor-equipped transistor; R1 = $4.7 \text{ k}\Omega$, R2 = open

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DATA SHEET STATUS(1)	PRODUCT STATUS ⁽²⁾	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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