OKI Semiconductor

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MSM6688/6688L

ADPCM Solid-State Recorder IC

GENERAL DESCRIPTION

The MSM6688/6688L is a "solid-state recorder" IC developed using the ADPCM method. By externally connecting a microphone, a speaker, a speaker drive amplifier, and a dedicated register to store ADPCM data, it can record and play back voice data in a manner similar to a tape recorder.
The MSM6688 supports 5 V operation and has a stand-alone mode and a microcontroller interface mode.
The MSM6688L supports 3 V operation and controls recording/playback in microcontroller interface mode.
In the stand-alone mode, recording/playback conditions can be selected by pins and the MSM6688/6688L can be controlled by a simple drive timing. In the microcontroller interface mode, recording/playback can be controlled by commands from the microcontroller. In the microcontroller interface mode, the MSM6688/6688L is much more flexible than in the stand-alone mode.
In addition, the MSM6688/6688L can form easily a recording and playback circuit with fixed messages by connecting serial registers and serial voice ROMs as external memories.

Note: This data sheet explains a stand-alone mode and a microcontroller interface mode, separately.

Differences Between MSM6688 and MSM6688L

Parameter	MSM6688	MSM6688L
Operating voltage	3.5 to 5.5 V	2.7 to 3.6 V
Control mode	Standalone mode, Microcontroller interface mode	Microcontroller interface mode only
Full scale of A/D and D/A converters	0 to V_{DD}	$\frac{1}{4} V_{DD}$ to $\frac{3}{4} V_{DD}$
Voice detection level for voice triggered starting	$\pm\frac{V_{DD}}{64}$, $\pm\frac{V_{DD}}{32}$, $\pm\frac{V_{DD}}{16}$	$\pm\frac{V_{DD}}{128}$, $\pm\frac{V_{DD}}{64}$, $\pm\frac{V_{DD}}{32}$
External-only register	32M bits (max.) 4M bits (MSM6684B) 8M bits (MSM6685A)	4M bits (max.) 4M bits (MSM66V84B)

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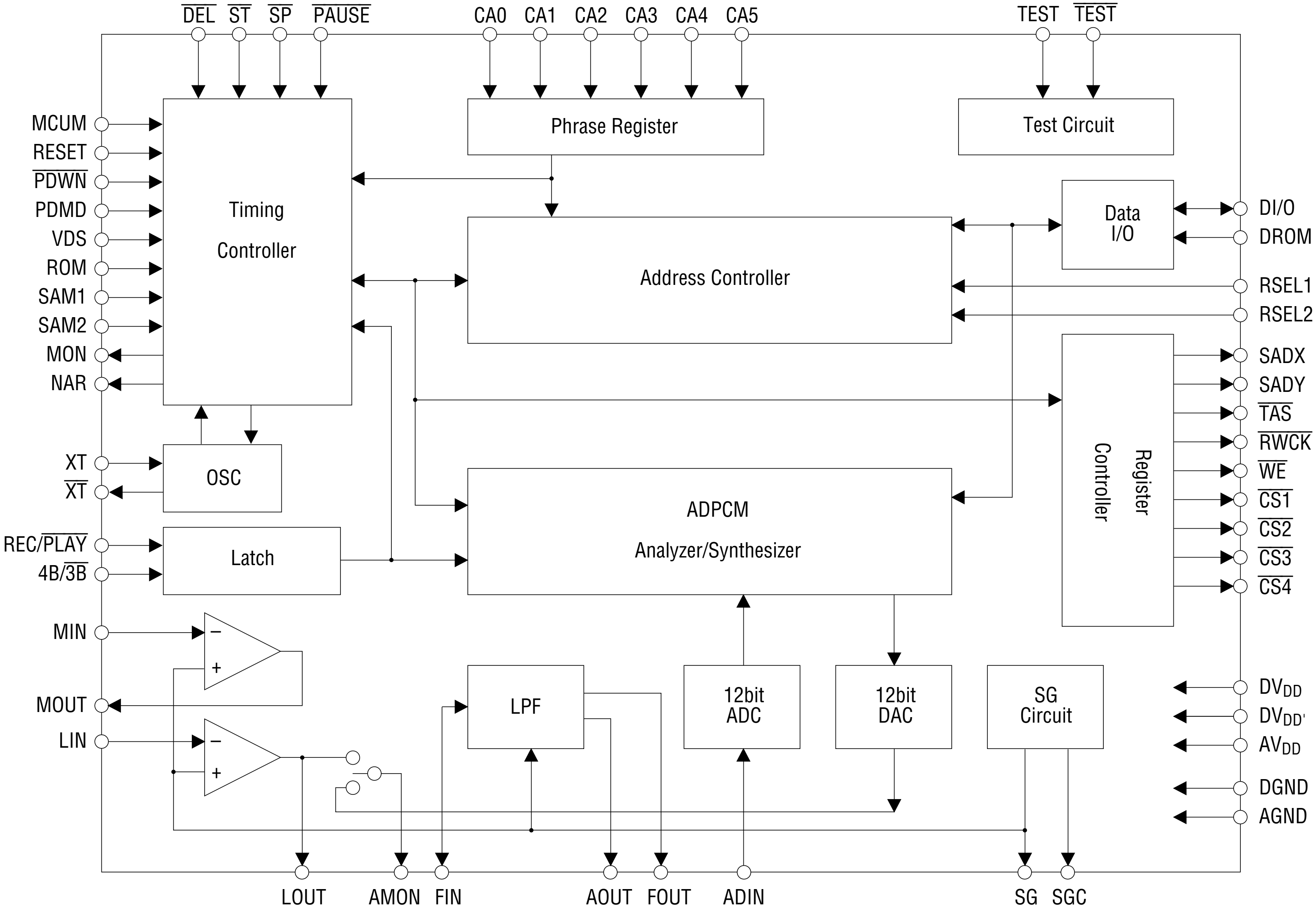
(1) STAND-ALONE MODE (for MSM6688 (5 V Version))

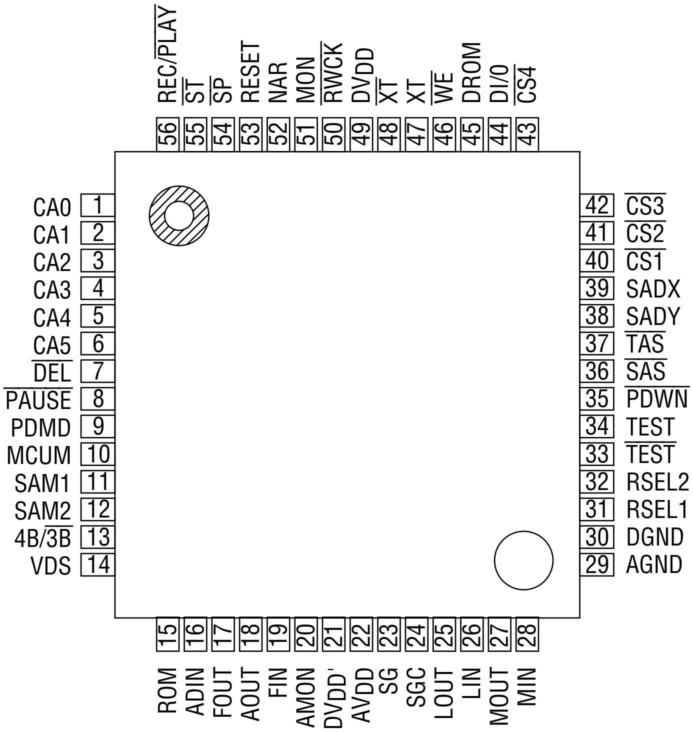
FEATURES

- 3-bit or 4-bit ADPCM
- Built-in 12-bit AD converter
- Built-in12-bit DA converter
- Built-in microphone amplifier
- Built-in low-pass filter
  Attenuation characteristics –40 dB/oct
- External memories
  Serial registers, 32M bits maximum (for variable messages)
    8M bit serial register (MSM6685A) can be driven directly
  Serial voice ROMs, 4M bits maximum (for fixed messages)
    1M bit serial voice ROM (MSM6595A) can be driven directly
    2M bit serial voice ROM (MSM6596A) can be driven directly
    3M bit serial voice ROM (MSM6597A) can be driven directly
- Sampling frequency
  4.0 kHz, 5.3 kHz, 6.4 kHz or 8.0 kHz (master clock frequency = 4.096 MHz)
  8.0 kHz, 10.6 kHz, 12.8 kHz, or 16.0 kHz (master clock frequency = 8.192 MHz)
- Number of phrases
  63 phrases for variable messages
  63 phrases for fixed messages
- Maximum recording time (when external 32M bit RAM is connected)
  34 minutes (for 16 kbps ADPCM)
  23 minutes (for 24 kbps ADPCM)
  17 minutes (for 32 kbps ADPCM)
- Voice triggered starting function
- Pause function
- Master clock frequency: 4.096 MHz~8.192 MHz
- Power supply voltage: Single 5 V power supply
- Package:
  56-pin plastic QFP (QFP56-P-910-0.65-2K) (Product name: MSM6688GS-2K)

BLOCK DIAGRAM


DEL
ST
SP
PAUSE
CA0
CA1
CA2
CA3
CA4
CA5
TEST
TEST
MCUM
RESET
PDWN
PDMD
VDS
ROM
SAM1
SAM2
MON
NAR
Timing Controller
Phrase Register
Test Circuit
Data I/O
Address Controller
DI/O
DROM
RSEL1
RSEL2
Register Controller
SADX
SADY
TAS
RWCK
WE
CS1
CS2
CS3
CS4
XT
XT
OSC
REC/PLAY
4B/3B
Latch
ADPCM Analyzer/Synthesizer
MIN
MOUT
LIN
LPF
12bit ADC
12bit DAC
SG Circuit
DVDD
DVDD'
AVDD
DGND
AGND
LOUT
AMON
FIN
AOUT
FOUT
ADIN
SG
SGC

PIN CONFIGURATION (TOP VIEW)


CA0 1
CA1 2
CA2 3
CA3 4
CA4 5
CA5 6
DEL 7
PAUSE 8
PDMD 9
MCUM 10
SAM1 11
SAM2 12
4B/3B 13
VDS 14
15 ROM
16 ADIN
17 FOUT
18 AOUT
19 FIN
20 AMON
21 DVDD'
22 AVDD
23 SG
24 SGC
25 LOUT
26 LIN
27 MOUT
28 MIN
29 AGND
30 DGND
31 RSEL1
32 RSEL2
33 TEST
34 TEST
35 PDWN
36 SAS
37 TAS
38 SADY
39 SADX
40 CS1
41 CS2
42 CS3
43 CS4
44 DI/0
45 DROM
46 WE
47 XT
48 XT
49 DVDD
50 RWCK
51 MON
52 NAR
53 RESET
54 SP
55 ST
56 REC/PLAY

56-Pin Plastic QFP

PIN DESCRIPTIONS

Pin	Symbol	Type	Description
49	DV_{DD}	—	Digital power supply pin. Insert a bypass capacitor of 0.1μF or more between this pin and the DGND pin.
21	$DV_{DD'}$	—	Digital power supply pin
22	AV_{DD}	—	Analog power supply pin. Insert a bypass capacitor of 0.1μF or more between this pin and the AGND pin.
30	DGND	—	Digital ground pin
29	AGND	—	Analog ground pin
23 24	SG SGC	O	Output pin for analog circuit reference voltage (signal ground)
28 26	MIN LIN	I	Inverting input pin of the built-in OP amplifier. Non-inverting input pin is internally connected to SG (signal ground).
27 25	MOUT LOUT	O	MOUT and LOUT are output pins of the built-in OP amplifier for MIN and LIN, respectively.
20	AMON	O	This pin is connected to the LOUT pin in the recording mode and to the DA converter output in the playback mode. Used to connect the built-in LPF input (FIN pin).
19	FIN	I	Input pin of the built-in LPF.
17	FOUT	O	Output pin of the built-in LPF. Used to connect the AD converter input (ADIN pin).
16	ADIN	I	Input pin of the built-in 12-bit AD converter.
18	AOUT	O	Output pin of the built-in LPF. This pin outputs playback waveforms and used to connect an external speaker drive amplifier.
39 38	SADX SADY	O	(Serial Address Data). SADX is used to connect the SAD pin of each external serial register and the SADX pin of each external serial voice ROM. SADY is used to connect the SADY pin of each external serial voice ROM. Outputs of starting address of read/write.
36	$\overline{\text{SAS}}$	O	(Serial Address Strobe). Used to connect the $\overline{\text{SAS}}$ pin of external serial register and the $\overline{\text{SASX}}$ and $\overline{\text{SASY}}$ pins of external serial voice ROM. Clock pin to write the serial address.
37	$\overline{\text{TAS}}$	O	(Transfer Address Strobe). Used to connect the $\overline{\text{TAS}}$ pin of each external serial register and serial voice ROM. This pin outputs address strobe outputs to set the serial address data from the SADX and SADY pins into the internal address counter of each serial register and serial voice ROM.
50	$\overline{\text{RWCK}}$	O	(Read/Write Clock). Used to connect the $\overline{\text{RWCK}}$ pin of each external serial register and the $\overline{\text{RDCK}}$ pin of each external serial voice ROM. This pin outputs a clock to read data from or write it into each external serial register.
46	$\overline{\text{WE}}$	O	(Write Enable) Used to connect the $\overline{\text{WE}}$ pin of each external serial register. This pin outputs $\overline{\text{WE}}$ signal to select either read or write mode.

<table>
<tr><th>Pin</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>44</td><td>DI/O</td><td>I/O</td><td>(Data I/O). Used to connect the DIN and DOUT pins of serial register. This pin outputs the data to be written into the serial register or inputs the data read from the serial registers.</td></tr>
<tr><td>45</td><td>DROM</td><td>I</td><td>(Data ROM). Used to connect the DOUT pin of each external serial voic ROM.</td></tr>
<tr><td>40
41
42
43</td><td>$\overline{\text{CS1}}$
$\overline{\text{CS2}}$
$\overline{\text{CS3}}$
$\overline{\text{CS4}}$</td><td>O</td><td>(Chip Select). Used to connect the $\overline{\text{CS}}$ pin of serial register and the $\overline{\text{CS}}$ ($\overline{\text{CS1}}$, $\overline{\text{CS2}}$, $\overline{\text{CS3}}$) pins of serial voice ROM.</td></tr>
<tr><td>31
32</td><td>RSEL1
RSEL2</td><td>I</td><td>(Register Select). These are used to select the number of external serial registers.
<table>
<tr><td>RSEL2</td><td>L</td><td>L</td><td>H</td><td>H</td></tr>
<tr><td>RSEL1</td><td>L</td><td>H</td><td>L</td><td>H</td></tr>
<tr><td>Number of serial registers</td><td>1</td><td>2</td><td>3</td><td>4</td></tr>
</table></td></tr>
<tr><td>10</td><td>MCUM</td><td>I</td><td>This pin is used to select either the stand-alone mode or the microcontroller interface mode.
Low level: Stand-alone mode
High level: Microcontroller interface mode.</td></tr>
<tr><td>53</td><td>RESET</td><td>I</td><td>A high input level to this pin causes the MSM6688 to be initialized and to go into the power down state.</td></tr>
<tr><td>35</td><td>$\overline{\text{PDWN}}$</td><td>I</td><td>(Power Down). When a low level is input to this pin, the MSM6688 goes to the power down state. Unlike the RESET pin, this pin does not force to reset the MSM6688. When an Low level is applied to this $\overline{\text{PDWN}}$ pin during recording operation, the MSM6688 is halted, and will be maintained in the power down state while PDWN is low. After this pin is restored to a high level, postprocessing for recording will be performed.</td></tr>
<tr><td>47</td><td>XT</td><td>I</td><td>Used to connect an oscillator. When an external clock is used, input the clock through this pin. At the power down state, this pin must be set to the ground level.</td></tr>
<tr><td>48</td><td>$\overline{\text{XT}}$</td><td>O</td><td>Used to connect an oscillator, when an external clock is used, this pin must be left open.</td></tr>
<tr><td>34
33</td><td>TEST
$\overline{\text{TEST}}$</td><td>I</td><td>Used to test the MSM6688. Input a low level to the TEST pin and a high level to the $\overline{\text{TEST}}$ pin.</td></tr>
</table>

<table>
<tr><th>Pin</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>15</td><td>ROM</td><td>I</td><td>When low, selects the record/playback operation. When high, selects the ROM playback operation.</td></tr>
<tr><td>56</td><td>REC/$\overline{\text{PLAY}}$</td><td>I</td><td>Used to select the recording mode or the playback mode. This pin is invalid during the ROM playback operation. When low, selects the playback mode. When high, selects the recording mode.</td></tr>
<tr><td>55</td><td>$\overline{\text{ST}}$</td><td>I</td><td>When a low-level pulse is applied to this pin, the record/playback or ROM playback is started.</td></tr>
<tr><td>54</td><td>$\overline{\text{SP}}$</td><td>I</td><td>When a low-level pulse is applied to this pin, the record/playback or ROM playback is stopped.</td></tr>
<tr><td>8</td><td>$\overline{\text{PAUSE}}$</td><td>I</td><td>When a low-level pulse is applied to this pin, the record/playback or ROM operation is stopped temporarily.</td></tr>
<tr><td>7</td><td>$\overline{\text{DEL}}$</td><td>I</td><td>When a low level pulse is applied to this pin, all phase deletion or specified phrase deletion can be performed according to the setting of pins CA0 through CA5,
ch00: All phase deletion
ch01 to ch3F: Specified phrase deletion
After powering up, be sure to input RESET signal and then to delete all phrases. After completing this procedure, start the record/playback operation.</td></tr>
<tr><td>1-6</td><td>CA0-CA5</td><td>I</td><td>Input pins used to specify desired phases.
A total of 63 phrases can be specified independently for the record/playback operation and the ROM playback operation.
<table>
<tr><th>CA5</th><th>CA4</th><th>CA3</th><th>CA2</th><th>CA1</th><th>CA0</th><th>Phrase No.</th><th>Remarks</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>ch00</td><td>All phrase deletion</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>H</td><td>ch01</td><td rowspan="5">A total of 63 phrases can be used both for record/playback and ROM playback operation.</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>L</td><td>H</td><td>L</td><td>ch02</td></tr>
<tr><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>L</td><td>ch3E</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>ch3F</td></tr>
</table>
</td></tr>
<tr><td>13</td><td>4B/$\overline{\text{3B}}$</td><td>I</td><td>Input pin used to select one of two types of ADPCM bit length.
When low, selects the 3-bit ADPCM.
When high, selects the 4-bit ADPCM.</td></tr>
</table>

<table>
<tr><th>Pin</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>11
12</td><td>SAM1
SAM2</td><td>I</td><td>Used to select one of the following four types of sampling frequency. The relationship between the master clock frequency (fosc) and the sampling frequency (fsamp) is shown below. Values in parentheses denote the sampling frequencies for fosc = 4.096 MHz.
<table>
<tr><td>SAM2</td><td>L</td><td>L</td><td>H</td><td>H</td></tr>
<tr><td>SAM1</td><td>L</td><td>H</td><td>L</td><td>H</td></tr>
<tr><td>fsamp</td><td>$\frac{\text{fosc}}{1024}$
(4.0kHz)</td><td>$\frac{\text{fosc}}{768}$
(5.3kHz)</td><td>$\frac{\text{fosc}}{640}$
(6.4kHz)</td><td>$\frac{\text{fosc}}{512}$
(8.0kHz)</td></tr>
</table></td></tr>
<tr><td>9</td><td>PDMD</td><td>I</td><td>This input pin is used to select the condition for transition to the power-down state.
Low level: The MSM6688 automatically goes to the power-down state, excepting the time the record/playback operation is being performed.
High level: The MSM6688 automatically goes to the standby state, instead of the power-down state, excepting the time the record/playback operation is being performed. In this case, the MSM6688 can be placed in the power-down state by setting the RESET pin to a high level. If it is desired to use the built-in LPF for an external circuit, this standby mode must be selected by applying a high level to the PDMD pin.</td></tr>
<tr><td>14</td><td>VDS</td><td>I</td><td>Used to select the voice triggered starting that starts recording when the voice input exceeds the preset amplitude. A high input level on this pin enables the voice triggered starting circuit.</td></tr>
<tr><td>51</td><td>MON</td><td>O</td><td>Outputs a high level while the record/playback operation is being performed.</td></tr>
<tr><td>52</td><td>NAR</td><td>O</td><td>Output pin to indicate the enable or disable state of the operation for specifying a phrase. When continuous ROM playback is performed, the next phrase can be specified after verifying that the NAR pin becomes high.</td></tr>
</table>

ABSOLUTE MAXIMUM RATINGS (for MSM6688 (5 V Version))

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	Ta=25°C	–0.3 to +7.0	V
Input Voltage	V_{IN}	Ta=25°C	–0.3 to V_{DD}+0.3	V
Storage temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (for MSM6688 (5 V Version))

Parameter	Symbol	Condition	Range	Unit
Power supply voltage	V_{DD}	DGND=AGND=0V	3.5 to 5.5 (Note 1)	V
Operating temperature	T_{op}	—	–40 to +85	°C
Master clock frequency	f_{osc}	—	4.0 to 8.192	MHz

Note: 1. Recording and playback should be performed at a power supply voltage of 4.5 to 5.5V. For other operations such as backup for a serial register, the IC operates at 3.5 to 5.5V.

ELECTRICAL CHARACTERISTICS (for MSM6688 (5 V Version))

DC Characteristics

$DV_{DD}=DV_{DD'}=AV_{DD}=4.5$ to 5.5V (Note 5)
$DGND=AGND=0V$ $Ta=-40$ to $+85°C$

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High input voltage	V_{IH}	—	$0.8\times V_{DD}$	—	—	V
Low input voltage	V_{IL}	—	—	—	$0.2\times V_{DD}$	V
High output voltage	V_{OH}	$I_{OH} = -40\mu A$	$V_{DD}-0.3$	—	—	V
Low output voltage	V_{OL}	$I_{OL} = 2mA$	—	—	0.45	V
High input current (Note 1)	I_{IH1}	$V_{IH} = V_{DD}$	—	—	10	µA
High input current (Note 2)	I_{IH2}	$V_{IH} = V_{DD}$	—	—	20	µA
Low input current (Note 3)	I_{IL1}	$V_{IL} = GND$	–10	—	—	µA
Low input current (Note 2)	I_{IL2}	$V_{IL} = GND$	–20	—	—	µA
Low input current (Note 4)	I_{IL3}	$V_{IL} = GND$	–400	—	–20	µA
Operating current consumption	I_{DD}	f_{OSC} = 8 MHz, no load	—	15	30	mA
Standby current consumption	I_{DDS}	During power down, no load Ta=–40 to +70°C	—	—	10	µA
		During power down, no load Ta=–40 to +85°C	—	—	50	µA

Note:
1. Applies to all input pins excluding the XT pin.
2. Applies to the XT pin.
3. Applies to the all input pins without pull-up resistors, excluding the XT pin.
4. Applies to the input pins ($\overline{ST}$, $\overline{SP}$, $\overline{PAUSE}$, $\overline{DEL}$) with pull-up resistors, excluding the XT pin.

Analog Characteristics

$DV_{DD}=DV_{DD'}=AV_{DD}=4.5$ to 5.5V
DGND=AGND=0V Ta=–40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
DA output relative error	$\lvert V_{DAE}\rvert$	no load	—	—	10	mV
FIN admissible input voltage range	V_{FIN}	—	1	—	$V_{DD}-1$	V
FIN input impedance	R_{FIN}	—	1	—	—	MΩ
ADIN admissible input voltage range	V_{ADIN}	—	0	—	V_{DD}	V
ADIN input impedance	R_{ADIN}	—	1	—	—	MΩ
Op-amp open loop gain	G_{OP}	$f_{IN}=0$ to 4kHz	40	—	—	dB
Op-amp input impedance	R_{INA}	—	1	—	—	MΩ
Op-amp load resistance	R_{OUTA}	—	200	—	—	kΩ
AOUT load resistance	R_{AOUT}	—	50	—	—	kΩ
FOUT load resistance	R_{FOUT}	—	50	—	—	kΩ

AC Characteristics

$DV_{DD}=DV_{DD'}=AV_{DD}=4.5$ to 5.5V
DGND=AGND=0V Ta=–40 to +85°C
fosc=4.096MHz $f_{SAMP}=8.0$kHz

Parameter			Symbol	Min.	Typ.	Max.	Unit
RESET pulse width			t_{RST}	1	—	—	µs
RESET execution time (Note 1)*			t_{REX}	—	1	—	ms
$\overline{\text{PDWN}}$ low level time *			t_{PDL}	500	—	—	µs
$\overline{\text{PDWN}}$ high level time (Note 1)*			t_{PDH}	500	—	—	µs
Oscillating time after input of $\overline{\text{PDWN}}$ *			t_{PX}	125	—	500	µs
BUSY time after release of $\overline{\text{PDWN}}$ (Note 1)*			t_{BPD}	0.25	—	—	ms
$\overline{\text{ST}}$ pulse width (Note 2)**			t_{ST}	40	—	—	µs
$\overline{\text{SP}}$ pulse width **			t_{SP}	40	—	—	µs
$\overline{\text{PAUSE}}$ pulse width **			t_{PSE}	40	—	—	µs
$\overline{\text{DEL}}$ pulse width (Note 2)*			t_{DEL}	40	—	—	µs
Time required to delete all phrases *			t_{WBLA}	550	—	—	ms
Time required to delete a specified phrase *			t_{WBL1}	70	—	—	ms
Time from input of $\overline{\text{DEL}}$ pulse to $\overline{\text{CSI}}$ fall (Note 2)*			t_{DCS}	—	—	270	µs
Hold time of CA0 to CA5, REC/$\overline{\text{PLAY}}$ after MON rise			t_{CAH}	1	—	—	ms
Address control time at the start of record/playback *			t_{AD1}	—	1	—	ms
Time from input of $\overline{\text{ST}}$ pulse to NAR fall (Note 2)*			t_{STN}	—	—	40	µs
Unvoiced time between phrases during repeated playback *			t_{MID}	0.75	—	1	ms
POMD=H	Time from input of $\overline{\text{ST}}$ pulse to MON rise	Record *	t_{TMH1}	—	—	50	ms
		Playback *	t_{TMH2}	—	—	20	ms
		ROM playback*	t_{TMH3}	—	—	1	ms
	Time from input of $\overline{\text{SP}}$ pulse to MON fall	Record *	t_{PMH1}	—	—	80	ms
		Playback *	t_{PMH2}	—	—	2	ms
		ROM playback*	t_{PMH3}	—	—	2	ms
	Time from input of $\overline{\text{ST}}$ pulse to standby for voice *		t_{STVH}	—	—	50	ms
	Time from input of $\overline{\text{SP}}$ pulse during standby for voice to release of standby for voice *		t_{SPVH}	—	—	80	ms

Items with * are proportional to the period of master clock frequency fosc.
Items with ** are proportional to the period of the master clock frequency fosc, and are also proportional to the sampling frequency f_{SAMP} during record/playback.

Note: 1. The oscillation start stabilization time is added to t_{REX} and t_{BPD}.
The oscillation start stabilization time is several tens of milliseconds for crystals and several hundreds of microseconds for ceramic oscillators.

Note: 2. The oscillation start stabilization time is added if PDMD pin = "L".
The oscillation start stabilization time is several tens of milliseconds for crystals and several hundreds of microseconds for ceramic oscillators.

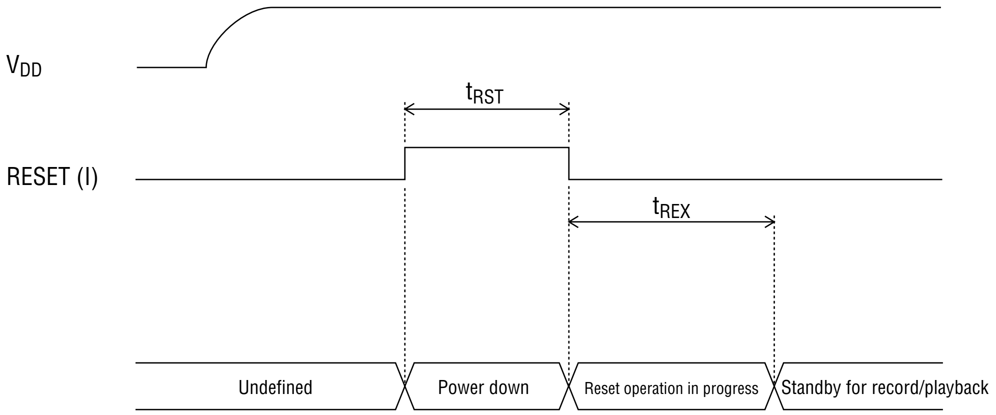
$DV_{DD}=DV_{DD'}=AV_{DD}=4.5$ to 5.5V
DGND=AGND=0V Ta=–40 to +85°C
fosc=4.096MHz $f_{SAMP}=8.0$kHz

Parameter			Symbol	Min.	Typ.	Max.	Unit
PDMD=L	Time from input of $\overline{ST}$ pulse to MON rise	Record *	t_{TML1}	—	—	120	ms
		Playback *	t_{TML2}	—	—	150	ms
		ROM playback *	t_{TML3}	—	—	150	ms
	Time from input of $\overline{SP}$ pulse to MON fall	Record *	t_{PML1}	—	—	80	ms
		Playback *	t_{PML2}	—	—	260	ms
		ROM playback *	t_{PML3}	—	—	260	ms
	Time from input of $\overline{ST}$ pulse to standby for voice	*	t_{STVL}	—	—	120	ms
	Time from input of $\overline{SP}$ pulse during standby for voice to release of standby for voice	*	t_{SPVL}	—	—	80	ms
	Standby transition time at start of playback	*	t_{AOR}	—	64	—	ms
	Standby transition time at end of playback	*	t_{AOF}	—	256	—	ms
Time from input of $\overline{PAUSE}$ pulse to pause		**	t_{PP}	—	—	1	ms
Time from input of $\overline{ST}$ pulse during pause to restart of record/playback		**	t_{PST}	—	—	1	ms

Items with * are proportional to the period of master clock frequency fosc.
Items with ** are proportional to the period of the master clock frequency fosc, and are also proportional to the sampling frequency f_{SAMP} during record/playback.

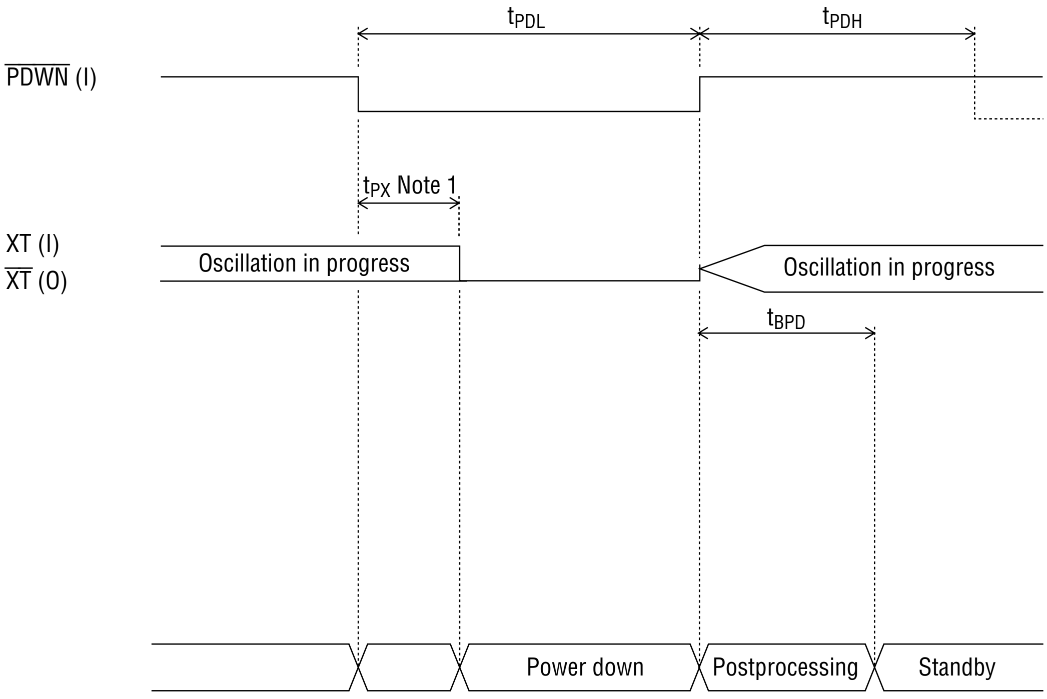
TIMING DIAGRAMS

RESET FUNCTION



V_{DD}
t_{RST}
RESET (I)
t_{REX}
Undefined
Power down
Reset operation in progress
Standby for record/playback

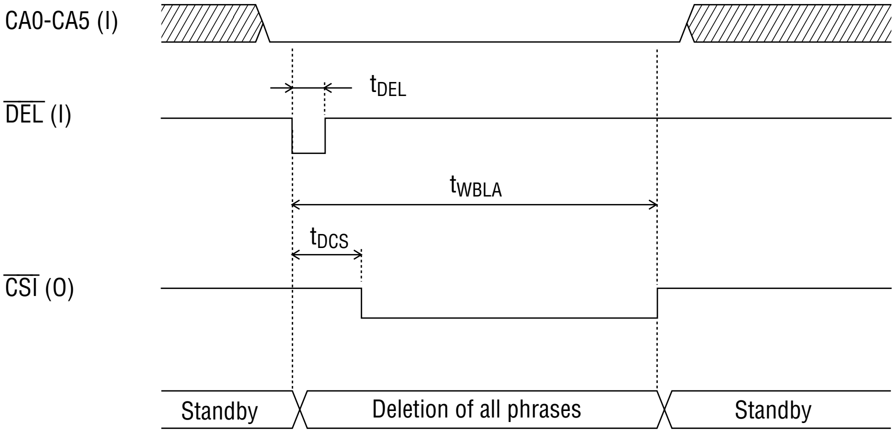
Power Down by $\overline{\text{PDWN}}$ Pin



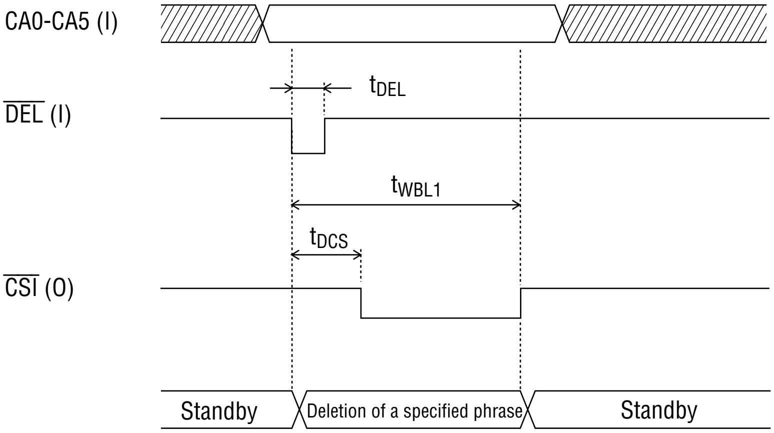
t_{PDL}
t_{PDH}
$\overline{\text{PDWN}}$ (I)
t_{PX} Note 1
XT (I)
$\overline{\text{XT}}$ (O)
Oscillation in progress
Oscillation in progress
t_{BPD}
Power down
Postprocessing
Standby

Note: 1. When an external clock is used, continue to apply the clock input to the XT terminal during t_{PX} after the $\overline{\text{PDWN}}$ pin is set to a low level.

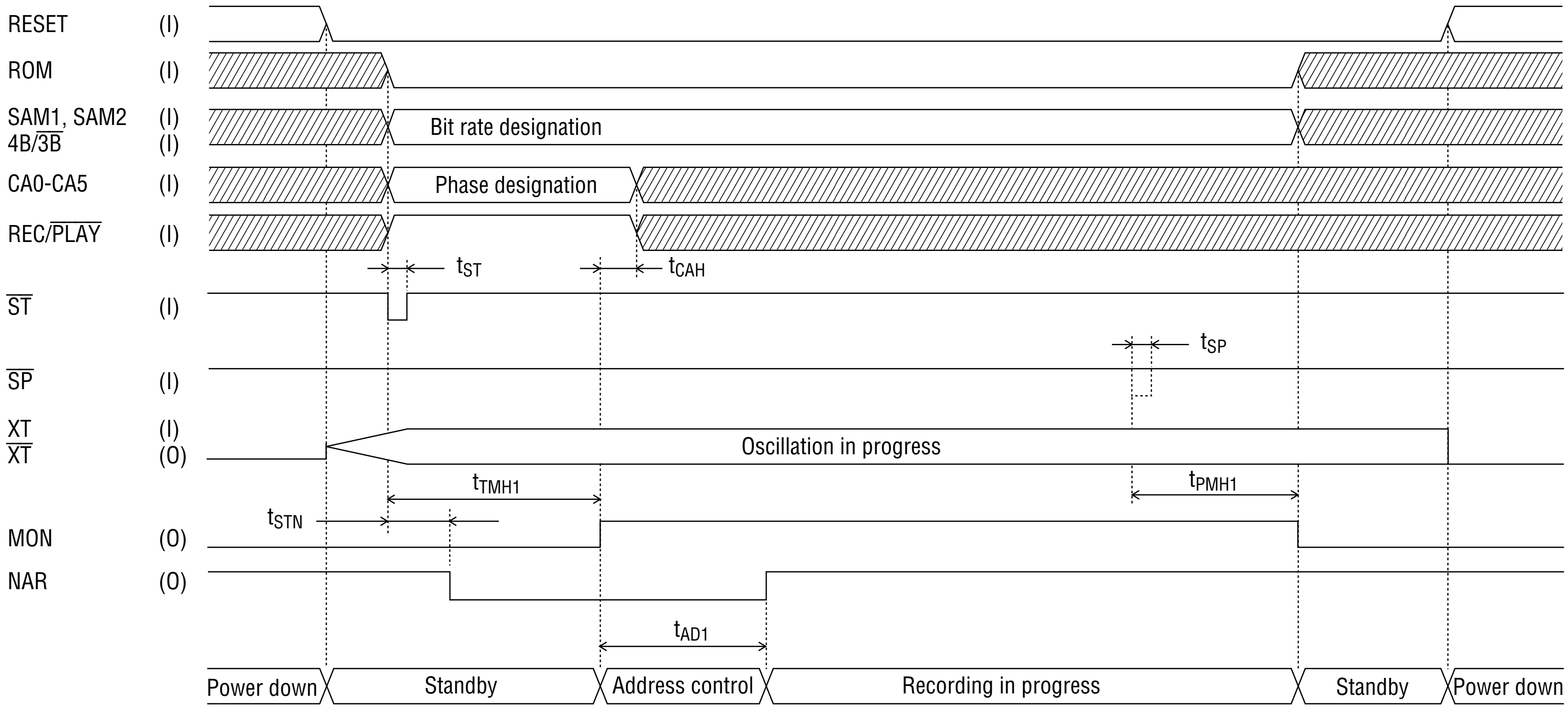
Timing for Deletion of All Phrases


CA0-CA5 (I)
DEL (I)
CSI (O)
tDEL
tWBLA
tDCS
Standby
Deletion of all phrases
Standby

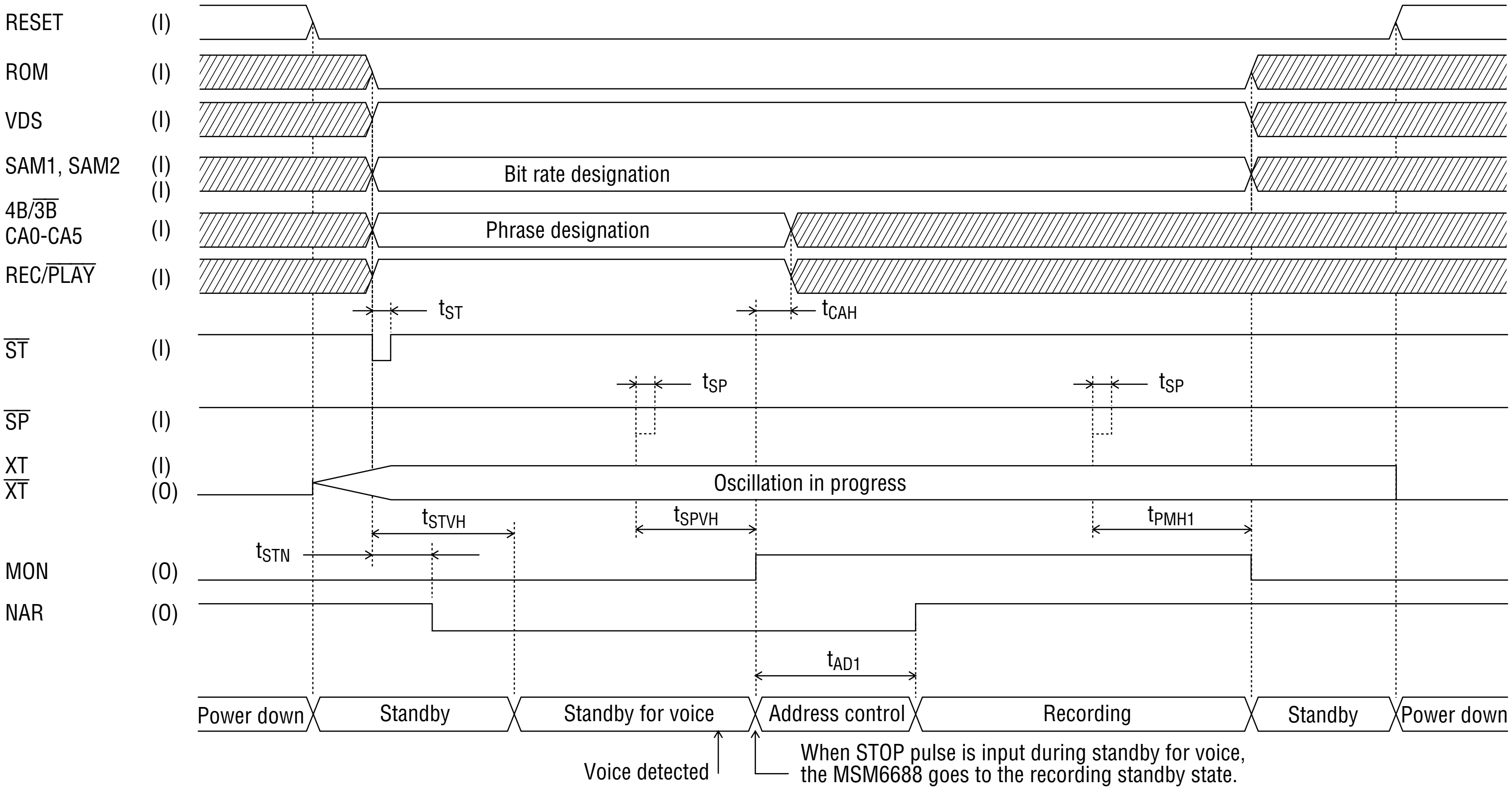
Timing for Deletion of a Specified Phrase


CA0-CA5 (I)
DEL (I)
CSI (O)
tDEL
tWBL1
tDCS
Standby
Deletion of a specified phrase
Standby

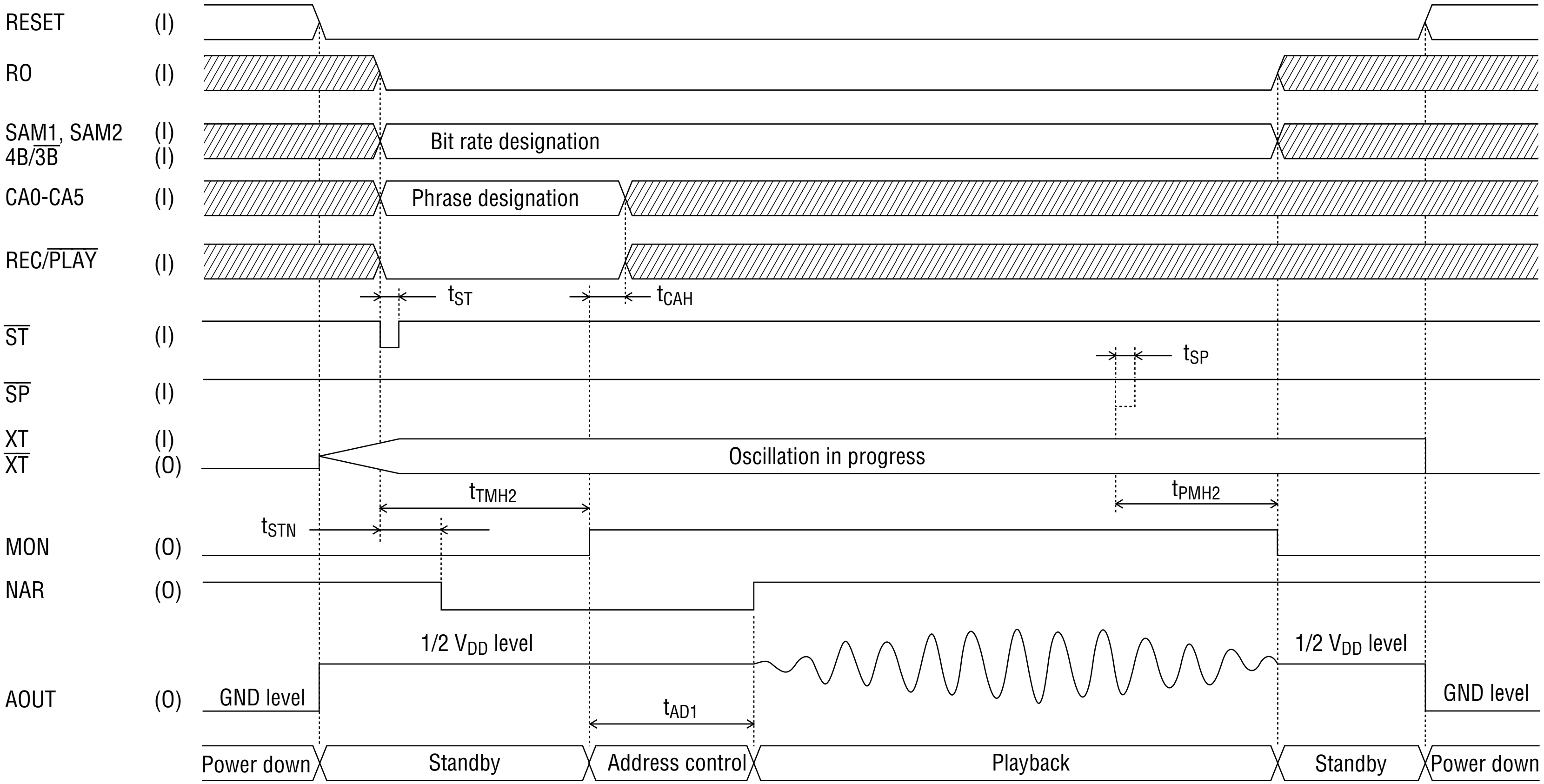
Recording Timing (PDMD Pin = High)


RESET (I)
ROM (I)
SAM1, SAM2 (I)
4B/$\overline{3B}$ (I)
CA0-CA5 (I)
REC/$\overline{PLAY}$ (I)
$\overline{ST}$ (I)
$\overline{SP}$ (I)
XT (I)
$\overline{XT}$ (O)
MON (O)
NAR (O)
Bit rate designation
Phase designation
t_{ST}
t_{CAH}
t_{SP}
Oscillation in progress
t_{TMH1}
t_{PMH1}
t_{STN}
t_{AD1}
Power down
Standby
Address control
Recording in progress
Standby
Power down

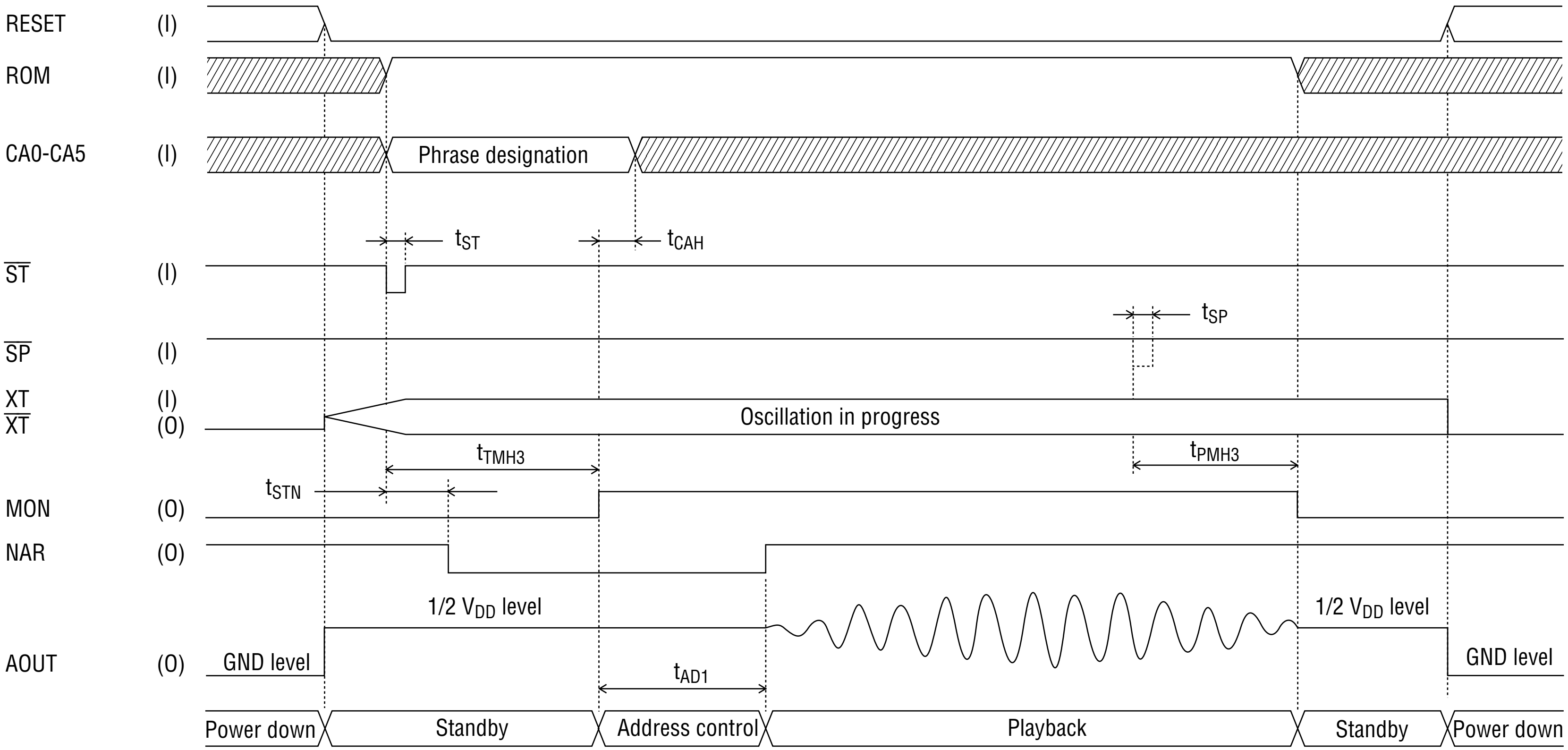
Timing for Voice Triggered Recording (PDMD Pin = High)


RESET (I)
ROM (I)
VDS (I)
SAM1, SAM2 (I)
4B/$\overline{3B}$ (I)
CA0-CA5 (I)
REC/$\overline{PLAY}$ (I)
$\overline{ST}$ (I)
$\overline{SP}$ (I)
XT (I)
$\overline{XT}$ (O)
MON (O)
NAR (O)
Bit rate designation
Phrase designation
t_{ST}
t_{CAH}
t_{SP}
t_{SP}
Oscillation in progress
t_{STVH}
t_{STN}
t_{SPVH}
t_{PMH1}
t_{AD1}
Power down
Standby
Standby for voice
Address control
Recording
Standby
Power down
Voice detected
When STOP pulse is input during standby for voice,
the MSM6688 goes to the recording standby state.

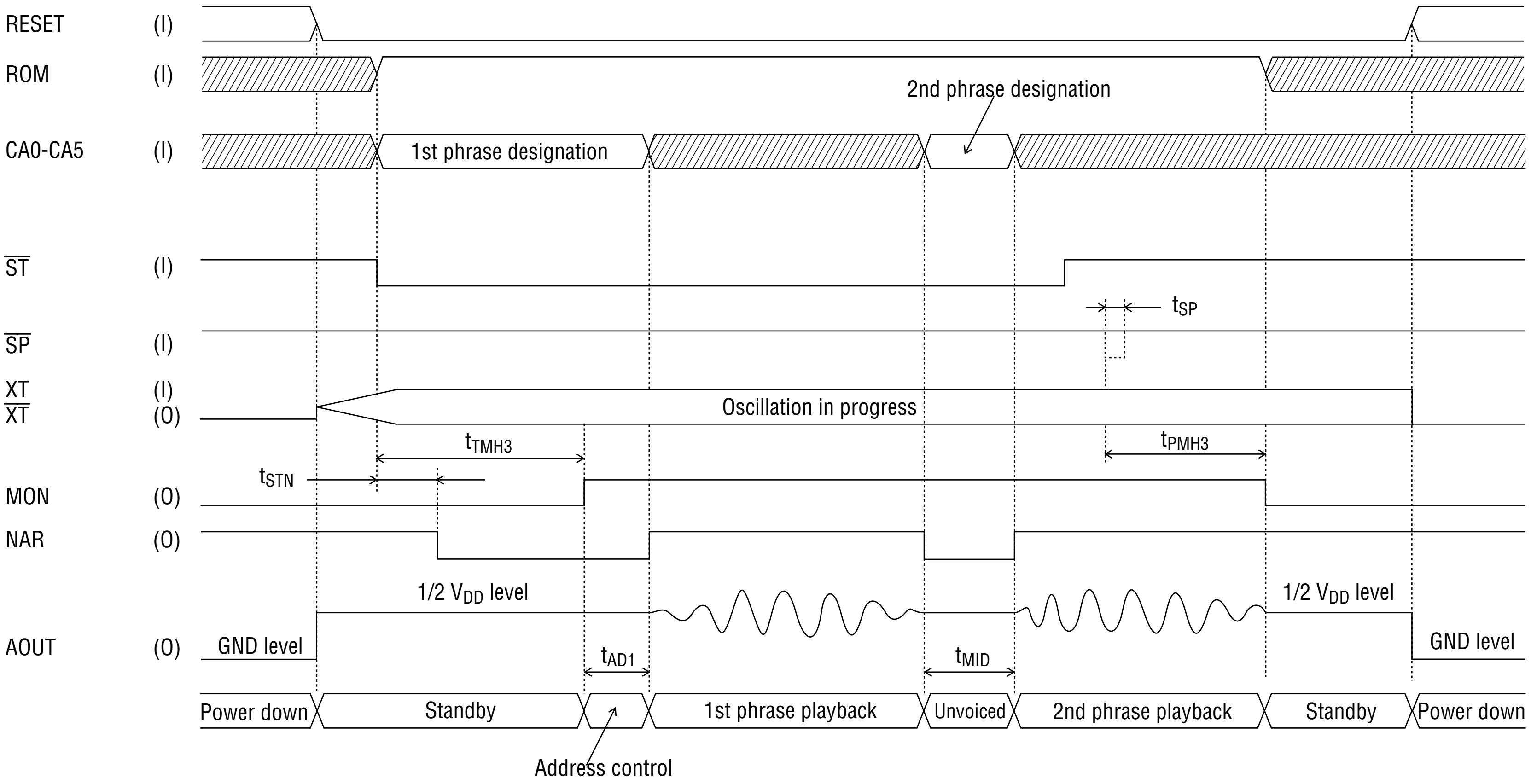
Playback Timing (PDMD Pin = High)


RESET (I)
RO (I)
SAM1, SAM2 (I)
4B/$\overline{3B}$ (I)
CA0-CA5 (I)
REC/$\overline{PLAY}$ (I)
$\overline{ST}$ (I)
$\overline{SP}$ (I)
XT (I)
$\overline{XT}$ (O)
MON (O)
NAR (O)
AOUT (O)
Bit rate designation
Phrase designation
t_{ST}
t_{CAH}
t_{SP}
Oscillation in progress
t_{TMH2}
t_{PMH2}
t_{STN}
1/2 V_{DD} level
GND level
t_{AD1}
1/2 V_{DD} level
GND level
Power down
Standby
Address control
Playback
Standby
Power down

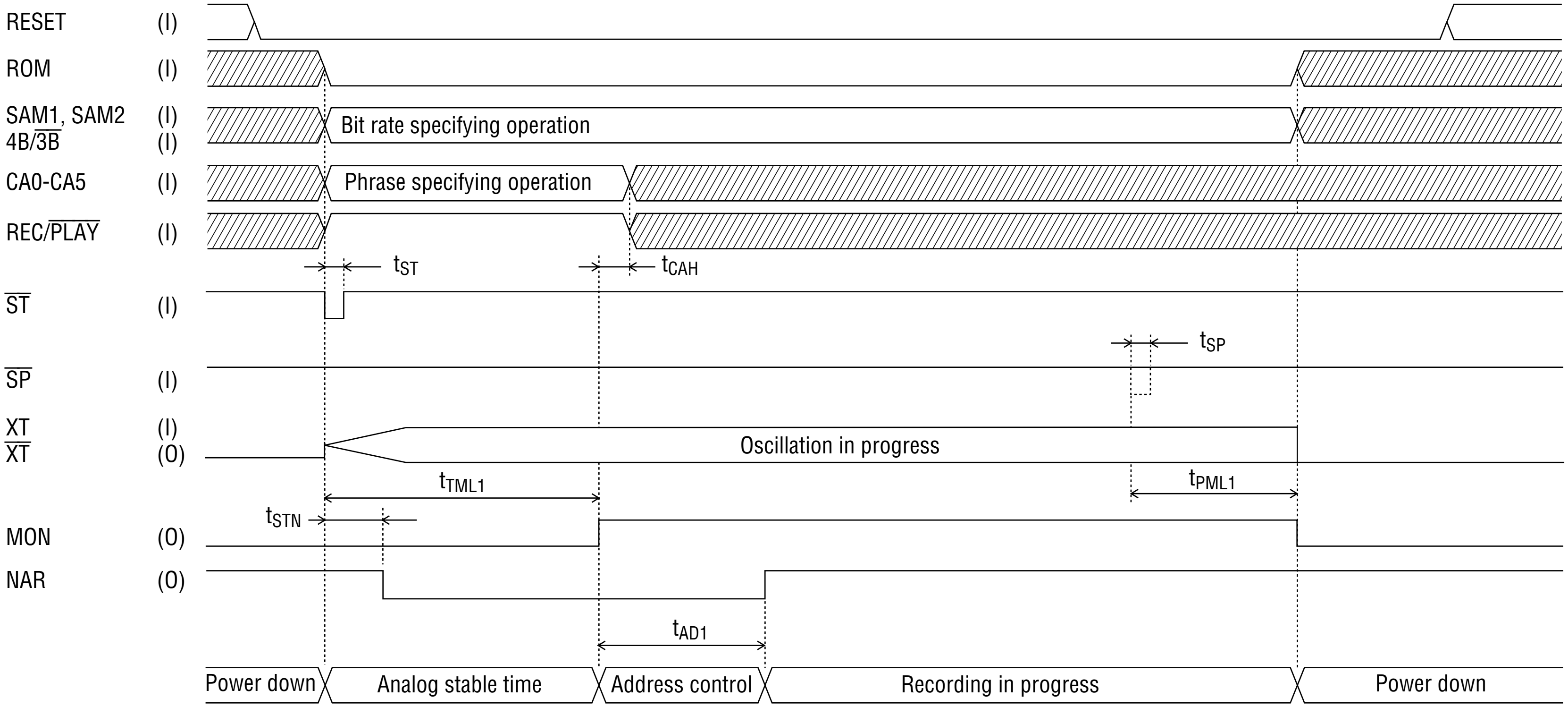
ROM Playback Timing (PDMD Pin = High)


RESET (I)
ROM (I)
CA0-CA5 (I)
Phrase designation
ST (I)
SP (I)
XT (I)
XT (O)
Oscillation in progress
MON (O)
NAR (O)
AOUT (O)
t_ST
t_CAH
t_SP
t_TMH3
t_PMH3
t_STN
t_AD1
1/2 V_DD level
GND level
1/2 V_DD level
GND level
Power down
Standby
Address control
Playback
Standby
Power down

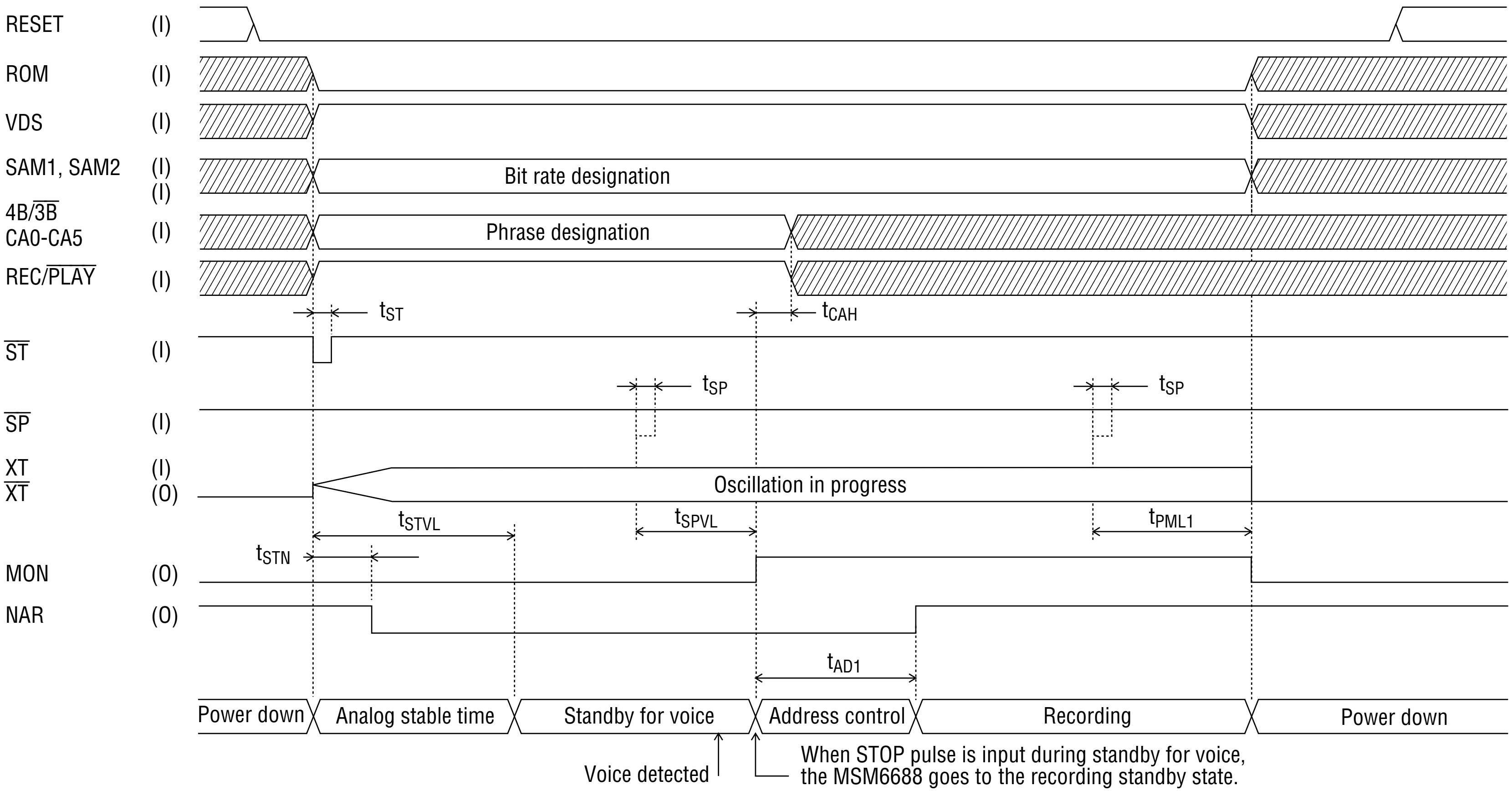
Continuous ROM Playback Timing (PDMD Pin = High)


RESET (I)
ROM (I)
CA0-CA5 (I)
$\overline{ST}$ (I)
$\overline{SP}$ (I)
XT (I)
$\overline{XT}$ (O)
MON (O)
NAR (O)
AOUT (O)
2nd phrase designation
1st phrase designation
t_{SP}
Oscillation in progress
t_{TMH3}
t_{PMH3}
t_{STN}
1/2 V_{DD} level
1/2 V_{DD} level
GND level
GND level
t_{AD1}
t_{MID}
Power down
Standby
1st phrase playback
Unvoiced
2nd phrase playback
Standby
Power down
Address control

Recording Timing (PDMD Pin = Low)

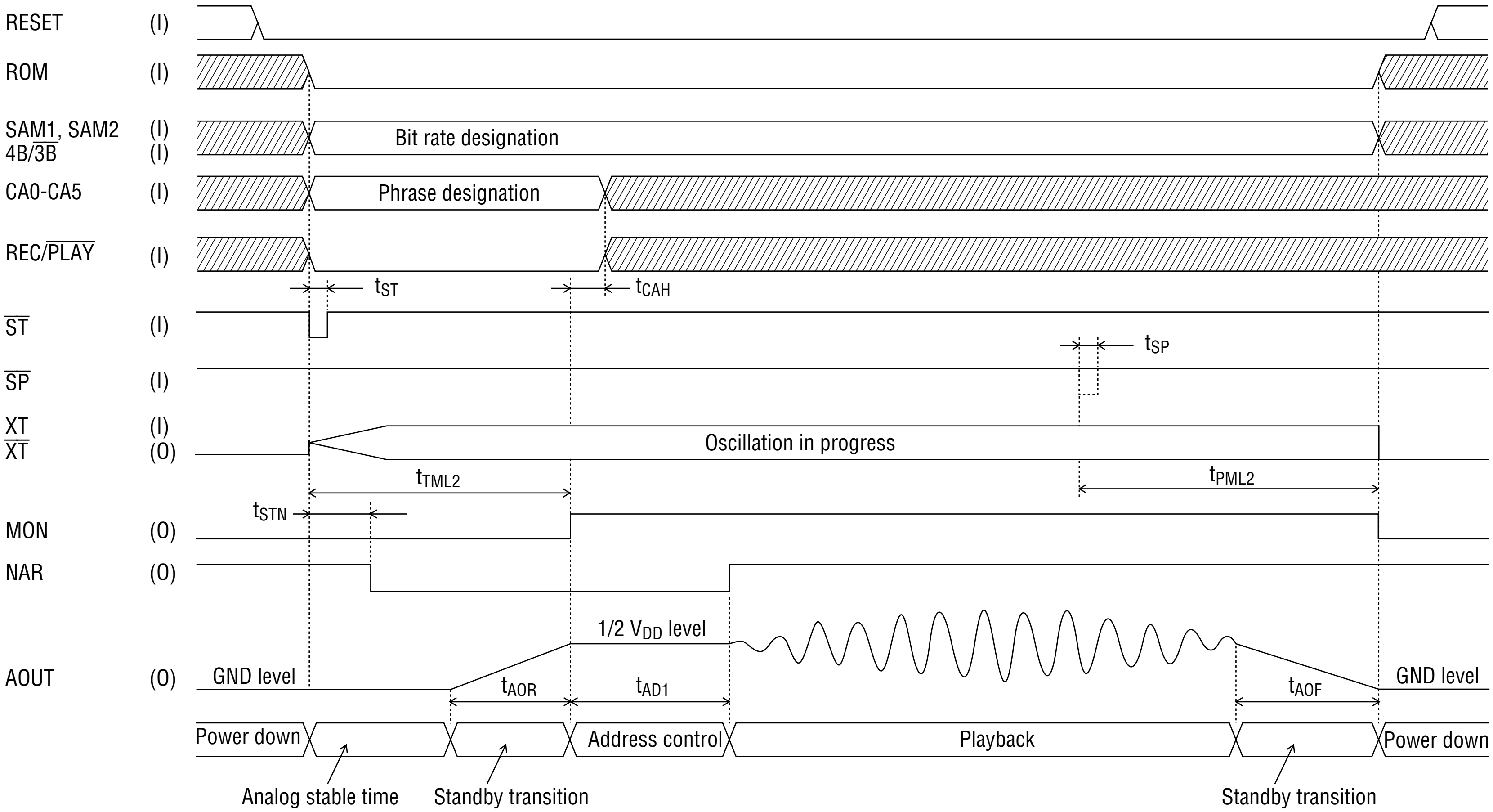

RESET (I)
ROM (I)
SAM1, SAM2 (I)
4B/3B (I)
Bit rate specifying operation
CA0-CA5 (I)
Phrase specifying operation
REC/PLAY (I)
t_{ST}
t_{CAH}
ST (I)
t_{SP}
SP (I)
XT (I)
XT (O)
Oscillation in progress
t_{TML1}
t_{PML1}
t_{STN}
MON (O)
NAR (O)
t_{AD1}
Power down
Analog stable time
Address control
Recording in progress
Power down

Timing for Voice Triggered Recording (PDMD Pin = Low)

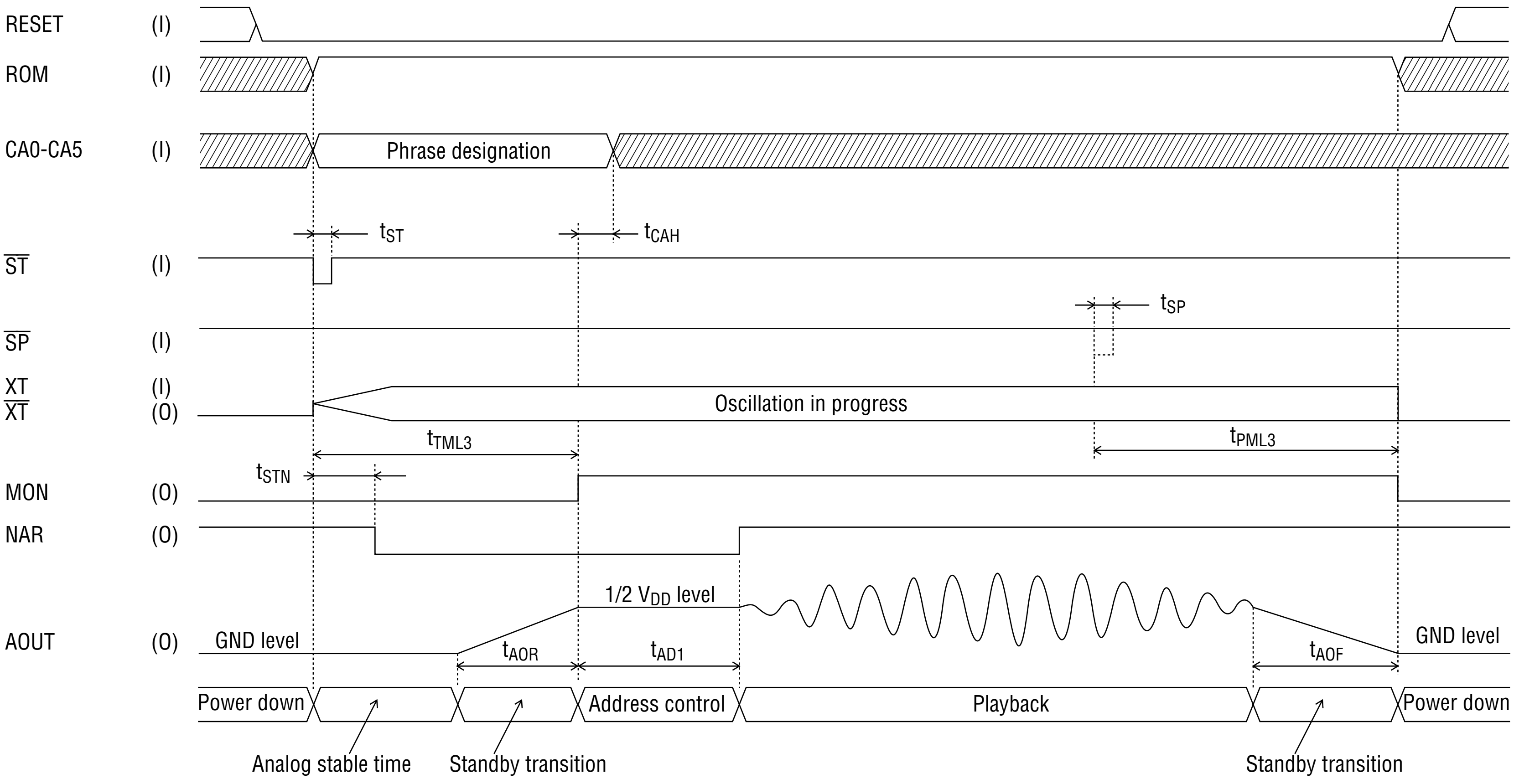

RESET (I)
ROM (I)
VDS (I)
SAM1, SAM2 (I)
4B/$\overline{3B}$ (I)
CA0-CA5 (I)
REC/$\overline{PLAY}$ (I)
$\overline{ST}$ (I)
$\overline{SP}$ (I)
XT (I)
$\overline{XT}$ (O)
MON (O)
NAR (O)
Bit rate designation
Phrase designation
t_{ST}
t_{CAH}
t_{SP}
t_{SP}
Oscillation in progress
t_{STVL}
t_{SPVL}
t_{PML1}
t_{STN}
t_{AD1}
Power down
Analog stable time
Standby for voice
Address control
Recording
Power down
Voice detected

When STOP pulse is input during standby for voice, the MSM6688 goes to the recording standby state.

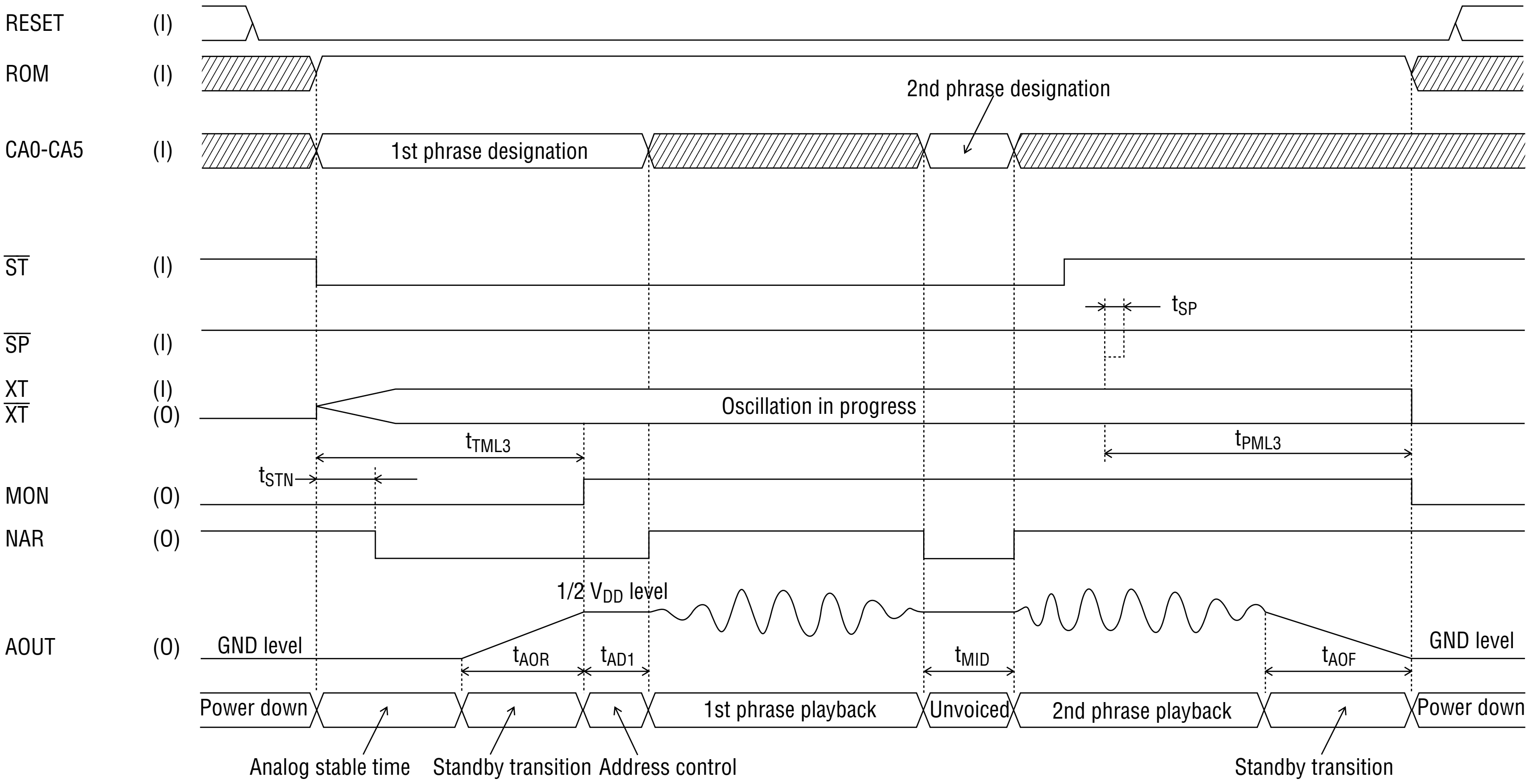
Playback Timing (PDMD Pin = Low)


RESET (I)
ROM (I)
SAM1, SAM2 (I)
4B/$\overline{3B}$ (I)
Bit rate designation
CA0-CA5 (I)
Phrase designation
REC/$\overline{PLAY}$ (I)
t_{ST}
t_{CAH}
$\overline{ST}$ (I)
t_{SP}
$\overline{SP}$ (I)
XT (I)
$\overline{XT}$ (O)
Oscillation in progress
t_{TML2}
t_{PML2}
t_{STN}
MON (O)
NAR (O)
1/2 V_{DD} level
AOUT (O)
GND level
t_{AOR}
t_{AD1}
t_{AOF}
GND level
Power down
Address control
Playback
Power down
Analog stable time
Standby transition
Standby transition

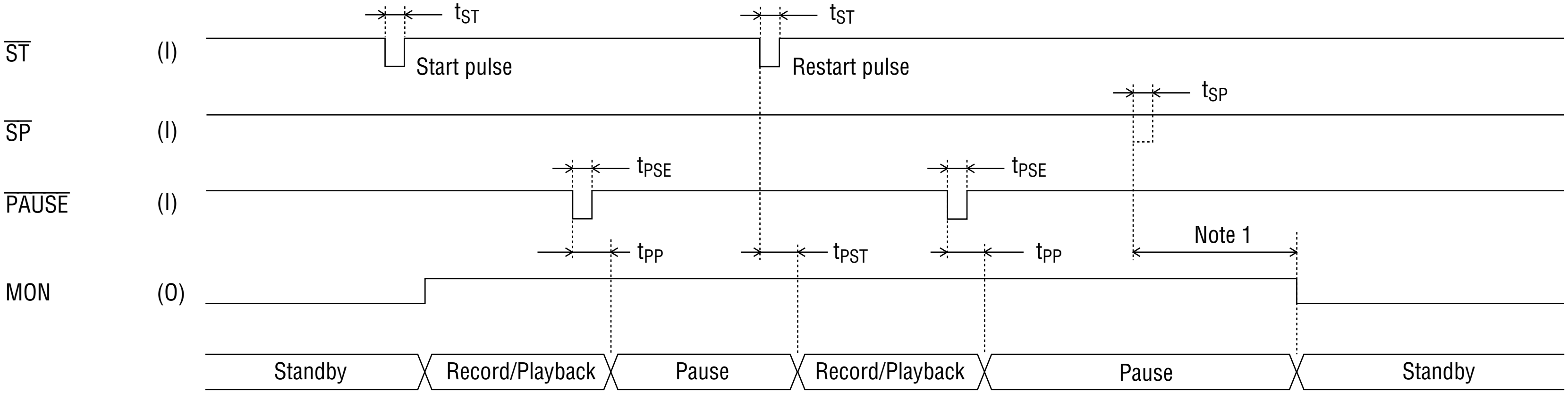
ROM Playback Timing (PDMD Pin = Low)


RESET (I)
ROM (I)
CA0-CA5 (I)
Phrase designation
t_{ST}
t_{CAH}
$\overline{ST}$ (I)
t_{SP}
$\overline{SP}$ (I)
XT (I)
$\overline{XT}$ (O)
Oscillation in progress
t_{TML3}
t_{PML3}
t_{STN}
MON (O)
NAR (O)
1/2 V_{DD} level
AOUT (O)
GND level
t_{AOR}
t_{AD1}
t_{AOF}
GND level
Power down
Address control
Playback
Power down
Analog stable time
Standby transition
Standby transition

Continuous ROM Playback Timing (PDMD Pin = Low)


RESET (I)
ROM (I)
CA0-CA5 (I)
ST (I)
SP (I)
XT (I)
XT (O)
MON (O)
NAR (O)
AOUT (O)
1st phrase designation
2nd phrase designation
t_{SP}
Oscillation in progress
t_{TML3}
t_{PML3}
t_{STN}
1/2 V_{DD} level
GND level
GND level
t_{AOR}
t_{AD1}
t_{MID}
t_{AOF}
Power down
1st phrase playback
Unvoiced
2nd phrase playback
Power down
Analog stable time
Standby transition
Address control
Standby transition

Record/Playback Pause Timing


$\overline{ST}$ (I)
$\overline{SP}$ (I)
$\overline{PAUSE}$ (I)
MON (O)
t_{ST}
Start pulse
t_{ST}
Restart pulse
t_{SP}
t_{PSE}
t_{PSE}
t_{PP}
t_{PST}
t_{PP}
Note 1
Standby
Record/Playback
Pause
Record/Playback
Pause
Standby

Note 1: This time interval varies depending on the state of PDMD pin and the record/playback mode and is one of t_{PMH1}, t_{PMH2}, t_{PMH3}, t_{PML1}, t_{PML2} and t_{PML3}.

FUNCTIONAL DESCRIPTION

Recording Time and Memory Capacity

The recording time depends on the memory capacity of the external serial registers, sampling frequency, and ADPCM bit length, and is given by

$$\text{Recording time} = \frac{1.024 \times \text{memory capacity (K bits)}}{\text{sampling frequency (kHz)} \times \text{bit length (bits)}} \quad \text{(seconds)}$$

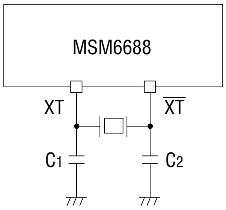
For example, if the sampling frequency is $\frac{4096}{768}$ kHz (= 5.333 kHz), ADPCM bit length is 3 bits, and four 8M bit serial registers are used, the recording time can be obtained as follows.

$$\begin{aligned} \text{Recording time} &= \frac{1.024 \times (8192 \times 4 - 64)}{5.333 \times 3} = 2093 \text{ seconds} \\ &= 34 \text{ minutes } 53 \text{ seconds} \end{aligned}$$

In the above equation, the memory capacity is obtained by subtracting the memory capacity (64 Kbits) for the channel index area from the total memory capacity.

Connection of an Oscillator

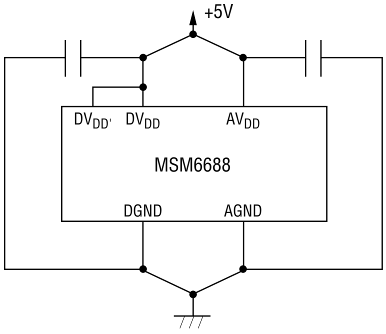
Connect a ceramic oscillator or a crystal oscillator to XT and XT pins as shown below. The optimal load capacities when connecting ceramic oscillators from MURATA MFG. and KYOCERA CORPORATION are shown below for reference.



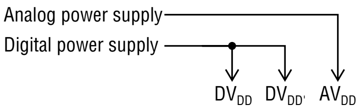
Ceramic oscillator			Optimal load capacity	
	Type	Freq(MHz)	C_1(pF)	C_2(pF)
MURATA MFG.	CSA4.00MG CST4.00MGW (with capacitor)	4.0	30	30
	CSA6.00MG CST6.00MGW (with capacitor)	6.0		
	CSA8.00MTZ CST8.00MTW (with capacitor)	8.0		
KYOCERA CORPO-RATION	KBR-4.0MSA KBR-4.0MKS (with capacitor)	4.0	33	33
	PBRC4.00A PBRC4.00B			
	KBR-6.0MSA KBR-6.0MKS (with capacitor)	6.0		
	PBRC6.00A PBRC6.00B			
	KBR-8.0M	8.0		
	PBRC8.00A PBRC8.00B			

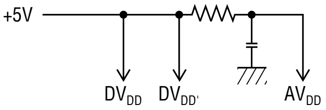
Power Supply Wiring

As shown in the following diagram, supply the power to this MSM6688 from the same power source, but separate the power supply wiring to the analog portion from that to the logic position.


+5V
DVDD'
DVDD
AVDD
MSM6688
DGND
AGND

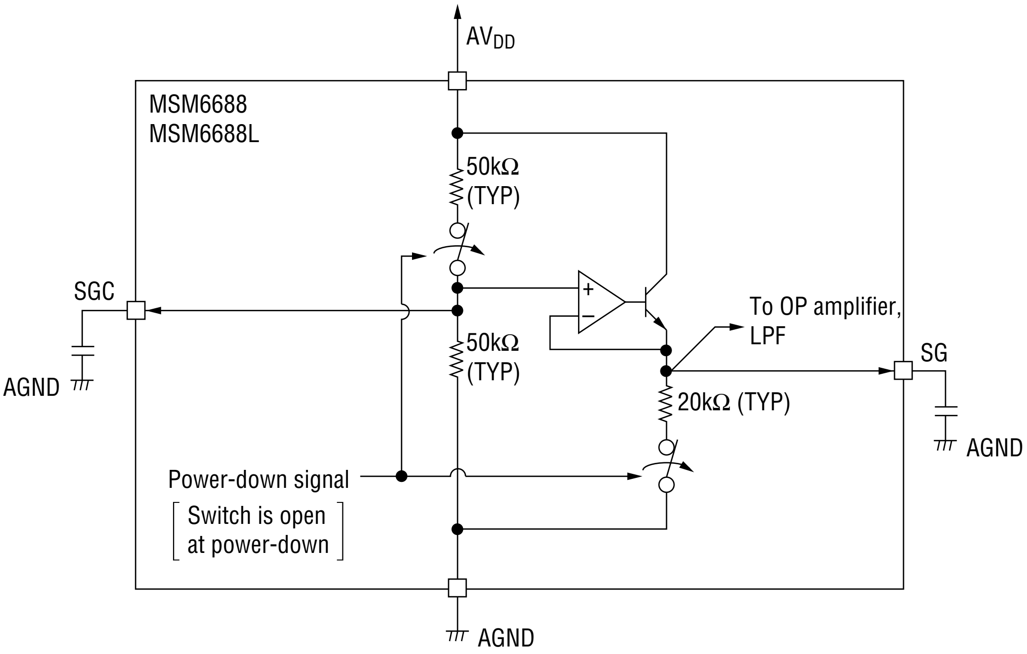
The following connections are not permitted.


Analog power supply
Digital power supply
DVDD
DVDD'
AVDD


+5V
DVDD
DVDD'
AVDD

Configuring SGC and SG pins

The internal equivalent circuit around the SGC and SG pins is shown below.


AVDD
MSM6688
MSM6688L
50kΩ (TYP)
SGC
AGND
50kΩ (TYP)
+
−
To OP amplifier, LPF
SG
20kΩ (TYP)
AGND
Power-down signal
Switch is open at power-down
AGND

The SG signal is a reference voltage (signal ground) for internal OP amplifiers and LPF. Install a capacitor between the SGC pin and AGND and between the SG pin and AGND respectively in order to make the SG signal noiseless. It is recommended to use an approx. 0.1 µF capacitor, which should be determined after evaluating the tone quality.

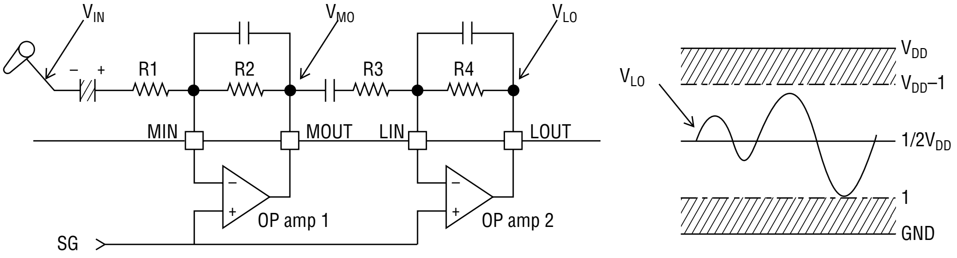
It takes several ten msec until the DC levels such as the SG level of the analog circuit is stabilized after the power-down mode is cancelled. The larger capacitance of a capacitor connected to SGC or SG requires the longer time for stabilizing.
After the power-down mode is cancelled, enter voices after the DC levels for the analog circuit has been stabilized.

When the device is in power-down mode, the output voltage of the SG pin becomes unstable. Therefore, SG must not be supplied to external circuits.
Otherwise, power supply current may be leaked via the internal SG circuit.
Same is true for the SGC pin.

Analog Input Amplifier Circuit

This MSM6688 has two built-in operational amplifiers for amplifying the microphone output. Each OP amplifier is provided with the inverting input pin and output pin. The analog circuit reference voltage SG (signal ground) is connected internally to the non-inverting input of each OP amplifier.

For amplification, form an inverting amplifier circuit and adjust the amplification factor by using external resistors as shown below.



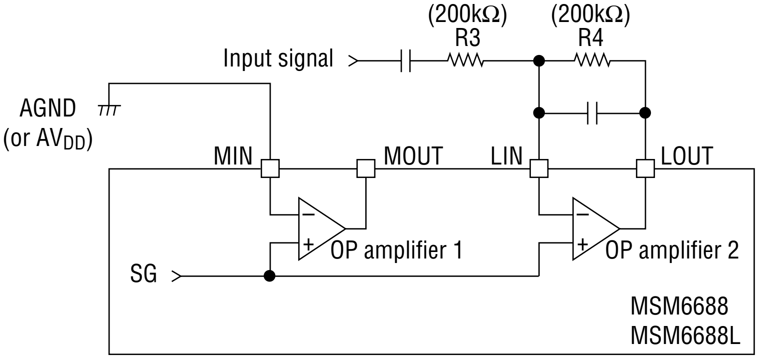
$$V_{LO} = \frac{R4}{R3}\, V_{MO} = \frac{R2 \bullet R4}{R1 \bullet R3}\, V_{IN}(V)$$

During the time the recording operation is performed, the output V_{LO} of OP amp 2 is connected to the input FIN of the built-in LPF. The allowable FIN input voltage (V_{FIN}) ranges from 1V to (V_{DD} – 1)V. Therefore, the amplification factor must be adjusted so that the V_{LO} amplitude can be within the allowable FIN input voltage range.

For example, if V_{DD} = 5V, V_{LO} becomes 3 V_{p-p} max. If V_{LO} exceeds the allowable FIN input voltage range, the output of the LPF will be a clipped waveform.

The load resistance R_{OUTA} of the OP amplifier is 200 kΩ minimum, so that the feedback resistors R2 and R4 of the inverting amplifier circuit must be 200 kΩ or more.

When OP amplifier 1 is not used and OP amplifier 2 is used, the MIN pin must be connected to AGND or AV_{DD}, and the MOUT pin must be open.
Even if amplification is unnecessary, OP amplifier 2 must be always used.
Below is an example of an analog input amplifier circuit when the amplification factor is 1.


(200kΩ)
R3
(200kΩ)
R4
Input signal
AGND
(or AV_{DD})
MIN
MOUT
LIN
LOUT
−
+
OP amplifier 1
−
+
OP amplifier 2
SG
MSM6688
MSM6688L

Connection of LPF Circuit Peripherals

The AMON pin is connected internally to the output of the amplifier circuit (LOUT pin) in the recording mode and to the output of the built-in DA converter in the playback mode. Therefore, connect the AMON pin directly to the input (FIN pin) of the built-in LPF.

Both the FOUT and AOUT pins are the output pins of the built-in LPF. Connect the FOUT pin to the input (ADIN pin) of the built-in AD converter and connect the AOUT pin to an external speaker through an external speaker drive amplifier.

In the MSM6688, the connection of each of the FOUT and AOUT pins is changed to one of the output of the LPF, GND (ground) level, and SG (signal ground) level, depending on the operation status as shown below.

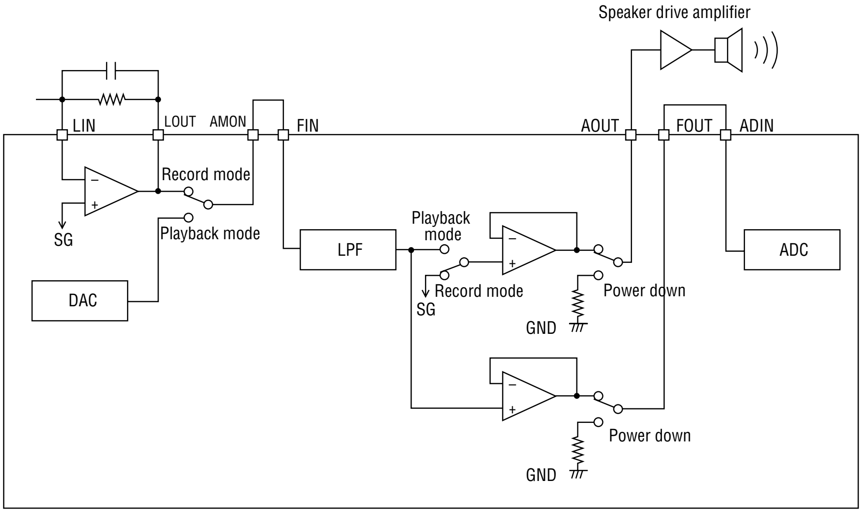
When PDMD pin = high level:

Analog pin	At power down (RESET pin = H)	During operation (RESET pin = L)	
		Recording mode	Playback mode
FOUT pin	GND level	LPF output (recording waveform)	LPF output
AOUT pin	GND level	SG level	LPF output (playback waveform)

When PDMD pin = L:

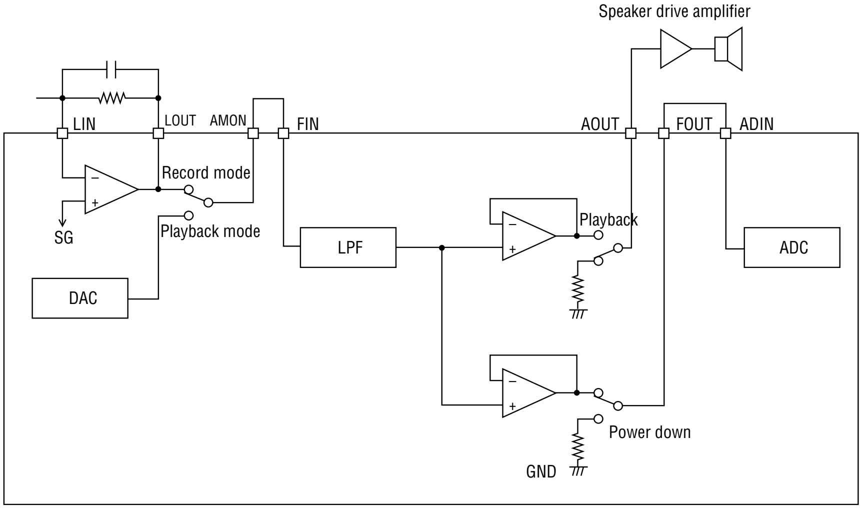
Analog pin	At power down	During operation	
		Recording mode	Playback mode
FOUT pin	GND level	LPF output (recording waveform)	LPF output
AOUT pin	GND level	GND level	LPF output (playback waveform)

When PDMD pin = H:


Speaker drive amplifier
LIN
LOUT
AMON
FIN
AOUT
FOUT
ADIN
Record mode
Playback mode
SG
DAC
LPF
Playback mode
Record mode
SG
GND
Power down
ADC
Power down
GND

Note: This diagram shows the state of each switch during the recording operation.

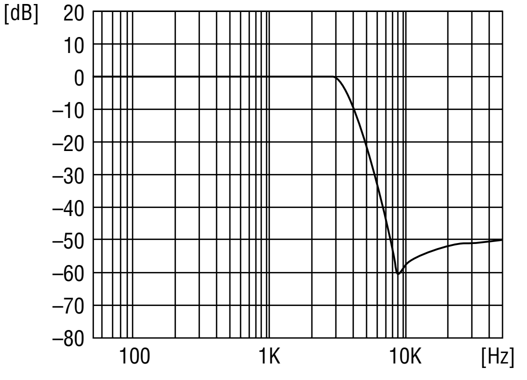
When PDMD = L:


Speaker drive amplifier
LIN
LOUT
AMON
FIN
AOUT
FOUT
ADIN
Record mode
Playback mode
SG
DAC
LPF
Playback
ADC
Power down
GND

Note: This diagram shows the state of each switch during the recording operation.

LPF Characteristics

This IC contains a fourth-order switched-capacitor LPF.
The attenuation characteristic of this LPF is –40 dB/oct. The cut-off frequency and frequency characteristics of this LPF vary in proportion to the sampling frequency (fsamp). The cut-off frequency is preset to 0.4 times the sampling frequency. The following graph depicts the frequency characteristics of the LPF at fsamp = 8 kHz.



LPF Frequency Characteristics (fsamp = 8.0 kHz)

Reset Function

By applying a high level to the RESET pin, the MSM6688 stops frequency oscillation to minimize current consumption and goes to the power-down state. At the same time, the control circuit is reset and initialized.

If a high level is applied to the RESET pin during record/playback operation , the MSM6688 is set to the power-down state and initialized state, so that voice data becomes undefined.

The following shows the power-down state of the MSM6688.

(1) Frequency oscillation is stopped and all operations of the internal circuit are halted.

(2) The current consumption is minimized. When an external clock is used, apply a ground (GND) level to the XT pin at power down so that no current can flow into the oscillation circuit.

(3) $\overline{\mathrm{CS1}}$ – $\overline{\mathrm{CS4}}$ pins are set to a high level to minimize the current consumption of external serial registers and serial voice ROMs.

(4) Pull-up resistors are removed from the input control $\overline{\mathrm{ST}}$, $\overline{\mathrm{SP}}$, $\overline{\mathrm{PAUSE}}$, and $\overline{\mathrm{DEL}}$ pins.

(5) The state of the output pins are as follows.

Pin name	Power down mode with RESET="H"	Power down mode with $\overline{\mathrm{PDWN}}$="L"
$\overline{\mathrm{SAS}}$, $\overline{\mathrm{TAS}}$, $\overline{\mathrm{CS1}}$-$\overline{\mathrm{CS4}}$, $\overline{\mathrm{RWCK}}$	"H" level	"H" level
SADX, $\overline{\mathrm{WE}}$, NAR	"H" level	"H" level or "L" level
SADY	"L" level	"H" level or "L" level
MON	"L" level	"L" level
AOUT, FOUT	GND level	GND level

After powering up the MSM6688, be sure to initialize it by applying a high level to the RESET pin.

Power Down by the $\overline{\text{PDWN}}$ pin

By applying a low level to the $\overline{\text{PDWN}}$ pin, the MSM6688 may be set to the power-down state, in which the oscillation and all operations of internal circuits are halted. Unlike the reset operation by the RESET input, the control circuit will not be initialized by this power-down operation.

The power-down operation will not affect the data in the internal control circuit and external serial registers. Therefore, this power-down operation is useful when the battery backup takes place in case of power failure.

When $\overline{\text{PDWN}}$ becomes low during one of the following operations, their respective operations will be performed after the power-down state is released ($\overline{\text{PDWN}}$ = H).

(1) When the MSM6688 is powered down ($\overline{\text{PDWN}}$ = L) during the record/plaback operation: The record/playback operation is stopped. After the release of the power-down state, the postprocessing will be performed.

(2) When the MSM6688 is powered down ($\overline{\text{PDWN}}$ = L) during the phrase deleting operation: The phrase deleting operation is temporarily stopped and will be restarted after the release of the power-down state.

(3) When the MSM6688 is powered down ($\overline{\text{PDWN}}$ = L) during the time the transition of the AOUT output to a DC level is in progress: This transition operation is temporalily stopped and will be continued after the release of the power-down state.

Record/Playback Control Mode

Either record / playback mode or ROM playback mode can be selected through the ROM pin as described below.

ROM pin	Record/playback control mode
L	Record/playback
H	ROM playback

1. Record/playback

The recorded voice data is stored in serial registers. The recording area is indirectly allocated to each phrase by setting the phase specifying pins CA0 to CA5 (63 phrases). The recording area for each phrase is managed by the MSM6688 as described below.

The total memory capacity of the connected external serial registers is equally divided into 256 memory blocks. When recording is performed, voice data is written into the memory blocks unused by other phrases. When a specified phase is deleted, the blocks used by this phrase become unused blocks.

When re-recording is performed, voice data is written in the memory area consisting of the memory blocks used by this phrase and the unused memory blocks.

The memory capacity of one memory block and the number of initially available memory blocks (recording time) vary according to the total memory capacity of the connected serial registers.

RSEL2		L	L	H	H
RSEL1		L	H	L	H
Total memory capacity		8M bits	16M bits	24M bits	32M bits
Memory capacity of one block		32K bits	64K bits	128K bits	128K bits
Recording time of one block	16kbps	2.0 seconds	4.1 seconds	8.2 seconds	8.2 seconds
	24kbps	1.4 seconds	2.7 seconds	5.5 seconds	5.5 seconds
	32kbps	1.0 second	2.0 seconds	4.1 seconds	4.1 seconds
Number of initially available blocks		254	255	191	255

2. ROM playback

For playback of the voice data stored in the connected serial voice ROM, the playback area is allocated indirectly to each fixed message phrase by setting phrase specifying pins CA0 to CA5 (63 phases).

The start address, stop address, sampling frequency, and ADPCM bit length which specify the playback area for each phase are written in the index area of the serial voice ROM. When the playback operation is started, the MSM6688 fetches these data from the index area.

Deleting phrases

1. Deleting all phrases

All 63 phrases ch01 through ch3F can be deleted by specifying ch00 and applying a low pulse to the $\overline{\text{DEL}}$ pin. When all phrases are deleted, all phrases ch01– ch3F (63 phrases) go to the unrecorded status and, at the same time, the initial data for address control is written in the serial registers. Therefore, whenever the MSM6688 is powered up, delete all phrases after applying a high level to the RESET pin.

2. Deleting a specified phrase

By specifying one of ch01 - ch3F phrase and applying a low level to the $\overline{\text{DEL}}$ pin, the specified phrase can be deleted and put to the unrecorded state. The blocks for the deleted phrases are added to available unused blocks (available recording time).

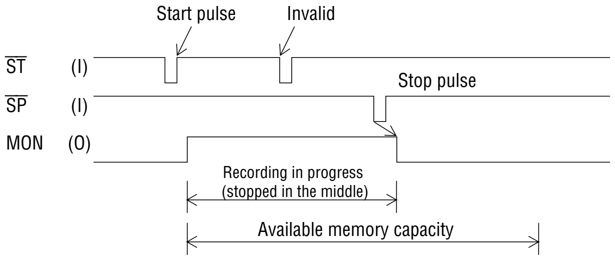
Recording Method

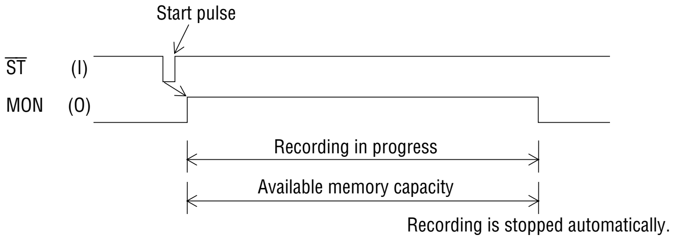
Whenever the MSM6688 is powered up, be sure to delete all phrases after applying a high level to the RESET pin. Then, start the recording operation.

(1) Set recording conditions at the relevant pins.

ROM pin:	Low level
REC/$\overline{\text{PLAY}}$ pin:	High level
VOS pin:	Selection of voice triggered starting (high level enables voice activation and low level disables voice activation.)
SAM1 and SAM2 pins:	Select the sampling frequency.
4B /$\overline{\text{3B}}$ pin:	Select the ADPCM bit length.
CA0 – CA5 pins:	Specify one of 63 phrases ch01 – ch3F.

(2) To start recording, apply a low pulse to the $\overline{\text{ST}}$ pin.
To stop recording in progress, apply a low pulse to the $\overline{\text{SP}}$ pin. When recording continues to the end of the memory capacity, recording is automatically stopped. In case of re-recording, voice data will be written in the memory block used by the specified phrase and unused memory blocks. Therefore, the voice data is overwritten on the previously recorded contents. The MON pin outputs a high level during recording.


Start pulse
Invalid
ST (I)
Stop pulse
SP (I)
MON (O)
Recording in progress
(stopped in the middle)
Available memory capacity


Start pulse
ST (I)
MON (O)
Recording in progress
Available memory capacity
Recording is stopped automatically.

Playback Method

(1) Set playback conditions at the relevant pins.

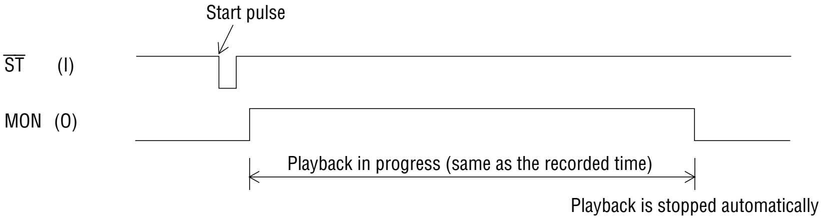
ROM pin:	Low level
REC/$\overline{\text{PLAY}}$ pin:	Low level
SAM1 and SAM2 pins:	Select the sampling frequency.
4B/$\overline{\text{3B}}$ pin:	Specify the ADPCM bit length selected for recording.
CA0–CA5 pins:	Specify one of 63 phases ch01–ch3F.

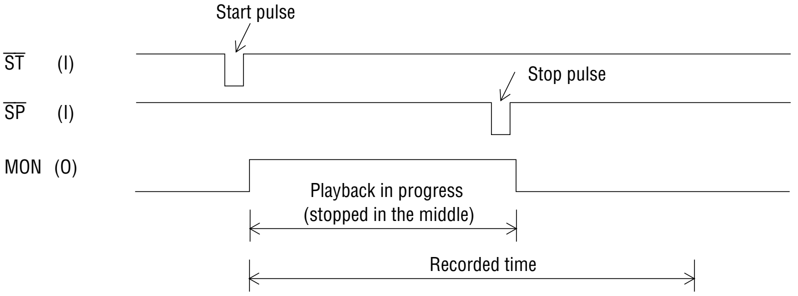
(2) To start playback, apply a low pulse to the $\overline{\text{ST}}$ pin.

When playback for the duration of the recorded data is finished, the playback is stopped automatically.

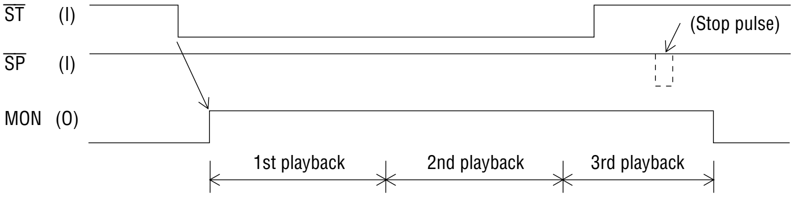
To stop playback in progress, apply a low pulse to the $\overline{\text{SP}}$ pin.

The MON pin outputs a high level during playback.


Start pulse
$\overline{\text{ST}}$ (I)
MON (O)
Playback in progress (same as the recorded time)
Playback is stopped automatically


Start pulse
$\overline{\text{ST}}$ (I)
Stop pulse
$\overline{\text{SP}}$ (I)
MON (O)
Playback in progress
(stopped in the middle)
Recorded time

By maintaining the $\overline{\text{ST}}$ pin at a low level, repeated playback is possible.


$\overline{\text{ST}}$ (I)
(Stop pulse)
$\overline{\text{SP}}$ (I)
MON (O)
1st playback
2nd playback
3rd playback

ROM Playback Method

(1) Apply a high level to the ROM pin.

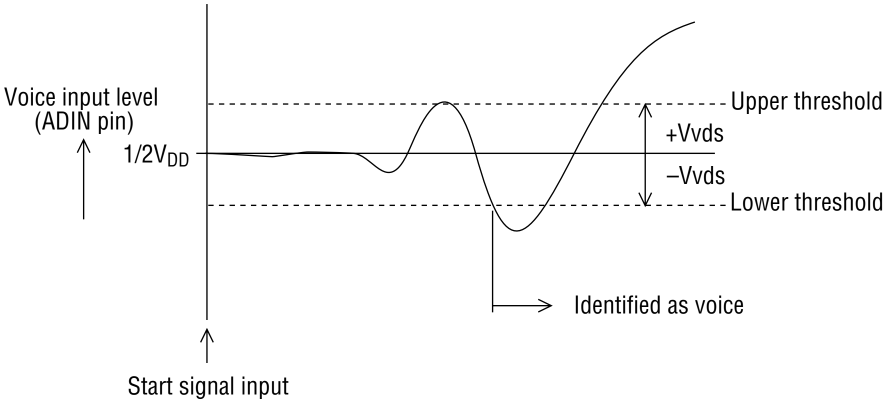
(2) Specify one of 63 phrases ch01 – ch3F by setting the CA0 – CA5 pins.

(3) To start playback, apply a low pulse to the $\overline{\text{ST}}$ pin. To stop playback in progress, apply a low pulse to the $\overline{\text{SP}}$ pin.

Voice Triggered Starting

This MSM6688 has the voice triggered starting function that starts recording when the level of voice input exceeds a preset amplitude. Using the voice activated function, the unvoiced part prior to voice detection will not be recorded, so that the memory capacity can be utilized efficiently.

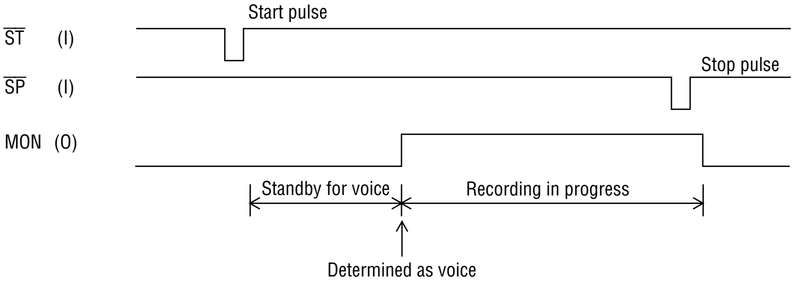
The unvoiced parts in the middle of recording are not eliminated. In the voice triggered starting mode, recording is started when a voice input exceeds the preset thresholds. Therefore, a consonant part with a low level may not be recorded.


Voice input level
(ADIN pin)
1/2V_DD
Upper threshold
+Vvds
–Vvds
Lower threshold
Identified as voice
Start signal input

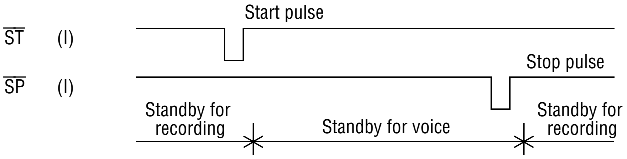
VDS pin	Voice triggered starting conditions
L	Voice triggered starting disabled
H	Voice triggered starting enabled Voice detection threshold Vvds = $V_{DD}/32$ (±160 mV)

The value in parentheses is for V_{DD} = 5.12V.

When a low level is applied to the $\overline{\text{ST}}$ pin, the MSM6688 goes to the standby state for voice. When detecting a voiced input, it starts recording and the MON pin outputs a high level.

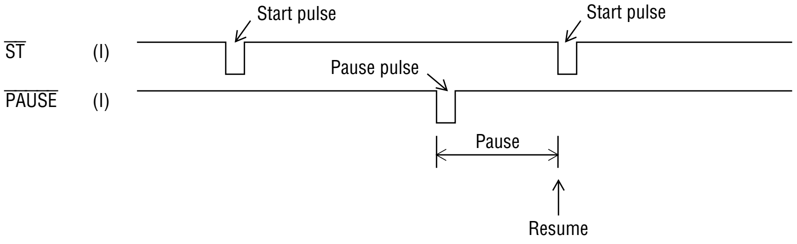

$\overline{\text{ST}}$ (I)
$\overline{\text{SP}}$ (I)
MON (O)
Start pulse
Stop pulse
Standby for voice
Recording in progress
Determined as voice

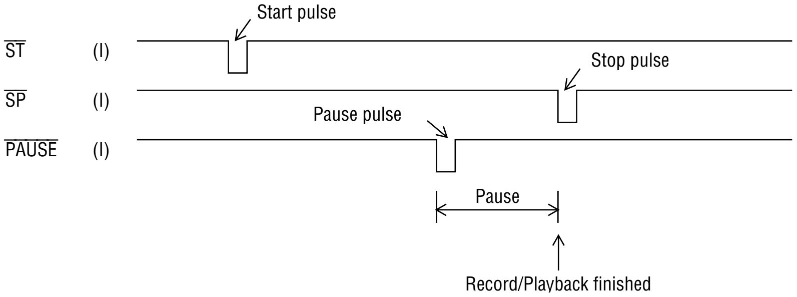
When a low level is applied to the $\overline{\text{SP}}$ pin during standby state for voice, the MSM6688 finishes the standby state for voice and goes to the standby state for recording.


$\overline{\text{ST}}$ (I)
$\overline{\text{SP}}$ (I)
Start pulse
Stop pulse
Standby for recording
Standby for voice
Standby for recording

Method of Temporarily Stopping Record/Playback by Pause Function

By applying a low pulse to the $\overline{\text{PAUSE}}$ pin during record/playback, record/playback operation can be stopped temporarily. To resume record/playback, apply a low pulse to the $\overline{\text{ST}}$ pin. To stop record/playback, apply a low pulse to the $\overline{\text{SP}}$ pin.

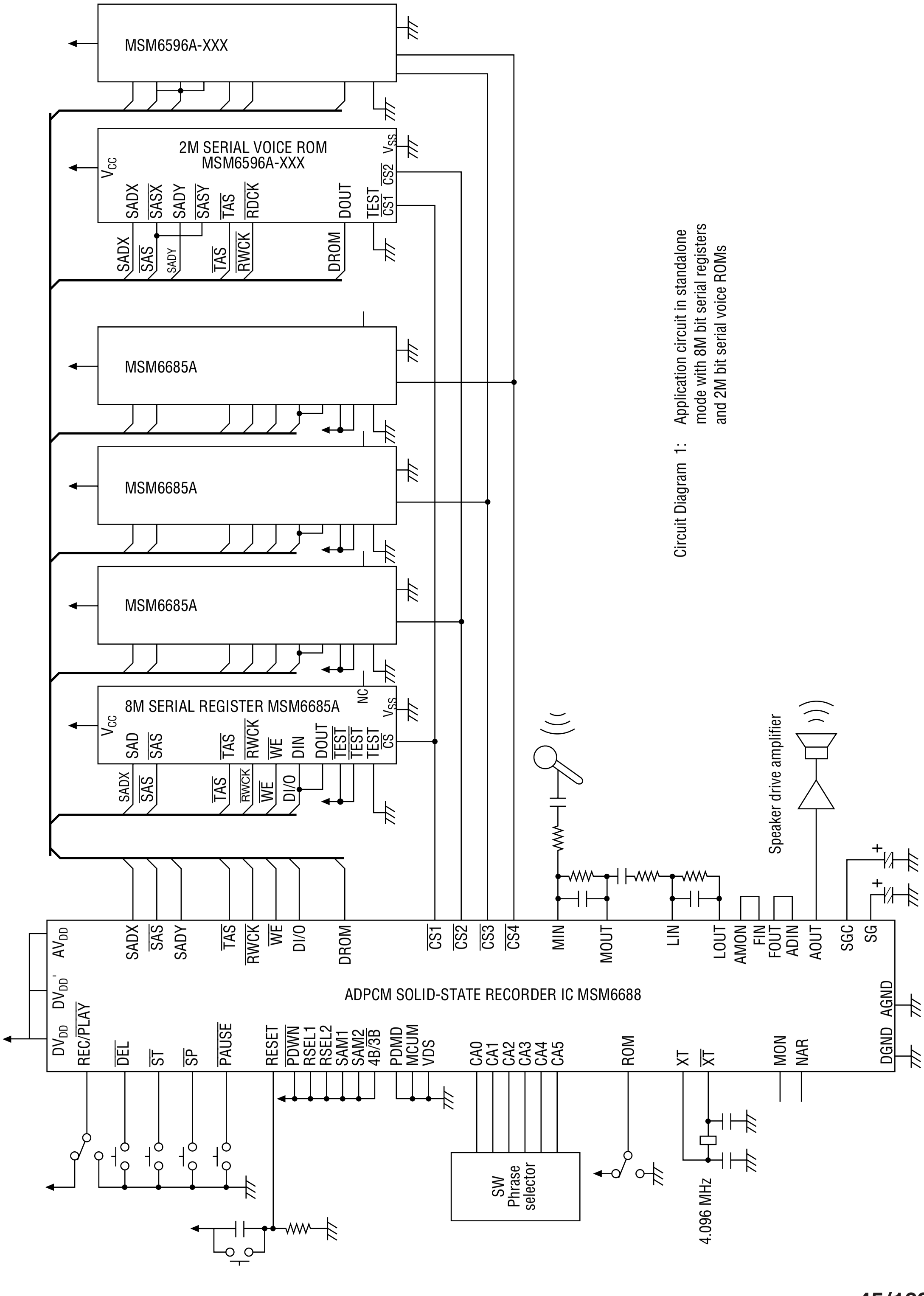

Start pulse
Start pulse
$\overline{\text{ST}}$ (I)
Pause pulse
$\overline{\text{PAUSE}}$ (I)
Pause
Resume


Start pulse
$\overline{\text{ST}}$ (I)
Stop pulse
$\overline{\text{SP}}$ (I)
Pause pulse
$\overline{\text{PAUSE}}$ (I)
Pause
Record/Playback finished

When record/playback is resumed after temporary stop, the voice triggered starting circuit is not operated and recording is started when a start low pulse is applied to $\overline{\text{SP}}$ pin.

APPLICATION CIRCUIT

The circuit diagram 1 shows an application circuit example where the MSM6688 is used in the stand-alone mode and four 8M bit serial registers and two 2M bit serial voice ROMs also connected.


MSM6596A-XXX
2M SERIAL VOICE ROM
MSM6596A-XXX
V_{CC}
SADX
SASX
SADY
SASY
TAS
RDCK
DOUT
TEST
CS1
CS2
V_{SS}
SADX
SAS
SADY
TAS
RWCK
DROM
MSM6685A
MSM6685A
MSM6685A
8M SERIAL REGISTER MSM6685A
NC
V_{CC}
SAD
SAS
TAS
RWCK
WE
DIN
DOUT
TEST
TEST
TEST
CS
V_{SS}
SADX
SAS
TAS
RWCK
WE
DI/O
ADPCM SOLID-STATE RECORDER IC MSM6688
DV_{DD}
DV_{DD}'
AV_{DD}
SADX
SAS
SADY
TAS
RWCK
WE
DI/O
DROM
CS1
CS2
CS3
CS4
MIN
MOUT
LIN
LOUT
AMON
FIN
FOUT
ADIN
AOUT
SGC
SG
REC/PLAY
DEL
ST
SP
PAUSE
RESET
PDWN
RSEL1
RSEL2
SAM1
SAM2
4B/3B
PDMD
MCUM
VDS
CA0
CA1
CA2
CA3
CA4
CA5
ROM
XT
XT
MON
NAR
DGND
AGND
SW
Phrase
selector
4.096 MHz
Speaker drive amplifier
+
+

Circuit Diagram 1: Application circuit in standalone mode with 8M bit serial registers and 2M bit serial voice ROMs

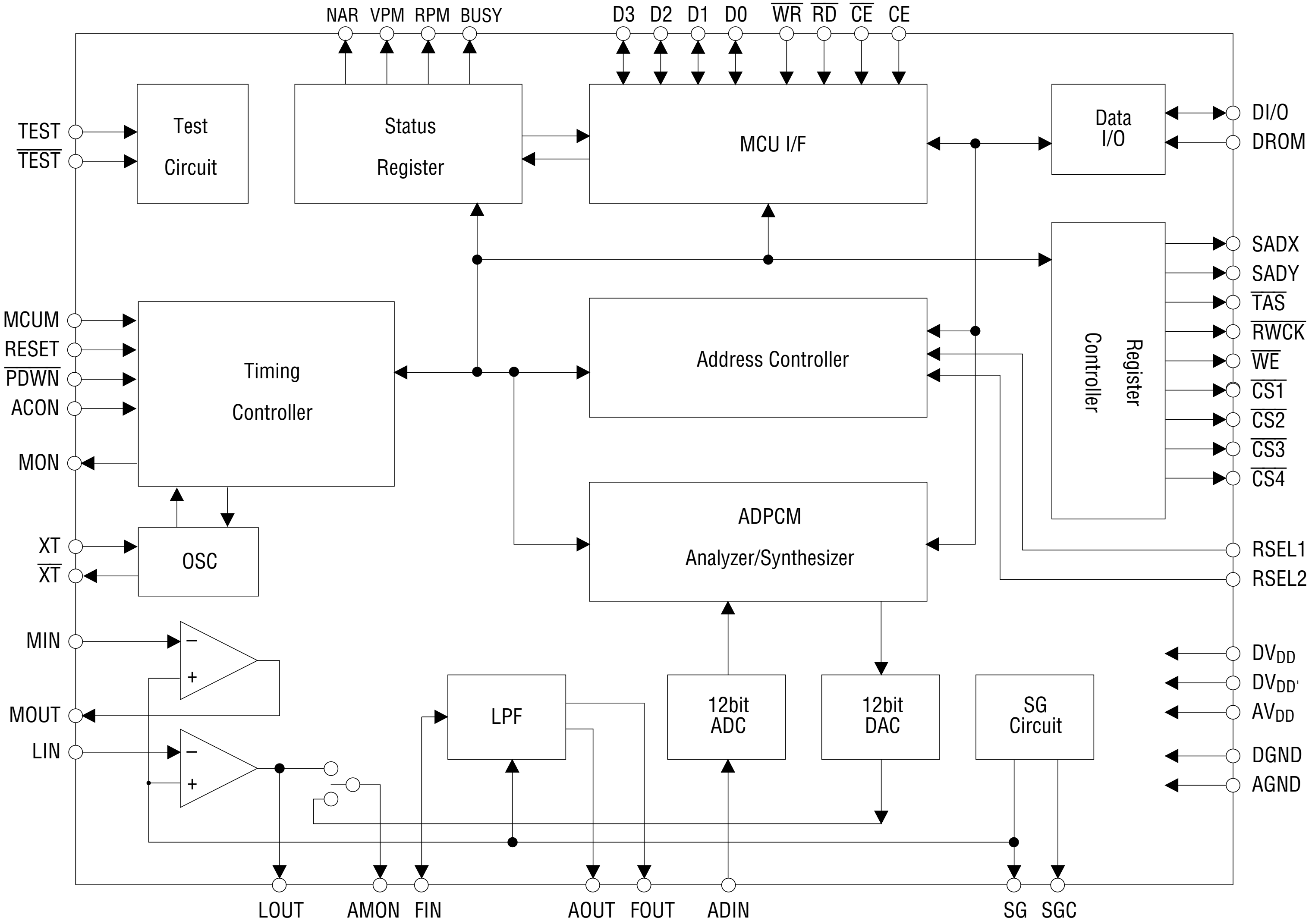
(2) MICROCONTROLLER INTERFACE MODE (for MSM6688 (5 V Version) and MSM6688L (3 V Version))

FEATURES

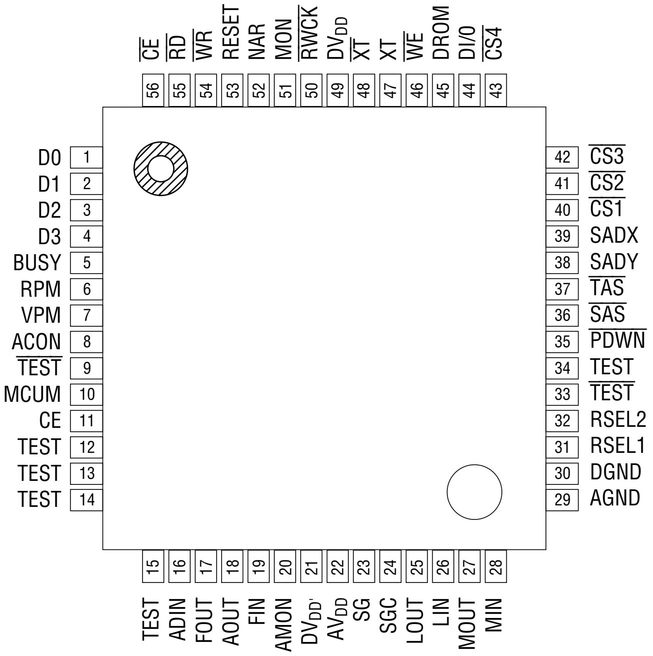
- 3-bit or 4-bit ADPCM
- Built-in 12-bit AD converter
- Built-in12-bit DA converter
- Built-in microphone amplifier
- Built-in low-pass filter
  Attenuation characteristics –40 dB/oct
- External only registers (for variable messages)
  MSM6688 (5 V version)
  - Serial registers, 32M bits maximum
    One 4M bit serial register (MSM6684B) can be driven directly
    Up to four 8M bit serial register (MSM6685A) can be driven directly
  MSM6688L (3 V version)
  - Serial registers, 4M bits maximum
    One 4M bit serial register (MSM66V84B) can be driven directly
- External only ROMs (for fixed messages)
  - Serial voice ROMs, 4M bits maximum
    1M bit serial voice ROM (MSM6595A) can be driven directly
    2M bit serial voice ROM (MSM6596A) can be driven directly
    3M bit serial voice ROM (MSM6597A) can be driven directly
- Sampling frequency
  4.0 kHz, 5.3 kHz, 6.4 kHz or 8.0 kHz (master clock frequency = 4.096 MHz)
  8.0 kHz, 10.6 kHz, 12.8 kHz or 16.0 kHz (master clock frequency = 8.192 MHz)
- Number of phrases
  63 phrases for variable messages
  63 phrases for fixed messages
- Maximum recording time (when external 32M bit RAM is connected)
  34 minutes (for 16 kbps ADPCM)
  23 minutes (for 24 kbps ADPCM)
  17 minutes (for 32 kbps ADPCM)
- Voice triggered starting function
- Pause function
- Master clock frequency: 4.096 MHz to 8.192 MHz
- Power supply voltage
  MSM6688: Single 5 Vpower supply
  MSM6688L: Single 3 V power supply
- Package options:

56-pin plastic QFP	(QFP56-P-910-0.65-2K)	(Product name: MSM6688GS-2K)
56-pin plastic QFP	(QFP56-P-910-0.65-2K)	(Product name: MSM6688LGS-2K)
64-pin plastic TQFP	(TQFP64-P-1010-0.50-K)	(Product name: MSM6688LTS-K)

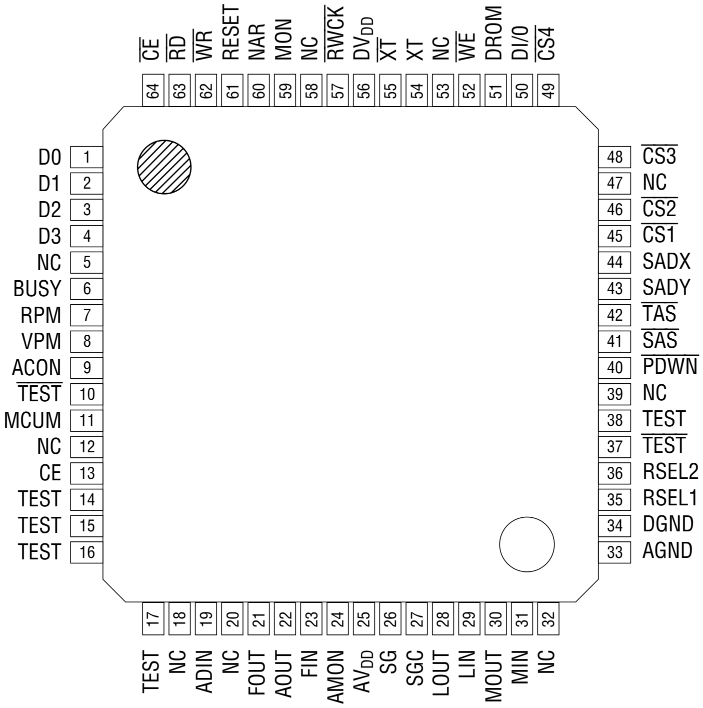
BLOCK DIAGRAM


NAR
VPM
RPM
BUSY
D3
D2
D1
D0
$\overline{WR}$
$\overline{RD}$
$\overline{CE}$
CE
TEST
$\overline{TEST}$
Test Circuit
Status Register
MCU I/F
Data I/O
DI/O
DROM
Register Controller
SADX
SADY
$\overline{TAS}$
$\overline{RWCK}$
$\overline{WE}$
$\overline{CS1}$
$\overline{CS2}$
$\overline{CS3}$
$\overline{CS4}$
MCUM
RESET
$\overline{PDWN}$
ACON
MON
Timing Controller
Address Controller
ADPCM Analyzer/Synthesizer
OSC
XT
$\overline{XT}$
RSEL1
RSEL2
MIN
MOUT
LIN
−
+
LPF
12bit ADC
12bit DAC
SG Circuit
DV_{DD}
$DV_{DD'}$
AV_{DD}
DGND
AGND
LOUT
AMON
FIN
AOUT
FOUT
ADIN
SG
SGC

PIN CONFIGURATION (TOP VIEW)


1 D0
2 D1
3 D2
4 D3
5 BUSY
6 RPM
7 VPM
8 ACON
9 TEST
10 MCUM
11 CE
12 TEST
13 TEST
14 TEST
15 TEST
16 ADIN
17 FOUT
18 AOUT
19 FIN
20 AMON
21 DVDD'
22 AVDD
23 SG
24 SGC
25 LOUT
26 LIN
27 MOUT
28 MIN
29 AGND
30 DGND
31 RSEL1
32 RSEL2
33 TEST
34 TEST
35 PDWN
36 SAS
37 TAS
38 SADY
39 SADX
40 CS1
41 CS2
42 CS3
43 CS4
44 DI/0
45 DROM
46 WE
47 XT
48 XT
49 DVDD
50 RWCK
51 MON
52 NAR
53 RESET
54 WR
55 RD
56 CE

56-Pin Plastic QFP


1 D0
2 D1
3 D2
4 D3
5 NC
6 BUSY
7 RPM
8 VPM
9 ACON
10 TEST
11 MCUM
12 NC
13 CE
14 TEST
15 TEST
16 TEST
17 TEST
18 NC
19 ADIN
20 NC
21 FOUT
22 AOUT
23 FIN
24 AMON
25 AVDD
26 SG
27 SGC
28 LOUT
29 LIN
30 MOUT
31 MIN
32 NC
33 AGND
34 DGND
35 RSEL1
36 RSEL2
37 TEST
38 TEST
39 NC
40 PDWN
41 SAS
42 TAS
43 SADY
44 SADX
45 CS1
46 CS2
47 NC
48 CS3
49 CS4
50 DI/0
51 DROM
52 WE
53 NC
54 XT
55 XT
56 DVDD
57 RWCK
58 NC
59 MON
60 NAR
61 RESET
62 WR
63 RD
64 CE

NC: No connection

64-Pin Plastic TQFP

PIN DESCRIPTIONS

Pin		Symbol	Type	Description
QFP	TQFP			
49	56	DV_{DD}	—	Digital power supply pin. Insert a bypass capacitor of 0.1μF or more between this pin and the DGND pin.
21	—	$DV_{DD'}$	—	Digital power supply pin
22	25	AV_{DD}	—	Analog power supply pin. Insert a bypass capacitor of 0.1μF or more between this pin and the AGND pin.
30	34	DGND	—	Digital ground pin
29	33	AGND	—	Analog ground pin
23 24	26 27	SG SGC	O	Output pin for analog circuit reference voltage (signal ground)
28 26	31 29	MIN LIN	I	Inverting input pin of the built-in OP amplifier. Non-inverting input pin is internally connected to SG (signal ground).
27 25	30 28	MOUT LOUT	O	MOUT and LOUT are output pins of the built-in OP amplifier for MIN and LIN, respectively.
20	24	AMON	O	This pin is connected to the LOUT pin in the recording mode and to the DA converter output in the playback mode. Used to connect the built-in LPF input (FIN pin).
19	23	FIN	I	Input pin of the built-in LPF.
17	21	FOUT	O	Output pin of the built-in LPF. Used to connect the AD converter input (ADIN pin)
16	19	ADIN	I	Input pin of the built-in 12-bit AD converter.
18	22	AOUT	O	Output pin of the built-in LPF. This pin outputs playback waveforms and used to connect an external speaker drive amplifier.
39 38	44 43	SADX SADY	O	(Serial Address Data). SADX is used to connect the SAD pin of each external serial register and the SADX pin of each external serial voice ROM. SADY is used to connect the SADY pin of each external serial voice ROM. Outputs of starting address of read/write.
36	41	$\overline{\text{SAS}}$	O	(Serial Address Strobe). Used to connect the $\overline{\text{SAS}}$ pin of external serial register and the $\overline{\text{SASX}}$ and $\overline{\text{SASY}}$ pins of external serial voice ROM Clock pin to write the serial address.
37	42	$\overline{\text{TAS}}$	O	(Transfer Address Strobe). Used to connect the $\overline{\text{TAS}}$ pin of each external serial register and serial voice ROM. This pin outputs address strobe outputs to set the serial address data from the SADX and SADY pins into the internal address counter of each serial register and serial voice ROM.
50	57	$\overline{\text{RWCK}}$	O	(Read/Write Clock). Used to connect the $\overline{\text{RWCK}}$ pin of each external serial register and the RDCK pin of each external serial voice ROM. This pin outputs a clock to read data from or write it into each external serial register.
46	52	$\overline{\text{WE}}$	O	(Write Enable) Used to connect the $\overline{\text{WE}}$ pin of each external serial register. This pin outputs $\overline{\text{WE}}$ signal to select either read or write mode.
44	50	DI/O	I/O	(Data I/O). Used to connect the DIN and DOUT pins of DRAM and serial register. This pin outputs the data to be written into the serial register or inputs the data read from the serial registers.
45	51	DROM	I	(Data ROM). Used to connect the DOUT pin of each external serial voiceROM.

<table>
<tr><th colspan="2">Pin</th><th rowspan="2">Symbol</th><th rowspan="2">Type</th><th rowspan="2">Description</th></tr>
<tr><th>QFP</th><th>TQFP</th></tr>
<tr><td>40
41
42
43</td><td>45
46
48
49</td><td>$\overline{CS1}$
$\overline{CS2}$
$\overline{CS3}$
$\overline{CS4}$</td><td>O</td><td>(Chip Select). Used to connect the $\overline{CS}$ pin of serial register and the $\overline{CS}$ ($\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$) pins of each serial voice ROM.</td></tr>
<tr><td>31
32</td><td>35
36</td><td>RSEL1
RSEL2</td><td>I</td><td>(Register Select). These are used to select the number of external serial registers.
<table>
<tr><td>RSEL2</td><td>L</td><td>L</td><td>H</td><td>H</td></tr>
<tr><td>RSEL1</td><td>L</td><td>H</td><td>L</td><td>H</td></tr>
<tr><td>Number of serial registers</td><td>1</td><td>2</td><td>3</td><td>4</td></tr>
</table></td></tr>
<tr><td>10</td><td>11</td><td>MCUM</td><td>I</td><td>This pin is used to select either the stand-alone mode or the microcontroller interface mode.
Low level: Stand-alone mode
High level: Microcontroller interface mode</td></tr>
<tr><td>53</td><td>61</td><td>RESET</td><td>I</td><td>A high input level at this pin causes the MSM6688/6688L to be initialized and to go into the power down state.</td></tr>
<tr><td>35</td><td>40</td><td>$\overline{PDWN}$</td><td>I</td><td>(Power Down). When a low level is input to this pin, the MSM6688 goes to the power down state. Unlike the RESET pin, this pin does not force to reset the MSM6688/6688L. When an low level is applied to this $\overline{PDWN}$ pin during recording operation, the MSM6688/6688L is halted, and will be maintained in the power down state while $\overline{PDWN}$ is low. After this pin is restored to a high level, postprocessing for recording will be performed.</td></tr>
<tr><td>1
2
3
4</td><td>1
2
3
4</td><td>D0
D1
D2
D3</td><td>I/O</td><td>Bi-directional data bus to transfer commands and data to and from an external microcontroller.</td></tr>
<tr><td>54</td><td>62</td><td>$\overline{WR}$</td><td>I</td><td>Write pulse input pin. Inputting a low pulse to this $\overline{WR}$ pin causes a command or data to be input via D0-D3 pins.</td></tr>
<tr><td>55</td><td>63</td><td>$\overline{RD}$</td><td>I</td><td>Read pulse input pin. Inputting a low pulse to this $\overline{RD}$ pin causes status bits or data to be output via D0-D3 pins.</td></tr>
<tr><td>56
11</td><td>64
13</td><td>$\overline{CE}$
CE</td><td>I</td><td>Chip enable input pins. When the $\overline{CE}$ pin is set to a low level or the CE pin is set to a high level, the write pulse ($\overline{WR}$), read pulse ($\overline{RD}$) can be accepted.
When the $\overline{CE}$ pin is set to a high level or CE pin is set to a low level, the write pulse ($\overline{WR}$) and read pulse ($\overline{RD}$) cannot be accepted so that data cannot be transferred to and from via D0-D3 pins.</td></tr>
<tr><td>5</td><td>6</td><td>BUSY</td><td>O</td><td>Outputs a high level while a command is being executed. When this pin is held high, do not apply any data to D0-D3 pins. The state of this BUSY pin is the same as the contents of the BUSY bit of the status register.</td></tr>
<tr><td>6</td><td>7</td><td>RPM</td><td>O</td><td>Outputs a high level during recording or playback operation. The state of this RPM is the same as the contents of the RPM bit of the status register.</td></tr>
<tr><td>7</td><td>8</td><td>VPM</td><td>O</td><td>Outputs a high level during the standby for voice after the start of voice triggered recording and the record/playback is stopped temporarily by inputting the PAUSE command. The state of this VPM pin is the same as the contents of the VPM bit of the status register.</td></tr>
</table>

Pin		Symbol	Type	Description
QFP	TQFP			
52	60	NAR	O	This NAR bit indicates whether the phrase designation by the CHAN command is enabled or disabled. In the ROM playback operation, specify the next phrase after making sure that the NAR output is high, and input the START command.
8	9	ACON	I	Used to select the use or nonuse of the pop noise suppression circuit at the analog output (AOUT) pin. When low level, the pop noise suppression circuit is not used. When high level, the pop noise suppression circuit is used.
47	54	XT	I	Used to connect an oscillator. When an external clock is used, input the clock through this pin. At the power down state, this pin must be set to the ground level.
48	55	$\overline{\text{XT}}$	O	Used to connect an oscillator, when an external clock is used, this pin must be left open.
51	59	MON	O	Outputs a high level while the record/playback operation is being performed. Outputs a synchronizing clock while record/playback activated by the EXT command is being performed.
12-15,34 9,33	14-17,38 10,37	TEST $\overline{\text{TEST}}$	I	Used to test the MSM6688/6688L. Input a low level to the TEST pin and a high level to the $\overline{\text{TEST}}$ pin.

ABSOLUTE MAXIMUM RATINGS (for MSM6688 (5 V Version))

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	Ta=25°C	–0.3 to +7.0	V
Input voltage	V_{IN}	Ta=25°C	–0.3 to V_{DD}+0.3	V
Storage temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (for MSM6688 (5 V Version))

Parameter	Symbol	Condition	Range	Unit
Power supply voltage	V_{DD}	DGND=AGND=0V	3.5 to 5.5 (Note 3)	V
Operating temperature	T_{op}	—	–40 to +85	°C
Master clock frequency	f_{OSC}	—	4.0 to 8.192	MHz

ELECTRICAL CHARACTERISTICS (for MSM6688 (5 V Version))

DC Characteristics

$DV_{DD}=DV_{DD}'=AV_{DD}$=4.5 to 5.5V (Note 3)
DGND=AGND=0V Ta=–40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High input voltage	V_{IH}	—	0.8×V_{DD}	—	—	V
Low input voltage	V_{IL}	—	—	—	0.2×V_{DD}	V
High output voltage	V_{OH}	I_{OH}=–40µA	V_{DD}–0.3	—	—	V
Low output voltage	V_{OL}	I_{OL}=2mA	—	—	0.45	V
High input current (Note 1)	I_{IH1}	$V_{IH}=V_{DD}$	—	—	10	µA
High input current (Note 2)	I_{IH2}	$V_{IH}=V_{DD}$	—	—	20	µA
Low input current (Note 1)	I_{IL1}	V_{IL}=GND	–10	—	—	µA
Low input current (Note 2)	I_{IL2}	V_{IL}=GND	–20	—	—	µA
Operating current consumption	I_{DD}	f_{OSC} = 8 MHz, no load	—	15	30	mA
Standby current consumption	I_{DDS}	During power down, no load, Ta=–40 to +70°C	—	—	10	µA
		During power down, no load, Ta=–40 to +85°C	—	—	50	µA

Note: 1. Applies to all input pins excluding the XT pin.
2. Applies to the XT pin.
3. Recording and playback should be performed at a power supply voltage of 4.5 to 5.5V. For other operations such as backup for a serial register, the IC operates at 3.5 to 5.5V.

Analog Characteristics

$DV_{DD}=DV_{DD'}=AV_{DD}$=4.5 to 5.5V
DGND=AGND=0V Ta=–40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
DA output relative error	$\lvert V_{DAE} \rvert$	no load	—	—	10	mV
FIN admissible input voltage range	V_{FIN}	—	1	—	$V_{DD}-1$	V
FIN input impedance	R_{FIN}	—	1	—	—	MΩ
ADIN admissible input voltage range	V_{ADIN}	—	0	—	V_{DD}	V
ADIN input impedance	R_{ADIN}	—	1	—	—	MΩ
Op-amp open loop gain	G_{OP}	f_{IN}=0 to 4kHz	40	—	—	dB
Op-amp input impedance	R_{INA}	—	1	—	—	MΩ
Op-amp load resistance	R_{OUTA}	—	200	—	—	kΩ
AOUT load resistance	R_{AOUT}	—	50	—	—	kΩ
FOUT load resistance	R_{FOUT}	—	50	—	—	kΩ

AC Characteristics

DV_{DD}=$DV_{DD'}$=AV_{DD}=4.5 to 5.5V
DGND=AGND=0V Ta=–40 to +85°C
fosc=4.096MHz f_{SAMP}=8.0kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
RESET pulse width		t_{RST}	1	—	—	µs
RESET execution time	(Note 1)*	t_{REX}	—	1	—	ms
$\overline{\text{PDWN}}$ low level time	*	t_{PDL}	500	—	—	µs
$\overline{\text{PDWN}}$ high level time	*	t_{PDH}	500	—	—	µs
Oscillating time after input of $\overline{\text{PDWN}}$	*	t_{PX}	125	—	500	µs
BUSY time after release of $\overline{\text{PDWN}}$	(Note 1)*	t_{BPD}	0.25	—	80	ms
$\overline{\text{RD}}$ pulse width		t_{RR}	200	—	—	ns
Setup and hold time of $\overline{\text{CE}}$ and CE for $\overline{\text{RD}}$		t_{CR}	30	—	—	ns
Time from $\overline{\text{RD}}$ fall to data valid		t_{DRE}	—	—	200	ns
Time from $\overline{\text{RD}}$ rise to data float		t_{DRF}	—	10	50	ns
$\overline{\text{WR}}$ pulse width		t_{WW}	200	—	—	ns
Setup and hold time of $\overline{\text{CE}}$ and CE for $\overline{\text{WR}}$		t_{CW}	30	—	—	ns
Data setup time to $\overline{\text{WR}}$ rise		t_{DWS}	100	—	—	ns
Data hold time from $\overline{\text{WR}}$ rise		t_{DWH}	30	—	—	ns
$\overline{\text{RD}}$ and $\overline{\text{WR}}$ disable time		t_{DRW}	250	—	—	ns
BUSY time after release of RESET	(Note 1)*	t_{BR}	—	—	1	ms
BUSY time after input of 1-nibble command	**	t_{B1}	—	—	16	µs
BUSY time after input of 2-nibble command	**	t_{B2}	—	—	16	µs
BUSY time after input of 3-nibble command	**	t_{B3}	—	—	16	µs
BUSY time after input of 2-nibble or 3-nibble command data	**	t_{BD}	—	—	16	µs
WAIT time after input of BLKRD command	*	t_{WBR}	270	—	—	µs
WAIT time after output of BLKRD command block data	*	t_{WDR}	50	—	—	µs
BUSY time after input of ADRWR command	*	t_{BAW}	—	—	270	µs
BUSY time after input of ADRWR command address data	*	t_{BAD}	—	—	50	µs
WAIT time after input of ADRRD command	*	t_{WAR}	270	—	—	µs
WAIT time after output of ADRRD command address data	*	t_{WDR}	50	—	—	µs
Address control time at start of record/playback	*	t_{AD1}	—	1	—	ms

Items with * are proportional to the period of master clock frequency fosc.
Items with ** are proportional to the period of the master clock frequency fosc, and are also proportional to the sampling frequency f_{SAMP} during record/playback.

Note: 1. The oscillation startup stabilization time is added to t_{REX}, t_{BPD} and t_{BR}.
The oscillation startup stabilization time is several tens of milliseconds for crystal oscillators and is several hundreds of microseconds for ceramic oscillators.

$DV_{DD}=DV_{DD'}=AV_{DD}=4.5$ to $5.5V$
$DGND=AGND=0V$ $Ta=-40$ to $+85°C$
$fosc=4.096MHz$ $f_{SAMP}=8.0kHz$

Parameter			Symbol	Min.	Typ.	Max.	Unit
Time from input of START command to MON rise	Flex record	*	t_{STCM}	—	—	50	ms
	Flex playback	*	t_{STCM}	—	—	20	ms
	Direct record/playback	*	t_{STCM}	—	—	1	ms
	ROM playback	*	t_{STCM}	—	—	1	ms
Time from input of STOP command to MON fall	Flex record	*	t_{SPCM}	—	—	80	ms
	Flex playback	*	t_{SPCM}	—	—	2	ms
	Direct record/playback	*	t_{SPCM}	—	—	2	ms
	ROM playback	*	t_{SPCM}	—	—	2	ms
Time from input of START command to setting of RPM bit		*	t_{STCR}	—	—	16	µs
Time from input of STOP command to end of record/playback		*	t_{SPCR}	—	—	2	ms
Time from input of STOP command to release of standby for voice	Flex record	*	t_{SPCV}	—	—	80	ms
	Direct record	*	t_{SPCV}	—	—	2	ms
Time from input of START command to NAR bit fall during continuos playback		*	t_{STCN}	—	—	16	µs
Unvoiced time between phrases during continuous playback		*	t_{MID}	—	1.25	—	ms
Time from input of PAUSE command to setting of VPM bit		**	t_{PSCP}	—	—	16	µs
Time from input of START command during pause to resetting of VPM bit		**	t_{STCP}	—	—	500	µs
Time from input of STOP command during pause to resetting of VPM bit		**	t_{SPCP}	—	—	500	µs
CHRW command	WAIT time after input of command	*	t_{WCRW}	770	—	—	µs
	WAIT time after input of REC command	*	t_{WRC}	16	—	—	µs
	WAIT time after input of write data	*	t_{WWD}	50	—	—	µs
	WAIT time after input of PLAY command	*	t_{WPL}	50	—	—	µs
	WAIT time after input of STOP command	*	t_{WSP}	50	—	—	µs
DTRW and DTRD commands	WAIT time after input of command	*	t_{WRW}	16	—	—	µs
	WAIT time after input of address (2nd–5th nibbles)	*	t_{WA1}	16	—	—	µs
	WAIT time after input of address (6th nibble)	*	t_{WA2}	270	—	—	µs
	WAIT time after input of REC command	*	t_{WRC}	16	—	—	µs
	WAIT time after input of write data	*	t_{WWD}	50	—	—	µs
	WAIT time after input of PLAY command	*	t_{WPL}	50	—	—	µs
	WAIT time after input of STOP command	*	t_{WSP}	16	—	—	µs

Items with * are proportional to the period of master clock frequency fosc.
Items with ** are proportional to the period of the master clock frequency fosc, and are also proportional to the sampling frequency f_{SAMP} during record/playback.

$DV_{DD}=DV_{DD}'=AV_{DD}=4.5V$ to $5.5V$
DGND=AGND=0V Ta=–40 to +85°C
fosc=4.096MHz $f_{SAMP}=8.0kHz$

Parameter		Symbol	Min.	Typ.	Max.	Unit
WAIT time for deletion of all phrases after input of DEL command *		t_{WBLA}	550	—	—	ms
WAIT time for deletion of a specified phase after input of DEL command *		t_{WBLI}	70	—	—	ms
Time to start of DC level transition after input of LEV command *		t_{LV}	—	—	16	µs
DC level transition time (GND to 1/2 V_{DD}) *		t_{AOR}	—	64	—	ms
DC level transition time (1/2 V_{DD} to GND) *		t_{AOF}	—	256	—	ms
EXT command	Time from input of EXT command to MON rise **	t_{EM}	—	—	330	µs
	MON high level time **	t_{MH}	—	31	—	µs
	MON low level time **	t_{ML}	—	94	—	µs
	Time from MON rise to $\overline{\text{RD}}$ pulse rise during recording **	t_{ERD}	—	—	120	µs
	Time from MON rise to $\overline{\text{WR}}$ pulse rise during playback **	t_{EWR}	—	—	120	µs
	Time from ADPCM data $\overline{\text{WR}}$ pulse to input of STOP command during playback **	t_{WE1}	16	—	—	µs
	Time from MON rise to input of STOP command **	t_{ESP}	—	—	100	µs
	Time from input of STOP command to end of record/playback **	t_{WEX}	—	—	250	µs

Items with * are proportional to the period of master clock frequency fosc.
Items with ** are proportional to the period of the master clock frequency fosc, and are also proportional to the sampling frequency f_{SAMP} during record/playback.

ABSOLUTE MAXIMUM RATINGS (for MSM6688L (3 V Version))

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	Ta=25°C	–0.3 to +7.0	V
Input voltage	V_{IN}	Ta=25°C	–0.3 to V_{DD}+0.3	V
Storage temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (for MSM6688L (3 V Version))

Parameter	Symbol	Condition	Range	Unit
Power supply voltage	V_{DD}	DGND=AGND=0V	2.7 to 3.6	V
Operating temperature	T_{op}	—	–40 to +85	°C
Master clock frequency	fosc	—	4.0 to 8.192	MHz

ELECTRICAL CHARACTERISTICS (for MSM6688L (3 V Version))

DC Characteristics

$DV_{DD}=DV_{DD}'=AV_{DD}$=2.7 to 3.6V
DGND=AGND=0V Ta=–40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High input voltage	V_{IH}	—	0.85×V_{DD}	—	—	V
Low input voltage	V_{IL}	—	—	—	0.15×V_{DD}	V
High output voltage	V_{OH}	I_{OH}=–40µA	V_{DD}–0.3	—	—	V
Low output voltage	V_{OL}	I_{OL}=2mA	—	—	0.45	V
High input current (Note 1)	I_{IH1}	$V_{IH}=V_{DD}$	—	—	10	µA
High input current (Note 2)	I_{IH2}	$V_{IH}=V_{DD}$	—	—	20	µA
Low input current (Note 1)	I_{IL1}	V_{IL}=GND	-10	—	—	µA
Low input current (Note 2)	I_{IL2}	V_{IL}=GND	-20	—	—	µA
Operating current consumption	I_{DD}	f_{OSC} = 8 MHz, no load	—	15	30	mA
Standby current consumption	I_{DDS}	During power down, no load, Ta=–40 to +70°C	—	—	15	µA
		During power down, no load, Ta=–40 to +85°C	—	—	100	µA

Note: 1. Applies to all input pins excluding the XT pin.
2. Applies to the XT pin.

Analog Characteristics

DV_{DD}=$DV_{DD'}$=AV_{DD}=2.7 to 3.6V
DGND=AGND=0V Ta=–40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
DA output relative error	$\lvert V_{DAE} \rvert$	no load	—	—	10	mV
FIN admissible input voltage range	V_{FIN}	—	1/4×V_{DD}	—	3/4×V_{DD}	V
FIN input impedance	R_{FIN}	—	1	—	—	MΩ
ADIN admissible input voltage range	V_{ADIN}	—	0	—	V_{DD}	V
ADIN input impedance	R_{ADIN}	—	1	—	—	MΩ
Op-amp open loop gain	G_{OP}	f_{IN}=0 to 4kHz	40	—	—	dB
Op-amp input impedance	R_{INA}	—	1	—	—	MΩ
Op-amp load resistance	R_{OUTA}	—	200	—	—	kΩ
AOUT load resistance	R_{AOUT}	—	50	—	—	kΩ
FOUT load resistance	R_{FOUT}	—	50	—	—	kΩ

AC Characteristics

$DV_{DD}=DV_{DD'}=AV_{DD}=2.7$ to 3.6V
DGND=AGND=0V Ta=–40 to +85°C
fosc=4.096MHz $f_{SAMP}=8.0$kHz

Parameter	Symbol	Min.	Typ.	Max.	Unit
RESET pulse width	t_{RST}	1	—	—	µs
RESET execution time (Note 1)*	t_{REX}	—	1	—	ms
$\overline{\text{PDWN}}$ low level time *	t_{PDL}	500	—	—	µs
$\overline{\text{PDWN}}$ high level time *	t_{PDH}	500	—	—	µs
Oscillating time after input of $\overline{\text{PDWN}}$ *	t_{PX}	125	—	500	µs
BUSY time after release of $\overline{\text{PDWN}}$ (Note 1)*	t_{BPD}	0.25	—	80	ms
$\overline{\text{RD}}$ pulse width	t_{RR}	200	—	—	ns
Setup and hold time of $\overline{\text{CE}}$ and CE for $\overline{\text{RD}}$	t_{CR}	30	—	—	ns
Time from $\overline{\text{RD}}$ fall to data valid	t_{DRE}	—	—	200	ns
Time from $\overline{\text{RD}}$ rise to data float	t_{DRF}	—	10	50	ns
$\overline{\text{WR}}$ pulse width	t_{WW}	200	—	—	ns
Setup and hold time of $\overline{\text{CE}}$ and CE for $\overline{\text{WR}}$	t_{CW}	30	—	—	ns
Data setup time to $\overline{\text{WR}}$ rise	t_{DWS}	100	—	—	ns
Data hold time from $\overline{\text{WR}}$ rise	t_{DWH}	30	—	—	ns
$\overline{\text{RD}}$ and $\overline{\text{WR}}$ disable time	t_{DRW}	250	—	—	ns
BUSY time after release of RESET (Note 1)*	t_{BR}	—	—	1	ms
BUSY time after input of 1-nibble command **	t_{B1}	—	—	16	µs
BUSY time after input of 2-nibble command **	t_{B2}	—	—	16	µs
BUSY time after input of 3-nibble command **	t_{B3}	—	—	16	µs
BUSY time after input of 2-nibble or 3-nibble command data**	t_{BD}	—	—	16	µs
WAIT time after input of BLKRD command *	t_{WBR}	270	—	—	µs
WAIT time after output of BLKRD command block data *	t_{WDR}	50	—	—	µs
BUSY time after input of ADRWR command *	t_{BAW}	—	—	270	µs
BUSY time after input of ADRWR command address data *	t_{BAD}	—	—	50	µs
WAIT time after input of ADRRD command *	t_{WAR}	270	—	—	µs
WAIT time after output of ADRRD command address data *	t_{WDR}	50	—	—	µs
Address control time at start of record/playback *	t_{AD1}	—	1	—	ms

Items with * are proportional to the period of master clock frequency fosc.
Items with ** are proportional to the period of the master clock frequency fosc, and are also proportional to the sampling frequency f_{SAMP} during record/playback.

Note: 1. The oscillation startup stabilization time is added to t_{REX}, t_{BPD} and t_{BR}.
The oscillation startup stabilization time is several tens of milliseconds for crystal oscillators and is several hundreds of microseconds for ceramic oscillators.

$DV_{DD}=DV_{DD'}=AV_{DD}=2.7$ to 3.6V
DGND=AGND=0V Ta=–40 to +85°C
fosc=4.096MHz $f_{SAMP}=8.0kHz$

Parameter		Symbol	Min.	Typ.	Max.	Unit
Time from input of START command to MON rise	Flex record *	t_{STCM}	—	—	50	ms
	Flex playback *	t_{STCM}	—	—	20	ms
	Direct record/playback *	t_{STCM}	—	—	1	ms
	ROM playback *	t_{STCM}	—	—	1	ms
Time from input of STOP command to MON fall	Flex record *	t_{SPCM}	—	—	80	ms
	Flex playback *	t_{SPCM}	—	—	2	ms
	Direct record/playback *	t_{SPCM}	—	—	2	ms
	ROM playback *	t_{SPCM}	—	—	2	ms
Time from input of START command to setting of RPM bit *		t_{STCR}	—	—	16	µs
Time from input of STOP command to end of record/playback *		t_{SPCR}	—	—	2	ms
Time from input of STOP command to release of standby for voice	Flex record *	t_{SPCV}	—	—	80	ms
	Direct record *	t_{SPCV}	—	—	2	ms
Time from input of START command to NAR bit fall during continuos playback *		t_{STCN}	—	—	16	µs
Unvoiced time between phrases during continuous playback*		t_{MID}	—	1.25	—	ms
Time from input of PAUSE command to setting of VPM bit **		t_{PSCP}	—	—	16	µs
Time from input of START command during pause to resetting of VPM bit **		t_{STCP}	—	—	500	µs
Time from input of STOP command during pause to resetting of VPM bit **		t_{SPCP}	—	—	500	µs
CHRW command	WAIT time after input of command *	t_{WCRW}	770	—	—	µs
	WAIT time after input of REC command *	t_{WRC}	16	—	—	µs
	WAIT time after input of write data *	t_{WWD}	50	—	—	µs
	WAIT time after input of PLAY command *	t_{WPL}	50	—	—	µs
	WAIT time after input of STOP command *	t_{WSP}	50	—	—	µs
DTRW and DTRD commands	WAIT time after input of command *	t_{WRW}	16	—	—	µs
	WAIT time after input of address (2nd–5th nibbles) *	t_{WA1}	16	—	—	µs
	WAIT time after input of address (6th nibble) *	t_{WA2}	270	—	—	µs
	WAIT time after input of REC command *	t_{WRC}	16	—	—	µs
	WAIT time after input of write data *	t_{WWD}	50	—	—	µs
	WAIT time after input of PLAY command *	t_{WPL}	50	—	—	µs
	WAIT time after input of STOP command *	t_{WSP}	16	—	—	µs

Items with * are proportional to the period of master clock frequency fosc.
Items with ** are proportional to the period of the master clock frequency fosc, and are also proportional to the sampling frequency f_{SAMP} during record/playback.

$DV_{DD}=DV_{DD'}=AV_{DD}=2.7V$ to $3.6V$
$DGND=AGND=0V$ Ta=–40 to +85°C
fosc=4.096MHz $f_{SAMP}=8.0kHz$

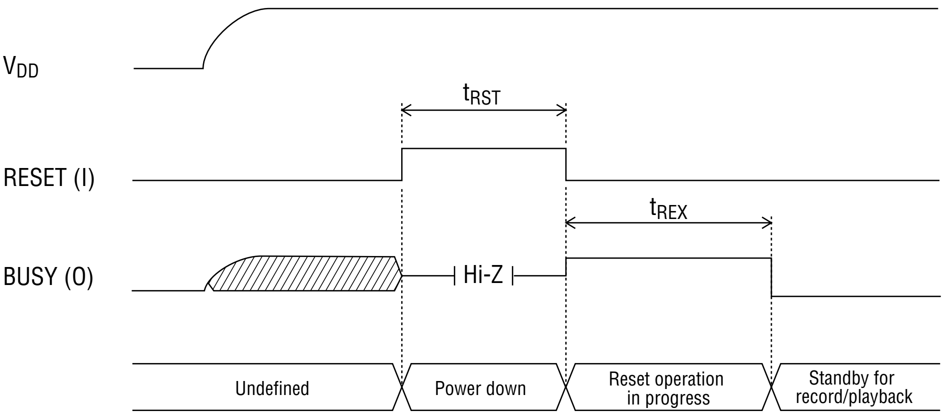
Parameter			Symbol	Min.	Typ.	Max.	Unit
WAIT time for deletion of all phrases after input of DEL command		*	t_{WBLA}	550	—	—	ms
WAIT time for deletion of a specified phase after input of DEL command		*	t_{WBLI}	70	—	—	ms
Time to start of DC level transition after input of LEV command		*	t_{LV}	—	—	16	µs
DC level transition time (GND to 1/2 V_{DD})		*	t_{AOR}	—	64	—	ms
DC level transition time (1/2 V_{DD} to GND)		*	t_{AOF}	—	256	—	ms
EXT command	Time from input of EXT command to MON rise	**	t_{EM}	—	—	330	µs
	MON high level time	**	t_{MH}	—	31	—	µs
	MON low level time	**	t_{ML}	—	94	—	µs
	Time from MON rise to RD pulse rise during recording	**	t_{ERD}	—	—	120	µs
	Time from MON rise to WR pulse rise during playback	**	t_{EWR}	—	—	120	µs
	Time from ADPCM data $\overline{WR}$ pulse to input of STOP command during playback	**	t_{WE1}	16	—	—	µs
	Time from MON rise to input of STOP command	**	t_{ESP}	—	—	100	µs
	Time from input of STOP command to end of record/playback	**	t_{WEX}	—	—	250	µs

Items with * are proportional to the period of master clock frequency fosc.

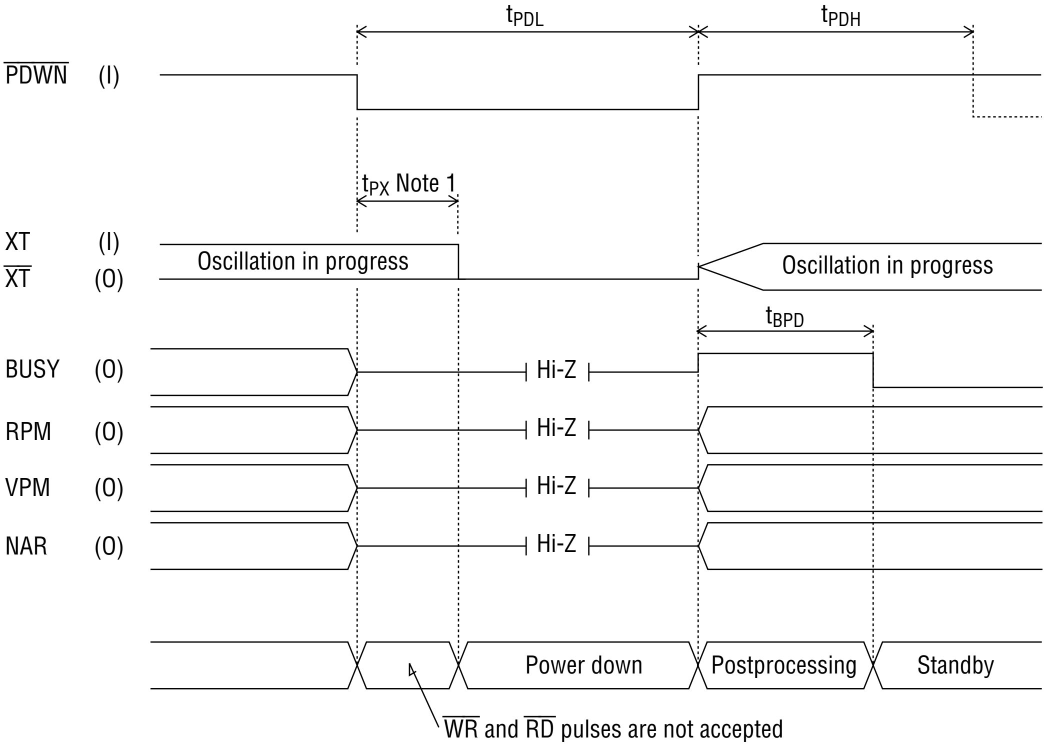
Items with ** are proportional to the period of the master clock frequency fosc, and are also proportional to the sampling frequency f_{SAMP} during record/playback.

TIMING DIAGRAMS

Reset Function

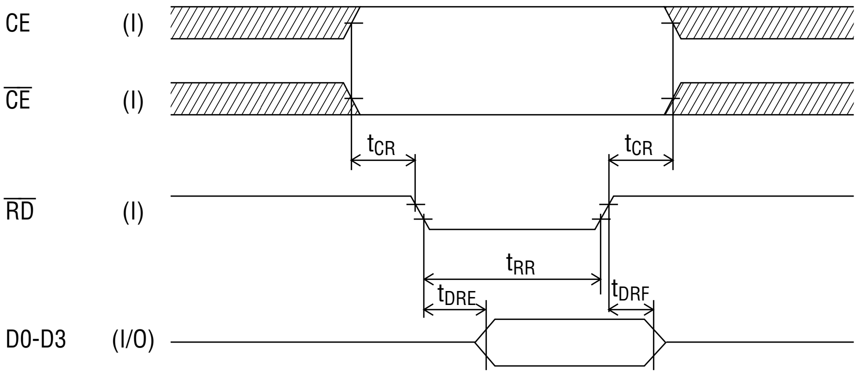

VDD
tRST
RESET (I)
tREX
BUSY (O)
Hi-Z
Undefined
Power down
Reset operation in progress
Standby for record/playback

Power Down by the $\overline{\text{PDWN}}$ pin

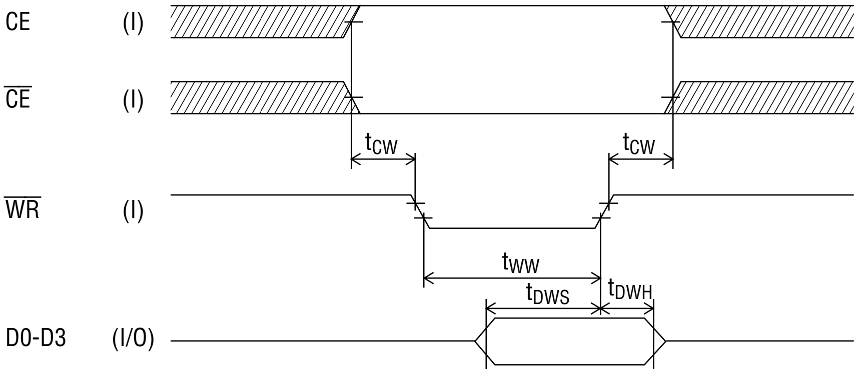

tPDL
tPDH
PDWN (I)
tPX Note 1
XT (I)
XT (O)
Oscillation in progress
Oscillation in progress
tBPD
BUSY (O)
RPM (O)
VPM (O)
NAR (O)
Hi-Z
Hi-Z
Hi-Z
Hi-Z
Power down
Postprocessing
Standby
WR and RD pulses are not accepted

Note: 1. When an external clock is used, apply a low level to the $\overline{\text{PDWN}}$ pin and then continue to apply the external clock to the XT pin for t_{PX}.

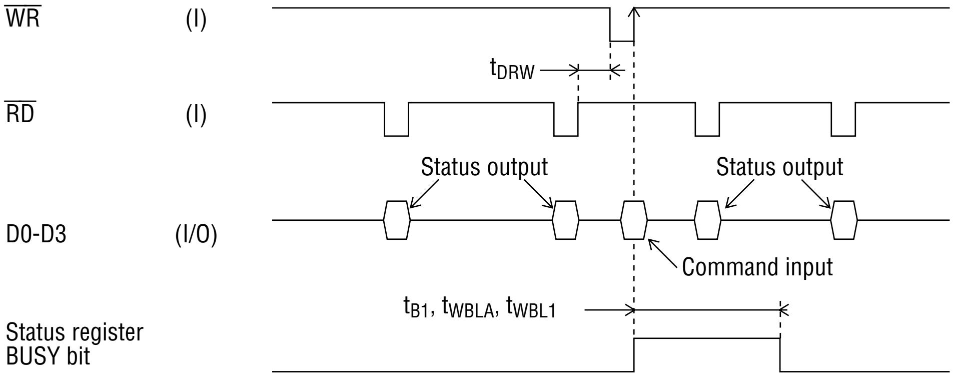
Data Read Timing ($\overline{\text{RD}}$ Pulse)


CE (I)
$\overline{\text{CE}}$ (I)
t_{CR}
t_{CR}
$\overline{\text{RD}}$ (I)
t_{RR}
t_{DRE}
t_{DRF}
D0-D3 (I/O)

Data Write Timing ($\overline{\text{WR}}$ Pules)

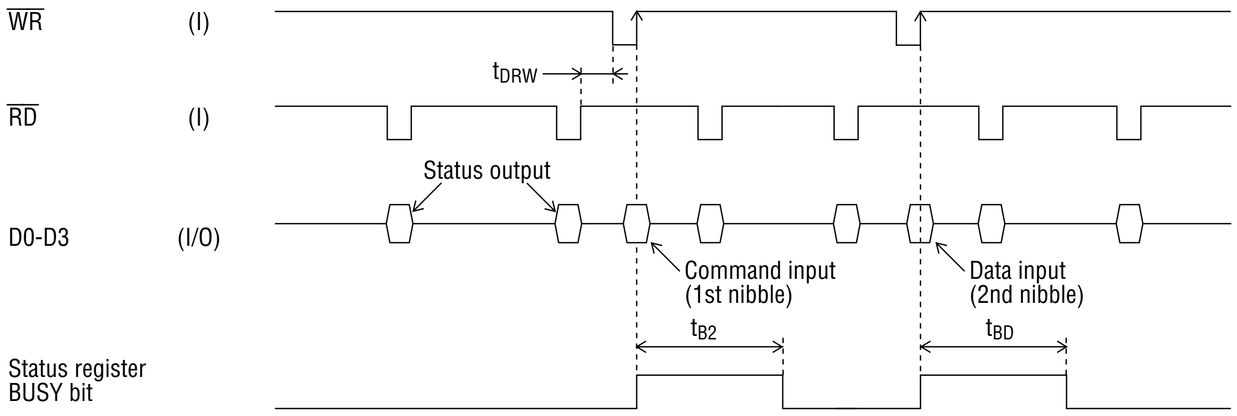

CE (I)
$\overline{\text{CE}}$ (I)
t_{CW}
t_{CW}
$\overline{\text{WR}}$ (I)
t_{WW}
t_{DWS}
t_{DWH}
D0-D3 (I/O)

Inputting 1-Nibble Commands (NOP, PAUSE, PLAY, REC, START, STOP and DEL Commands)


WR
(I)
tDRW
RD
(I)
Status output
Status output
D0-D3
(I/O)
Command input
tB1, tWBLA, tWBL1
Status register
BUSY bit

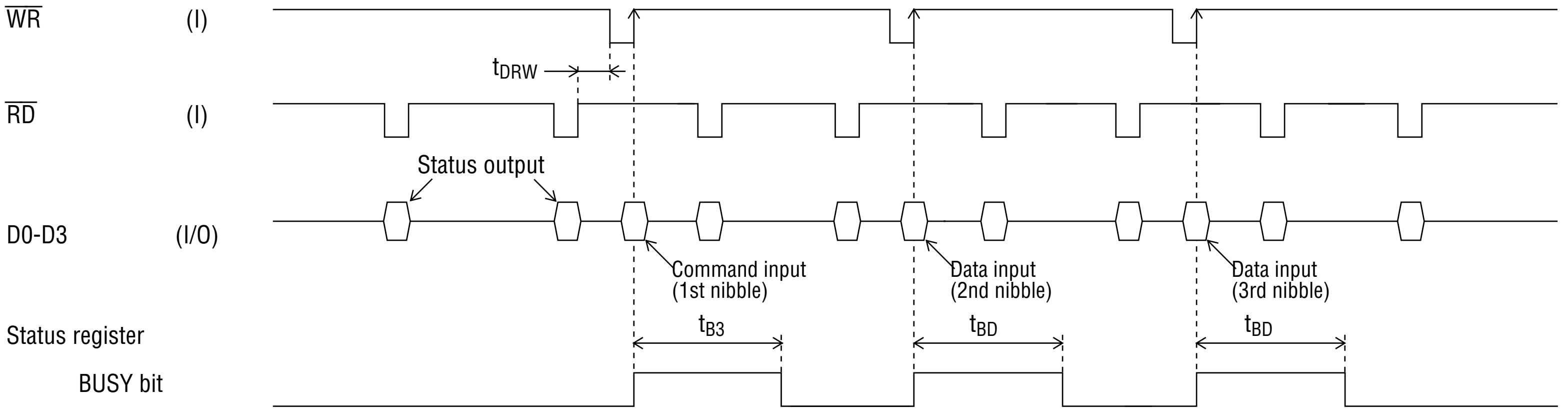
t_{B1}: NOP, PAUSE, PLAY, REC, START, and STOP commands
t_{WBLA}: DEL command (deletion of all phrases)
t_{WBL1}: DEL command (deletion of a specified phrase)

Inputting 2-Nibble Commands (SAMP, VDS, and LEV Commands)

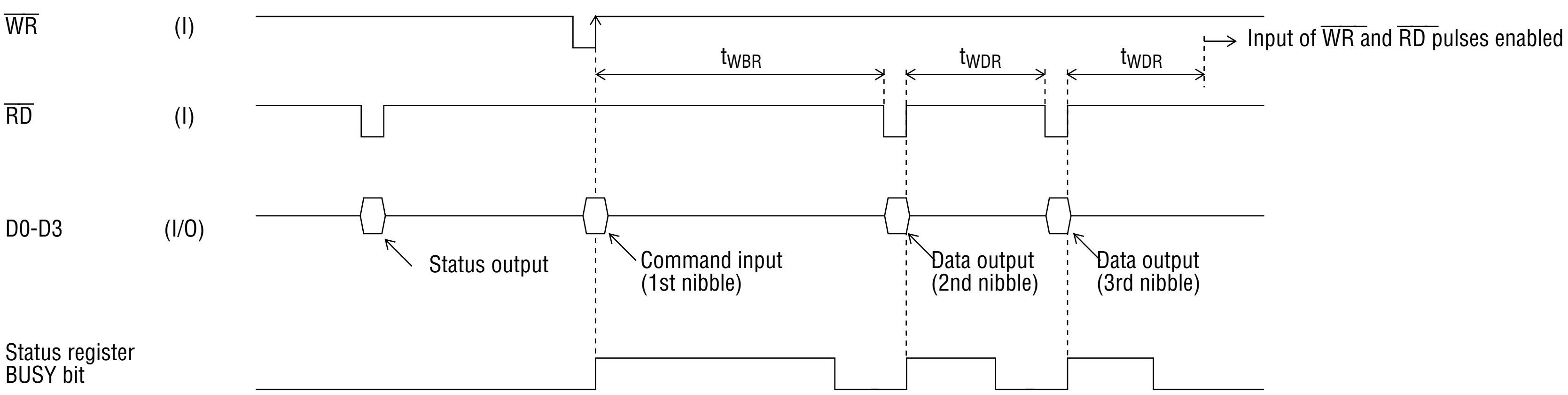

$\overline{WR}$
(I)
t_{DRW}
$\overline{RD}$
(I)
Status output
D0-D3
(I/O)
Command input
(1st nibble)
Data input
(2nd nibble)
t_{B2}
t_{BD}
Status register
BUSY bit

The LEV command is used to specify the playback level.
See the timing diagram for
DC level transition by the LEV command.

Inputting 3-Nibble Commands (CHAN and BLKWR Commands)

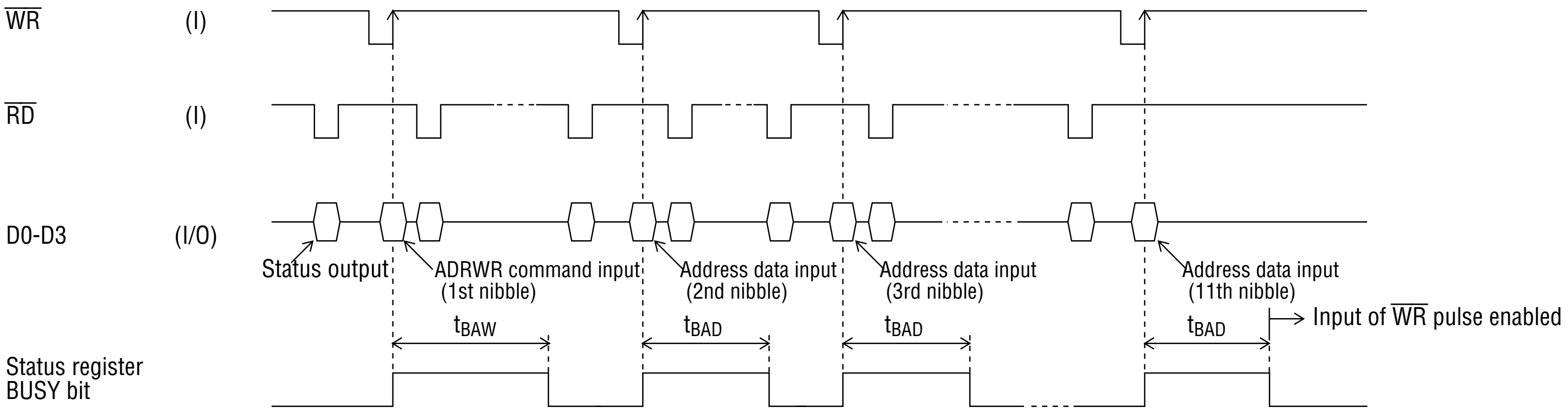

$\overline{WR}$ (I)
t_{DRW}
$\overline{RD}$ (I)
Status output
D0-D3 (I/O)
Command input (1st nibble)
Data input (2nd nibble)
Data input (3rd nibble)
Status register
BUSY bit
t_{B3}
t_{BD}
t_{BD}

Inputting the BLKRD Command


$\overline{WR}$ (I)
$\overline{RD}$ (I)
D0-D3 (I/O)
Status register BUSY bit
t_{WBR}
t_{WDR}
t_{WDR}
Input of $\overline{WR}$ and $\overline{RD}$ pulses enabled
Status output
Command input (1st nibble)
Data output (2nd nibble)
Data output (3rd nibble)

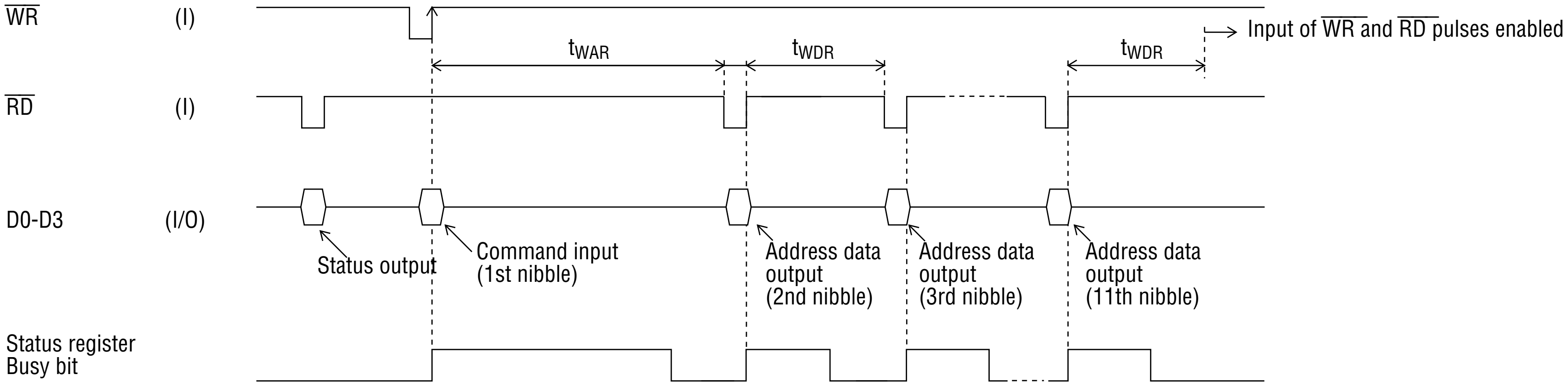
1. After making sure that the MSM6688/6688L is not in the busy state by checking the BUSY bit of the status register, input the BLKRD command.
2. Then, the data is read according to the 2nd and 3rd nibble command.
   However, the status of the BUSY bit cannot be verified by inputting the $\overline{RD}$ pulse. Therefore, input the $\overline{RD}$ pulse either after the waiting time t_{WBR} or t_{WDR} or after verifying the BUSY state at BUSY output pin.

Inputting the ADRWR Command


$\overline{\text{WR}}$ (I)
$\overline{\text{RD}}$ (I)
D0-D3 (I/O)
Status register BUSY bit
Status output
ADRWR command input (1st nibble)
Address data input (2nd nibble)
Address data input (3rd nibble)
Address data input (11th nibble)
t_{BAW}
t_{BAD}
t_{BAD}
t_{BAD}
Input of $\overline{\text{WR}}$ pulse enabled

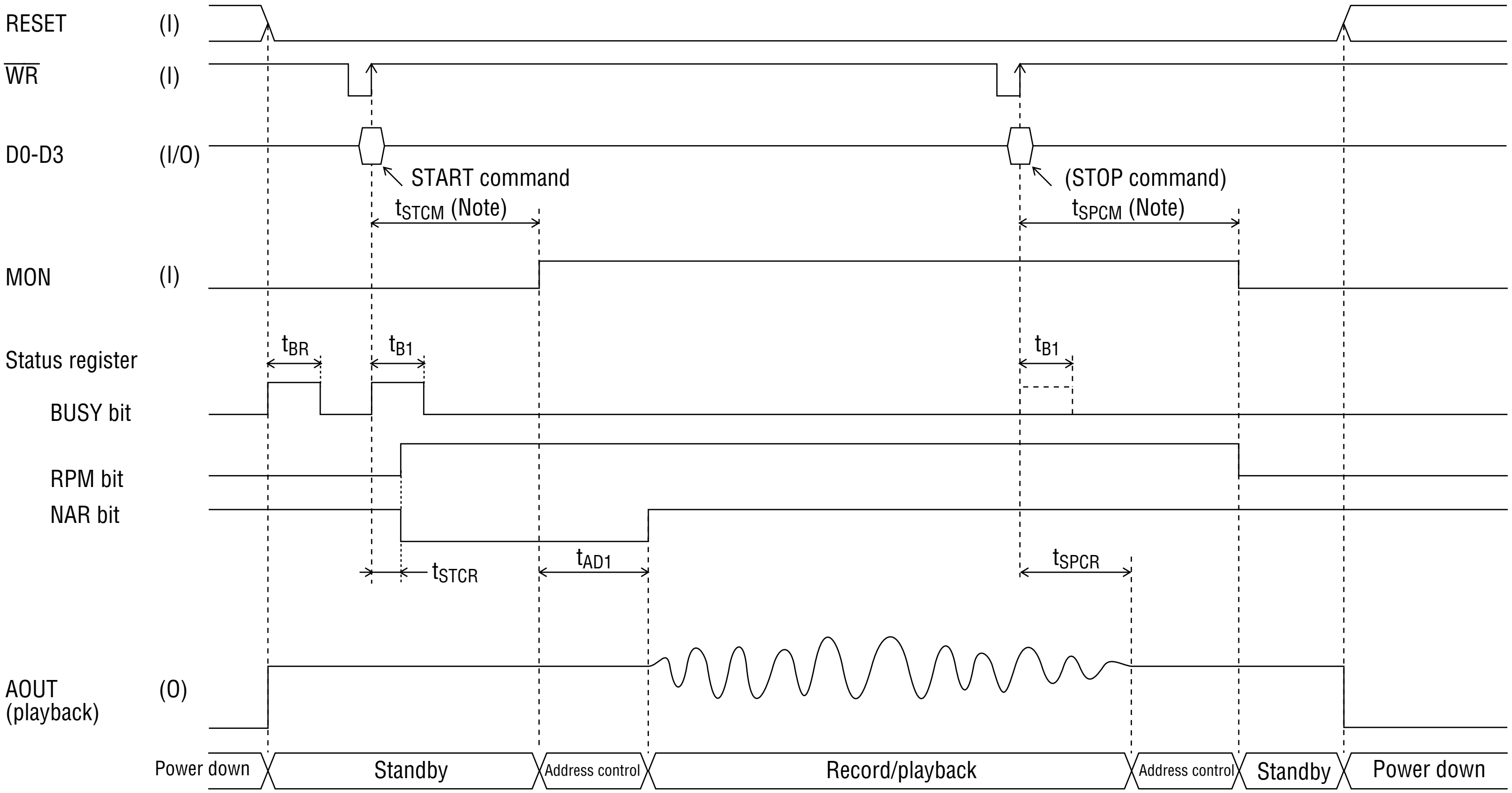
1. After making sure that the MSM6688/6688L is not in the busy state by checking the BUSY bit of the status register, input the ADRWR command.
2. Then, input 2nd-11th nibble address data after making sure that the MSM6688 is not in the BUSY state by one of the following two methods.
   - Check of the BUSY bit in the status register
   - Input the next $\overline{\text{WR}}$ pulse after the waiting time t_{BAW} or t_{BAD}.

Inputting the ADRRD Command


$\overline{WR}$ (I)
$\overline{RD}$ (I)
D0-D3 (I/O)
Status register Busy bit
t_{WAR}
t_{WDR}
t_{WDR}
Input of $\overline{WR}$ and $\overline{RD}$ pulses enabled
Status output
Command input (1st nibble)
Address data output (2nd nibble)
Address data output (3rd nibble)
Address data output (11th nibble)

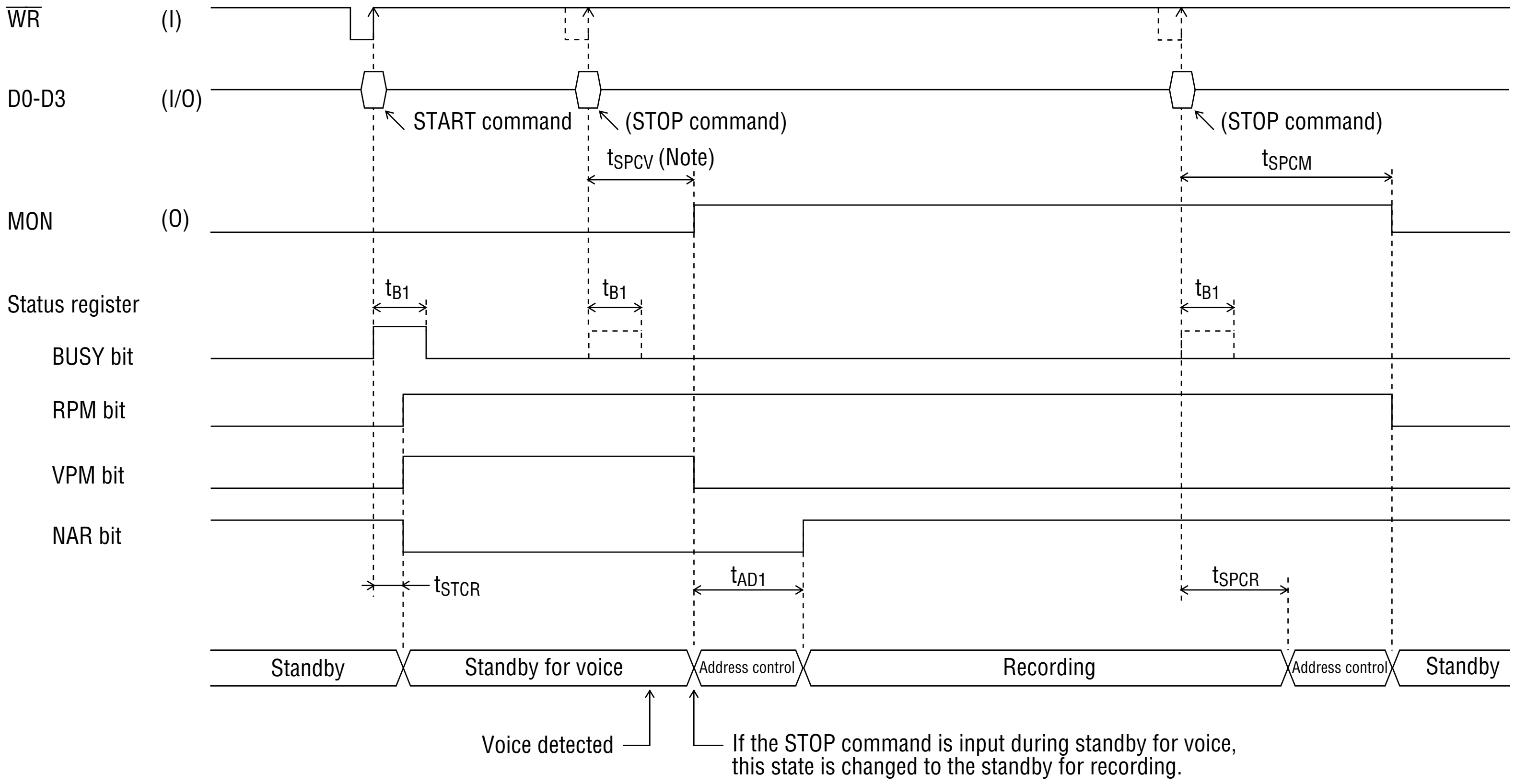
1. After making sure that the MSM6688/6688L is not in the busy state by checking the BUSY bit of the status register, input the ADRRD command.
2. Then, the address data is read according to 2nd through 11th nibble command.
   The state of the BUSY bit cannot be checked by the $\overline{RD}$ pulse.
   Therefore, input the $\overline{RD}$ pulse either after the waiting time t_{WAR} or t_{WDR} or after verifying the BUSY state at the BUSY output pin.

Timing for Record/Playback by START Command


RESET (I)
WR (I)
D0-D3 (I/O)
START command
t_{STCM} (Note)
(STOP command)
t_{SPCM} (Note)
MON (I)
Status register
BUSY bit
RPM bit
NAR bit
t_{BR}
t_{B1}
t_{B1}
t_{STCR}
t_{AD1}
t_{SPCR}
AOUT (playback) (O)
Power down
Standby
Address control
Record/playback
Address control
Standby
Power down

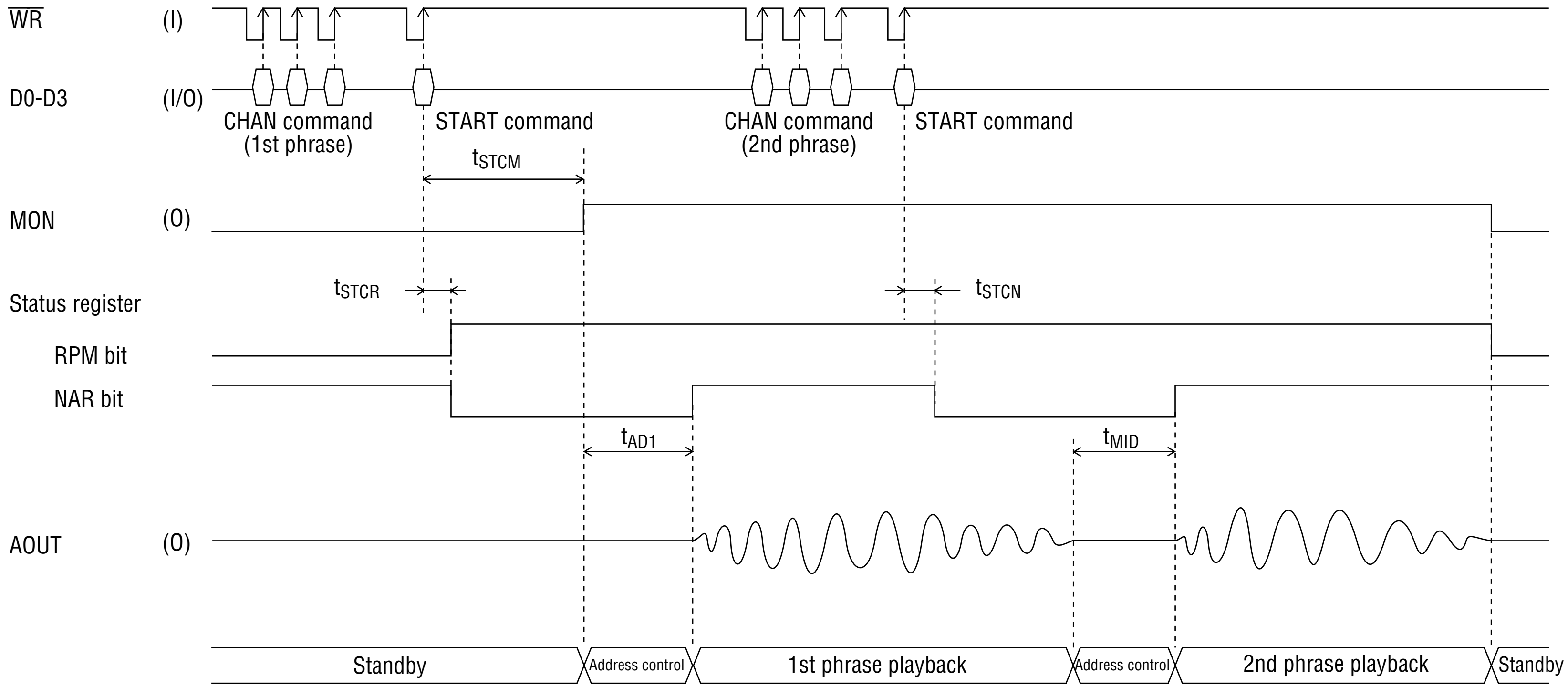
Note: t_{STCM} and t_{SPCM} vary depending on the control mode for record/playback and on record or playback mode.

Timing for Voice Triggered Recording

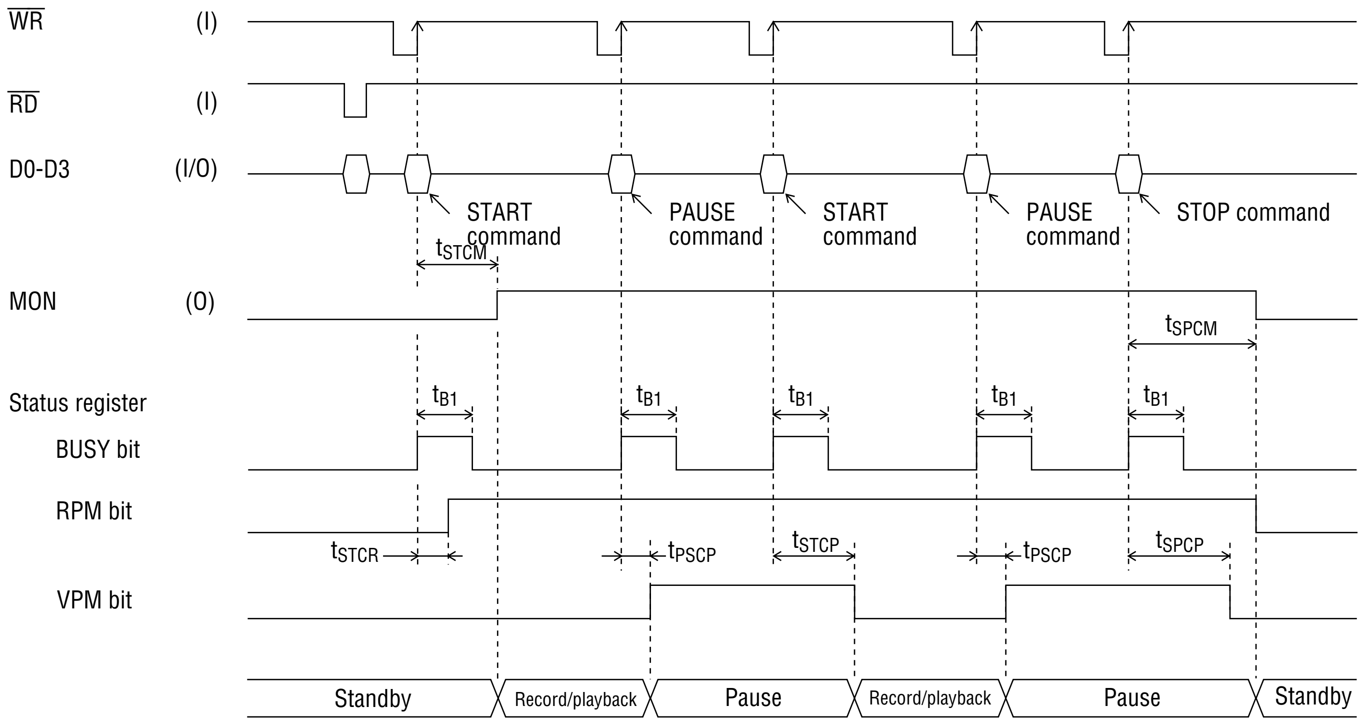

WR (I)
D0-D3 (I/O)
START command
(STOP command)
(STOP command)
tSPCV (Note)
tSPCM
MON (O)
Status register
tB1
tB1
tB1
BUSY bit
RPM bit
VPM bit
NAR bit
tSTCR
tAD1
tSPCR
Standby
Standby for voice
Address control
Recording
Address control
Standby
Voice detected
If the STOP command is input during standby for voice, this state is changed to the standby for recording.

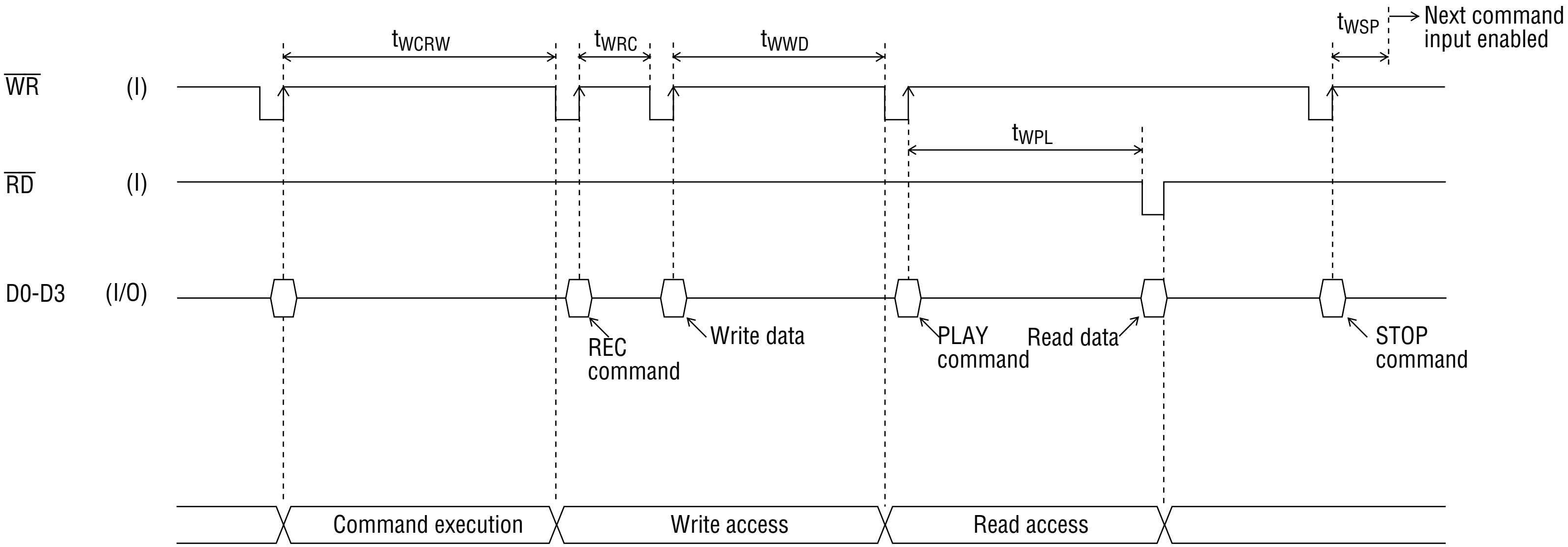
Note: t_{spcv} varies depending on the recording mode (flex recording or direct recording).

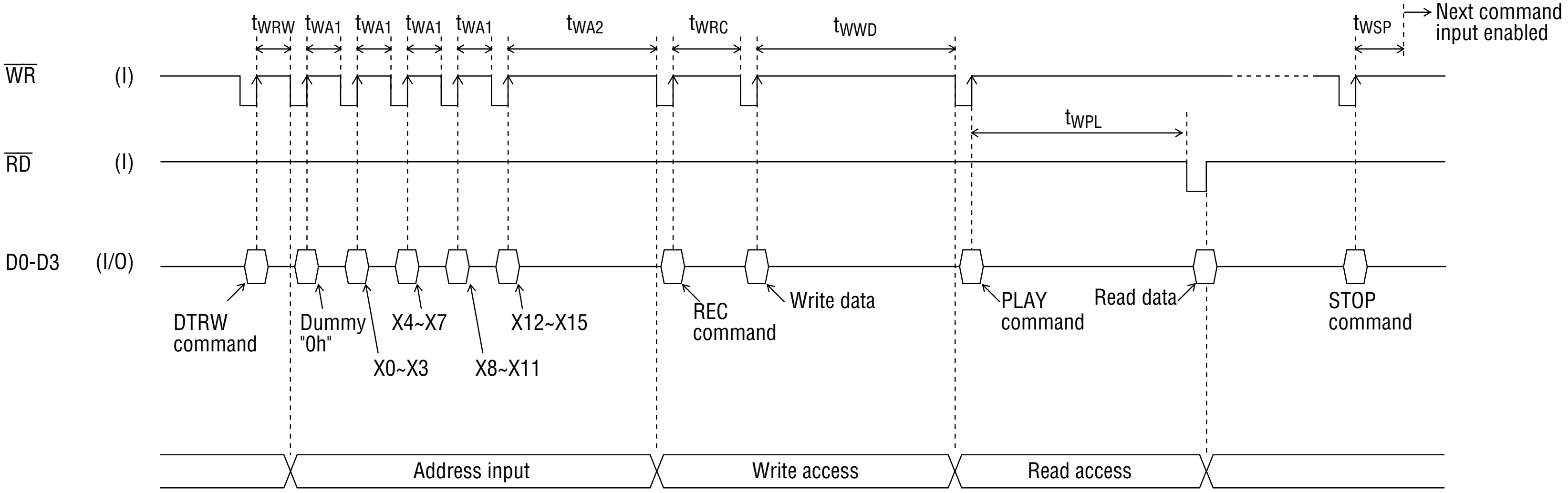
Timing for Continuous ROM Playback by Input of Address Code


WR (I)
D0-D3 (I/O)
CHAN command (1st phrase)
START command
CHAN command (2nd phrase)
START command
t_{STCM}
MON (0)
Status register
t_{STCR}
t_{STCN}
RPM bit
NAR bit
t_{AD1}
t_{MID}
AOUT (0)
Standby
Address control
1st phrase playback
Address control
2nd phrase playback
Standby

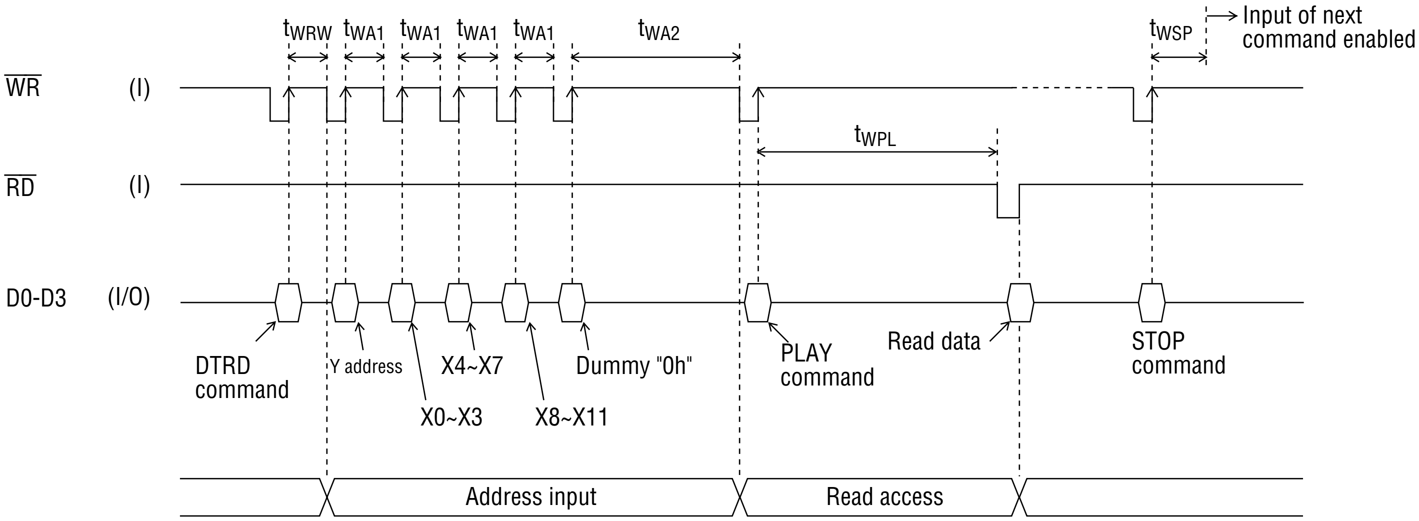
Timing for Record/Playback Pause Operation by PAUSE Command


WR (I)
RD (I)
D0-D3 (I/O)
START command
PAUSE command
START command
PAUSE command
STOP command
tSTCM
MON (O)
tSPCM
Status register
BUSY bit
tB1
RPM bit
tSTCR
tPSCP
tSTCP
tPSCP
tSPCP
VPM bit
Standby
Record/playback
Pause
Record/playback
Pause
Standby

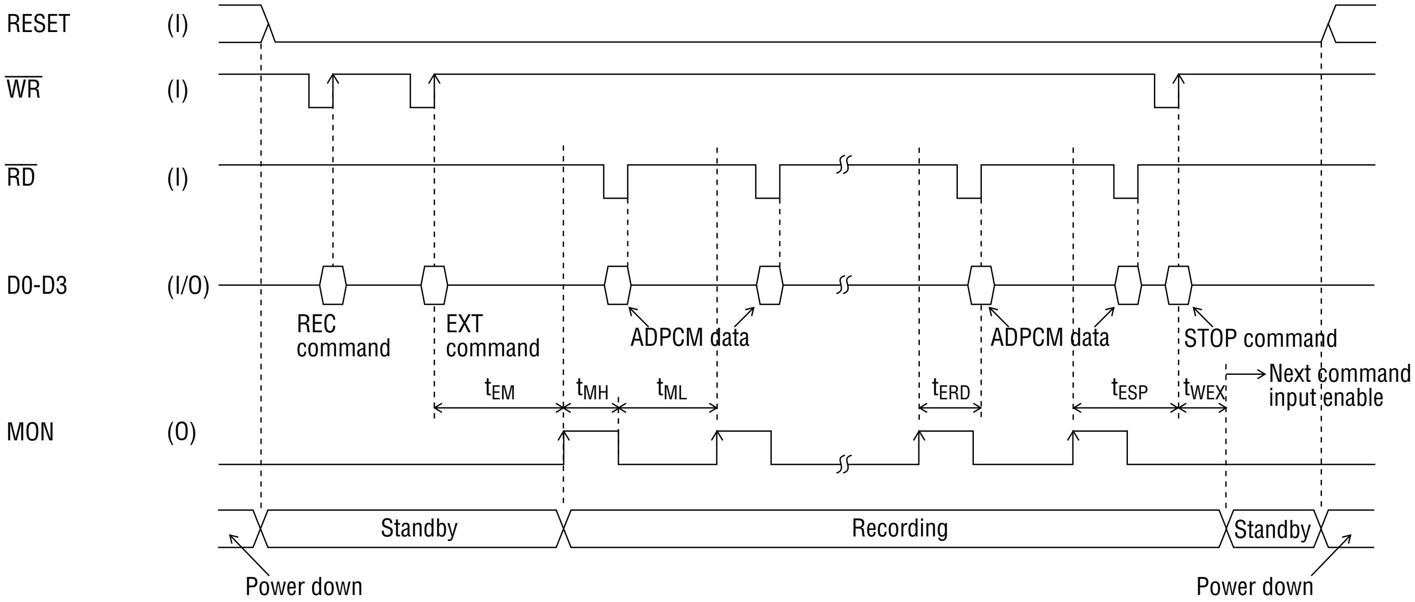

WR (I)
RD (I)
D0-D3 (I/O)
tWCRW
tWRC
tWWD
tWPL
tWSP
Next command input enabled
REC command
Write data
PLAY command
Read data
STOP command
Command execution
Write access
Read access


tWRW
tWA1
tWA1
tWA1
tWA1
tWA2
tWRC
tWWD
tWSP
Next command input enabled
WR (I)
tWPL
RD (I)
D0-D3 (I/O)
DTRW command
Dummy "0h"
X0~X3
X4~X7
X8~X11
X12~X15
REC command
Write data
PLAY command
Read data
STOP command
Address input
Write access
Read access

Timing for Data Read by DTRD command


t_{WRW}
t_{WA1}
t_{WA1}
t_{WA1}
t_{WA1}
t_{WA2}
t_{WSP}
Input of next command enabled
$\overline{WR}$ (I)
t_{WPL}
$\overline{RD}$ (I)
D0-D3 (I/O)
DTRD command
Y address
X0~X3
X4~X7
X8~X11
Dummy "0h"
PLAY command
Read data
STOP command
Address input
Read access

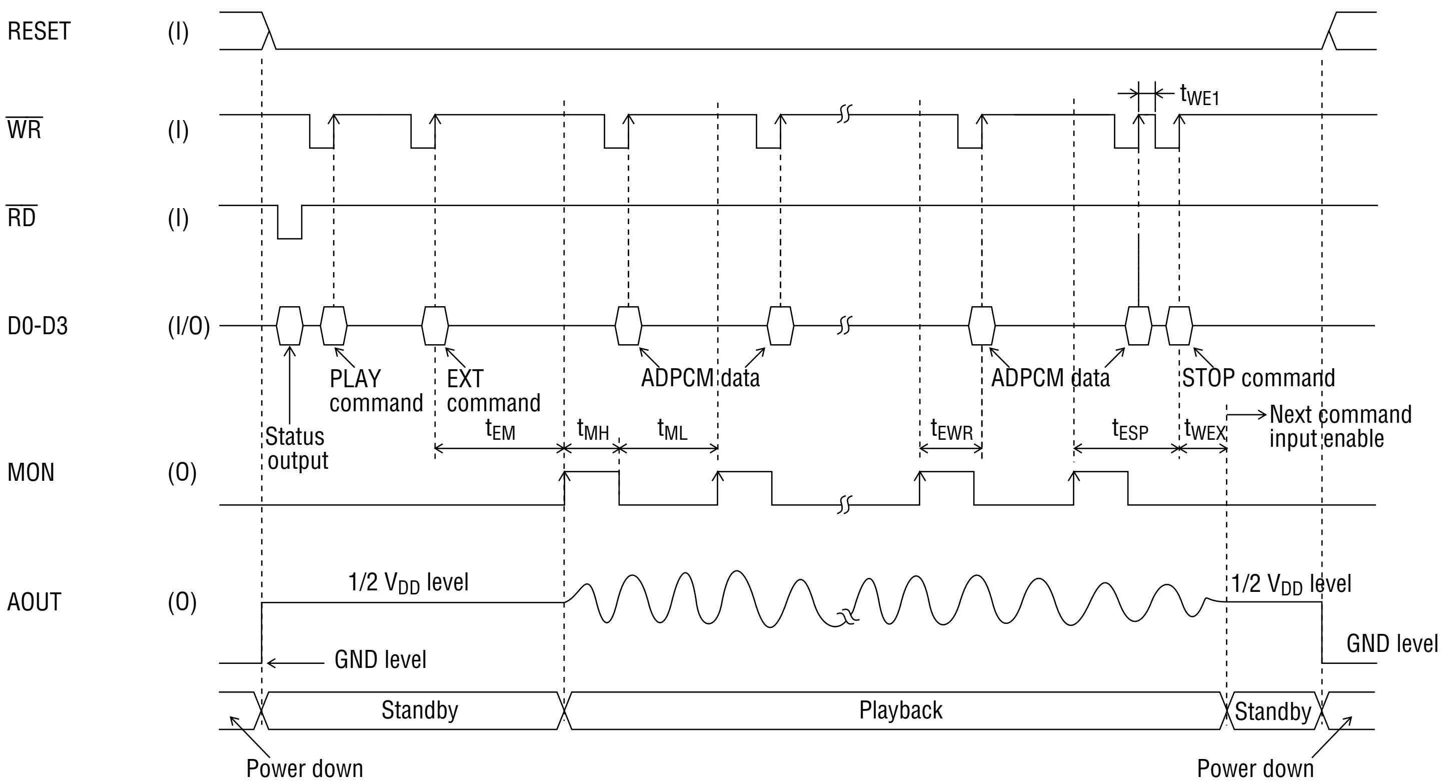
Recording by EXT Command


RESET (I)
WR (I)
RD (I)
D0-D3 (I/O)
MON (O)
REC command
EXT command
ADPCM data
ADPCM data
STOP command
Next command input enable
tEM
tMH
tML
tERD
tESP
tWEX
Standby
Recording
Standby
Power down
Power down

Notes: 1. When reading the ADPCM data, input the $\overline{RD}$ pulse to satisfy time t_{ERD} from rise of MON to rise of the rise of $\overline{RD}$ pulse.

2. Input the STOP command when the MON pin is "H", after reading the ADPCM data. At that time, it is required to satisfy time t_{ESP} from rise of MON to input of the STOP command.

Playback by EXT Command

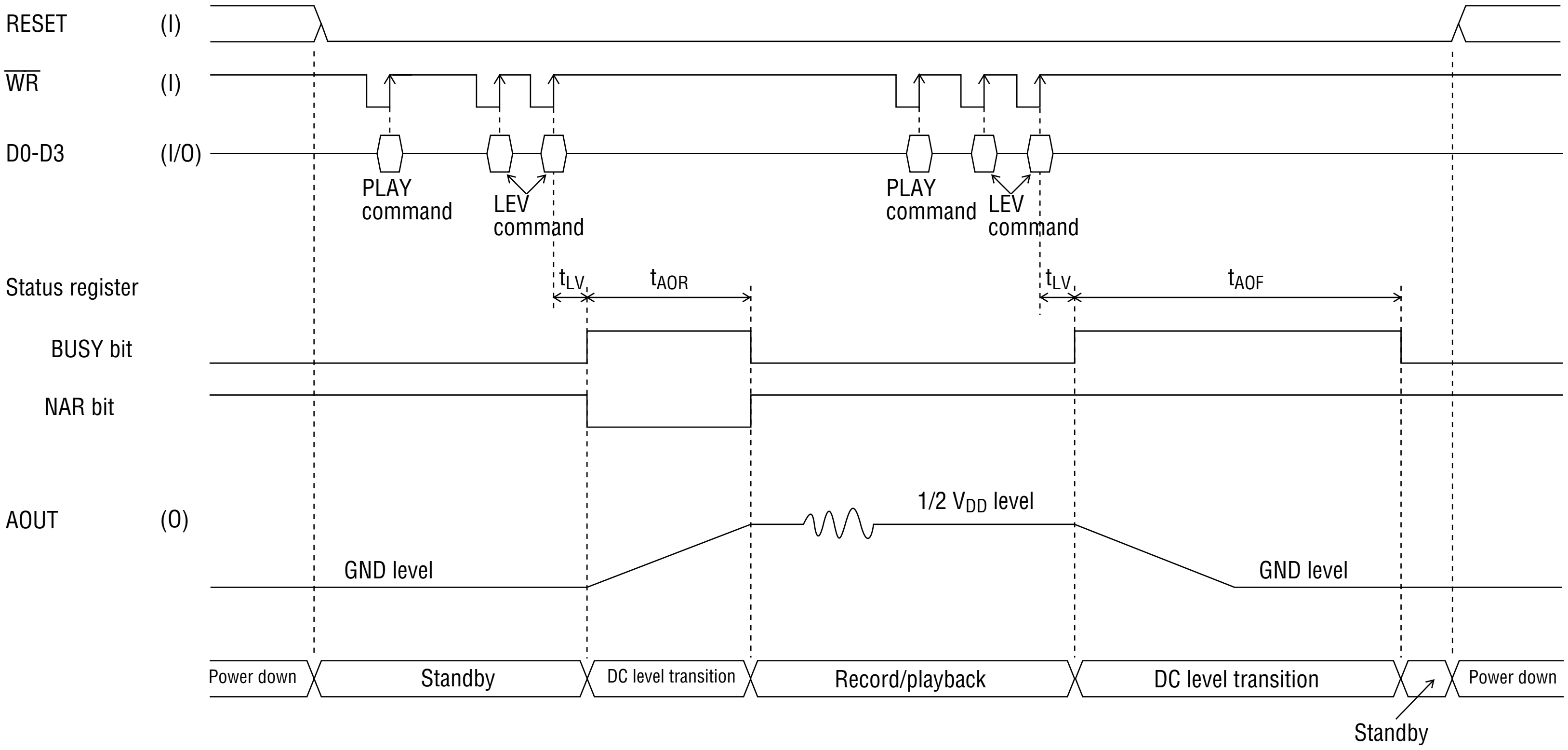

RESET (I)
$\overline{WR}$ (I)
$\overline{RD}$ (I)
D0-D3 (I/O)
MON (O)
AOUT (O)
t_{WE1}
Status output
PLAY command
EXT command
ADPCM data
ADPCM data
STOP command
t_{EM}
t_{MH}
t_{ML}
t_{EWR}
t_{ESP}
t_{WEX}
Next command input enable
1/2 V_{DD} level
1/2 V_{DD} level
GND level
GND level
Standby
Playback
Standby
Power down
Power down

Notes: 1. When writing the ADPCM data, input the $\overline{WR}$ pulse to satisfy time t_{EWR} from rise of MON to rise of the $\overline{WR}$ pulse.

2. Input the STOP command when the MON pin is "H", after writing the ADPCM data. At that time, it is required to satisfy time t_{ESP} from rise of MON to input of the STOP command, and interval t_{WE1} between the $\overline{WR}$ pulse and the STOP command pulse.

3. Input the ADPCM data beginning with the top of a phrase every sampling period sequentially. If the ADPCM data is input beginning with the second or following part of a phrase or with data missing, normal (playback) waveforms cannot be regenerated.

Timing for DC Level Transition by LEV Command


RESET (I)
WR (I)
D0-D3 (I/O)
PLAY command
LEV command
PLAY command
LEV command
Status register
t_{LV}
t_{AOR}
t_{LV}
t_{AOF}
BUSY bit
NAR bit
AOUT (O)
1/2 V_{DD} level
GND level
GND level
Power down
Standby
DC level transition
Record/playback
DC level transition
Power down
Standby

FUNCTIONAL DESCRIPTION

Recording Time and Memory Capacity

The recording time depends on the memory capacity of the external serial registers, sampling frequency, and ADPCM bit length, and is given by

$$\text{Recording time} = \frac{1.024 \times \text{memory capacity (K bits)}}{\text{sampling frequency (kHz)} \times \text{bit length (bits)}} \quad \text{(seconds)}$$

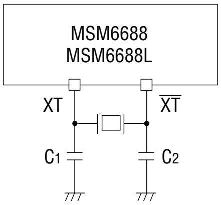
For example, if the sampling frequency is $\frac{4096}{768}$ kHz (= 5.333 kHz), ADPCM bit length is 3 bits, and four 8M bit serial registers are used, the recording time can be obtained as follows.

$$\text{Recording time} = \frac{1.024 \times (8192 \times 4 - 64)}{5.333 \times 3} = 2093 \text{ seconds}$$
$$= 34 \text{ minutes } 53 \text{ seconds}$$

In the above equation, the memory capacity is obtained by subtracting the memory capacity (64 Kbits) for the channel index area from the total memory capacity.

Connection of an Oscillator

Connect a ceramic oscillator or a crystal oscillator to XT and $\overline{\text{XT}}$ pins as shown below. The optimal load capacities when connecting ceramic oscillators from MURATA MFG., KYOCERA CORPORATION, and TDK CORPORATION are shown below for reference.



1. MSM6688

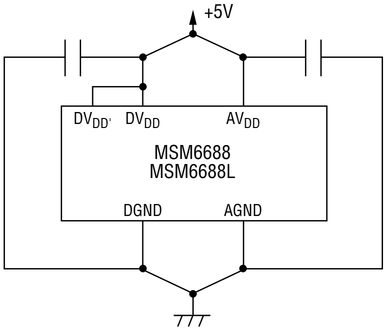
Ceramic oscillator				Optimal load capacity	
Type			Freq(MHz)	C1(pF)	C2(pF)
MURATA MFG.	CSA4.00MG		4.0	30	30
	CST4.00MGW	(with capacitor)			
	CSA6.00MG		6.0		
	CST6.00MGW	(with capacitor)			
	CSA8.00MTZ		8.0		
	CST8.00MTW	(with capacitor)			
KYOCERA CORPO-RATION	KBR-4.0MSA		4.0	33	33
	KBR-4.0MKS	(with capacitor)			
	PBRC4.00A				
	PBRC4.00B				
	KBR-6.0MSA		6.0		
	KBR-6.0MKS	(with capacitor)			
	PBRC6.00A				
	PBRC6.00B				
	KBR-8.0M		8.0		
	PBRC8.00A				
	PBRC8.00B				

2. MSM6688L

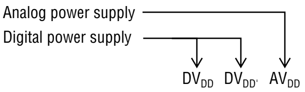
Ceramic oscillator				Optimal load capacity	
Type			Freq(MHz)	C_1(pF)	C_2(pF)
MURATA MFG.	CSA4.00MG		4.0	30	30
	CST4.00MGW	(with 30pF capacitor)		—	—
	CSTCS4.00MG0C5	(with 27pF capacitor)		—	—
	CSTCC4.00MG	(with 15pF capacitor)		—	—
	CSA6.00MG		6.0	30	30
	CST6.00MGW	(with 30pF capacitor)		—	—
	CSA8.00MTZ		8.0	30	30
	CST8.00MTW	(with 30pF capacitor)		—	—
KYOCERA CORPO-RATION	KBR-4.0MSB		4.0	33	33
	KBR-4.0MKC	(with capacitor)		—	—
	PBRC4.00A			33	33
	PBRC4.00B	(with capacitor)		—	—
	KBR-6.0MSB		6.0	33	33
	KBR-6.0MKC	(with capacitor)		—	—
	PBRC6.00A			33	33
	PBRC6.00B	(with capacitor)		—	—
	KBR-8.0M		8.0	33	33
	PBRC8.00A			33	33
	PBRC8.00B	(with capacitor)		—	—
TDK CORPO-RATION	FCR4.0M5		4.0	33	33
	FCR4.0MC5	(with 30 pF capacitor)		—	—
	FCR6.0M5		6.0	33	33
	FCR6.0MC5	(with 30 pF capacitor)		—	—
	CCR6.0MC3	(with capacitor)		—	—
	FCR8.0M2S		8.0	33	33
	CCR8.0MC5	(with capacitor)		—	—

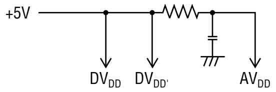
Power Supply Wiring

As shown in the following diagram, supply the power to this MSM6688 from the same power source, but separate the power supply wiring to the analog portion from that to the logic position.


+5V
DVDD'
DVDD
AVDD
MSM6688
MSM6688L
DGND
AGND

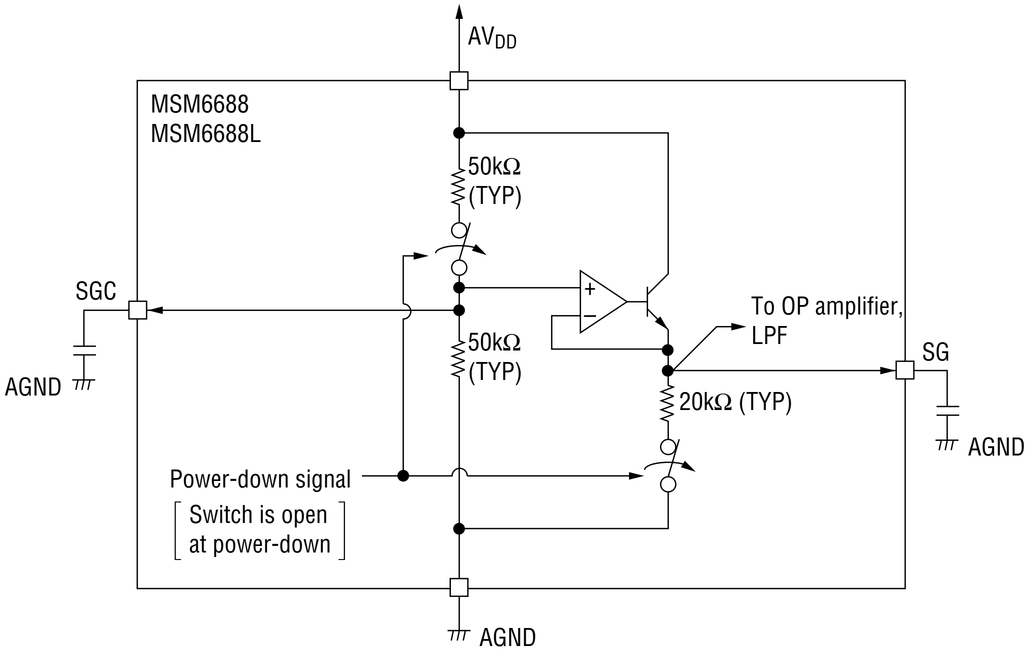
The following connections are not permitted.


Analog power supply
Digital power supply
DVDD
DVDD'
AVDD


+5V
DVDD
DVDD'
AVDD

Configuring SGC and SG pins

The internal equivalent circuit around the SGC and SG pins is shown below.


AVDD
MSM6688
MSM6688L
50kΩ (TYP)
SGC
AGND
+
−
To OP amplifier, LPF
SG
50kΩ (TYP)
20kΩ (TYP)
AGND
Power-down signal
Switch is open at power-down
AGND

The SG signal is a reference voltage (signal ground) for internal OP amplifiers and LPF. Install a capacitor between the SGC pin and AGND and between the SG pin and AGND respectively in order to make the SG signal noiseless. It is recommended to use an approx. 0.1 µF capacitor, which should be determined after evaluating the tone quality.

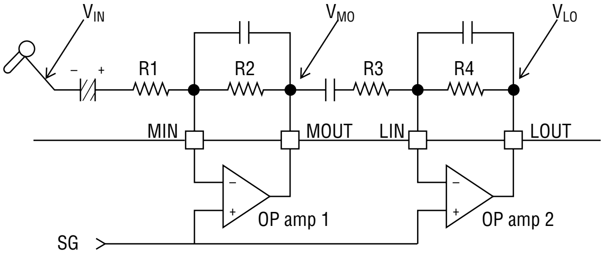
It takes several ten msec until the DC levels such as the SG level of the analog circuit is stabilized after the power-down mode is cancelled. The larger capacitance of a capacitor connected to SGC or SG requires the longer time for stabilizing.
After the power-down mode is cancelled, enter voices after the DC levels for the analog circuit has been stabilized.

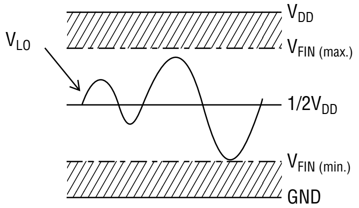
When the device is in power-down mode, the output voltage of the SG pin becomes unstable. Therefore, SG must not be supplied to external circuits.
Otherwise, power supply current may be leaked via the internal SG circuit.
Same is true for the SGC pin.

Analog Input Amplifier Circuit

This MSM6688 has two built-in operational amplifiers for amplifying the microphone output. Each OP amplifier is provided with the inverting input pin and output pin. The analog circuit reference voltage SG (signal ground) is connected internally to the non-inverting input of each OP amplifier.

For amplification, form an inverting amplifier circuit and adjust the amplification factor by using external resistors as shown below.





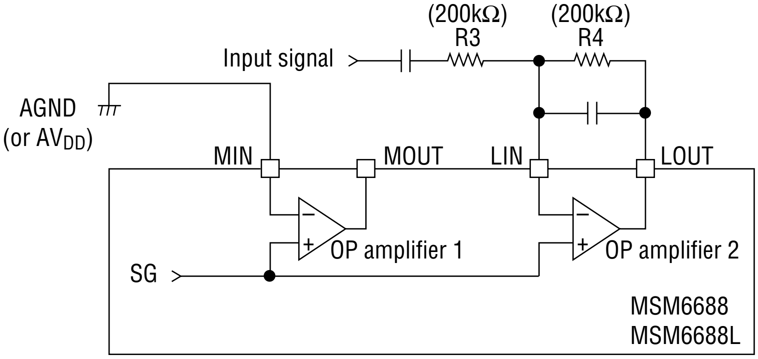
$$V_{LO} = \frac{R4}{R3} \quad V_{MO} = \frac{R2 \bullet R4}{R1 \bullet R3} V_{IN} \quad (V)$$

During recording, the output V_{LO} of OP amp 2 is connected to the input FIN of the LPF. Adjust the amplification factor by using the external resistors so that the V_{LO} amplitude is within the FIN admissible input voltage (V_{FIN}) range.
If V_{LO} exceeds the V_{FIN} range, the LPF output waveform will be distorted.
The table below shows an example of the allowable FIN input voltage range for the MSM6688 and MSM6688L.

Parameter	Power Supply Voltage V_{DD}	Allowable FIN input Voltage range V_{FIN}		Allowable FIN input Voltage
		min.	max.	
MSM6688	5 V	1 V	4 V	3 Vp-p
MSM6688L	3 V	0.75 V	2.25 V	1.5 Vp-p

The value of the OP amplifier load resistance R_{OUTA} is 200kΩ minimum. Therefore the values of the inverting amplifier circuit feedback resistors R2 and R4 should be 200kΩ or more.

When OP amplifier 1 is not used and OP amplifier 2 is used, the MIN pin must be connected to AGND or AV_{DD}, and the MOUT pin must be open.
Even if amplification is unnecessary, OP amplifier 2 must be always used.
Below is an example of an analog input amplifier circuit when the amplification factor is 1.


(200kΩ)
R3
(200kΩ)
R4
Input signal
AGND
(or AV_{DD})
MIN
MOUT
LIN
LOUT
OP amplifier 1
OP amplifier 2
SG
MSM6688
MSM6688L

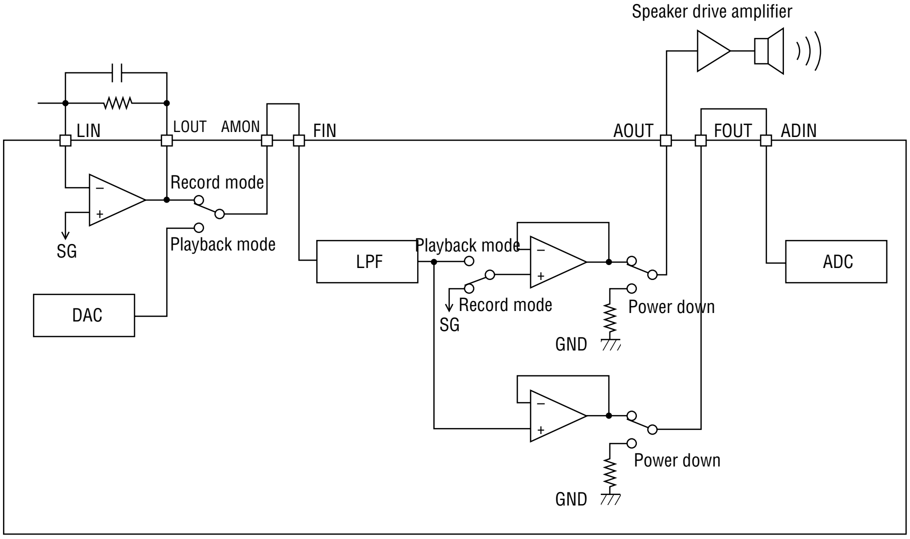
Connection of LPF Circuit Peripherals

The AMON pin is connected internally to the output of the amplifier circuit (LOUT pin) in the recording mode and to the output of the built-in DA converter in the playback mode. Therefore, connect the AMON pin directly to the input (FIN pin) of the built-in LPF.

Both the FOUT and AOUT pins are the output pins of the built-in LPF. Connect the FOUT pin to the input (ADIN pin) of the built-in AD converter and connect the AOUT pin to an external speaker through an external speaker drive amplifier.

In the MSM6688/6688L, the connection of each of the FOUT and AOUT pins is changed to one of the output of the LPF, GND (ground) level, and SG (signal ground) level, depending on the operation status as shown below.

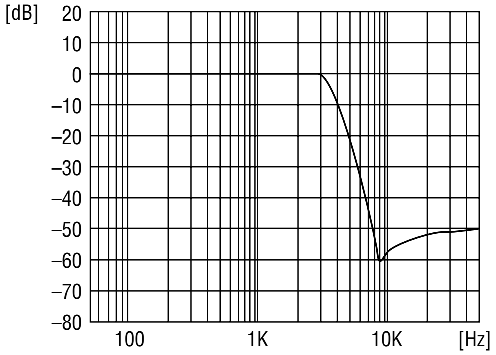
Analog pin	At power down (RESET pin = H)	During operation (RESET pin = L)	
		Recording mode	Playback mode
FOUT pin	GND level	LPF output (recording waveform)	LPF output
AOUT pin	GND level	SG level	LPF output (playback waveform)



Note: This diagram shows the state of each switch during the recording operation.

LPF Characteristics

This MSM6688/6688L contains a fourth-order switched-capacitor LPF.
The attenuation characteristic of this LPF is –40 dB/oct. The cut-off frequency and frequency characteristics of this LPF vary in proportion to the sampling frequency (fsamp). The cut-off frequency is preset to 0.4 times the sampling frequency. The following graph depicts the frequency characteristics of the LPF at fsamp = 8 kHz.

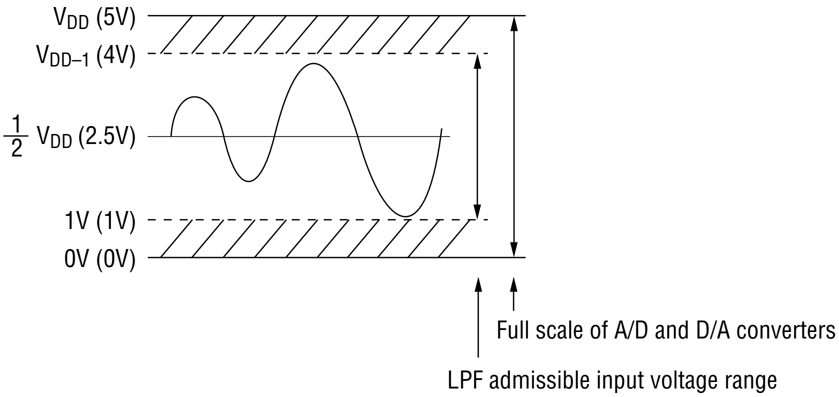


LPF Frequency Characteristics (fsamp = 8.0 kHz)

Full Scale of A/D and D/A Converters

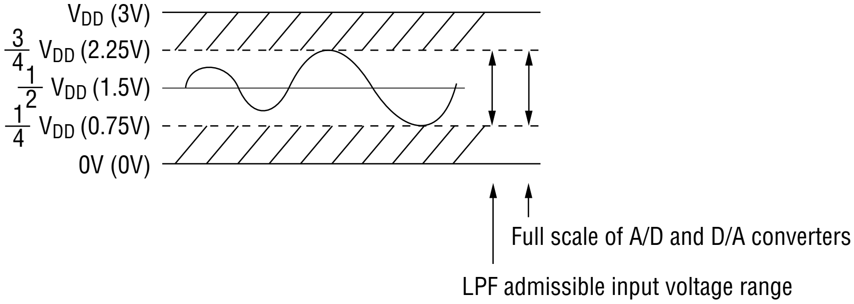
Parameter	Full scale of A/D and D/A converters		
	min. (V)	max. (v)	amplitude (Vp-p)
MSM6688	0	V_{DD}	V_{DD}
MSM6688L	$1/4 \times V_{DD}$	$3/4 \times V_{DD}$	$1/2 \times V_{DD}$

1. When the MSM6688 is used


V_{DD} (5V)
V_{DD-1} (4V)
$\frac{1}{2}$ V_{DD} (2.5V)
1V (1V)
0V (0V)
Full scale of A/D and D/A converters
LPF admissible input voltage range

Note: Value in parentheses applies when V_{DD}=5.0V.

2. When the MSM6688L is used


V_{DD} (3V)
$\frac{3}{4}$ V_{DD} (2.25V)
$\frac{1}{2}$ V_{DD} (1.5V)
$\frac{1}{4}$ V_{DD} (0.75V)
0V (0V)
Full scale of A/D and D/A converters
LPF admissible input voltage range

Note: Value in parentheses applies when V_{DD}=3.0 V.

Reset Function

By applying a high level to the RESET pin, the MSM6688/6688L stops oscillation to minimize current consumption and goes to the power-down state. At the same time, the control circuit is reset and initialized.

When this reset operation is performed, the record/playback condition, such as sampling frequency and ADPCM bit length, and the data stored in the serial registers are set to the data stored just before the reset takes place. In this case, the playback level is set to 0 dB amplitude.

If a high level is applied to the RESET pin during command execution or record/playback operation, the MSM6688/6688L is set to the power-down state and initialized state. Internal data voice data becomes undefined.

The following shows the power-down state of the MSM6688/6688L.

(1) Oscillation is stopped and all operations of the internal circuit are halted.

(2) The current consumption is minimized. When an external clock is used, apply a ground (GND) level to the XT pin at power down so that no current can flow into the oscillation circuit.

(3) D0–D3 pins constituting the data bus go to the high-impedance state, independent of the state of the $\overline{\text{RD}}$, $\overline{\text{CE}}$, and CE pins.

(4) $\overline{\text{CS1}}$ – $\overline{\text{CS4}}$ pins are set to a high level to minimize the current consumption of external serial registers and serial voice ROMs.

(5) The state of the output pins and input/output pins are as follows.

Pin name	Power down mode with RESET="H"	Power down mode with $\overline{\text{PDWN}}$="L"
$\overline{\text{SAS}}$, $\overline{\text{TAS}}$, $\overline{\text{CS1}}$-$\overline{\text{CS4}}$, $\overline{\text{RWCK}}$	"H" level	"H" level
SADX, $\overline{\text{WE}}$, NAR	"H" level	"H" level or "L" level
SADY	"L" level	"H" level or "L" level
MON	"L" level	"L" level
D0-D3, BUSY, RPM, VPM	Hi-Z	Hi-Z
DI/O	Hi-Z	"H" "L" or Hi-Z
AOUT, FOUT	GND level	GND level

After powering up the MSM6688/6688L, be sure to initialize it by applying a high level to the RESET pin.

Power Down by the $\overline{\text{PDWN}}$ pin

By applying a low level to the $\overline{\text{PDWN}}$ pin, the MSM6688/6688L is set to the power-down state, in which the frequency oscillation and all operations of internal circuits are halted. Unlike the reset operation by the RESET input, the control circuit will not be initialized by this power-down operation.

The power-down operation will not affect the data in the internal control circuit and external serial registers. Therefore, this power-down operation is useful when the battery backup takes place in case of power failure.

When $\overline{\text{PDWN}}$ goes to a low level during command execution, this execution of command is halted at the time that power-down operation is performed. When $\overline{\text{PDWN}}$ becomes low during one of the following operations, their respective operations will be performed after the power-down state is released ($\overline{\text{PDWN}}$ = H).

(1) When the MSM6688/6688L is powered down ($\overline{\text{PDWN}}$ = L) during the record/playback operation: The record/playback operation is stopped. After the release of the power-down state, the postprocessing will be performed. The end of the postprocessing can be verified by checking the BUSY bit and RPM bit of the status register.

(2) When the MSM6688/6688L is powered down ($\overline{\text{PDWN}}$ = L) during the phrase deleting operation: The phrase deleting operation is temporarily stopped and will be restarted after the release of the power-down state. The end of the phrase deleting operation can be verified by checking the BUSY bit.

(3) When the MSM6688/6688L is powered down ($\overline{\text{PDWN}}$ = L) during the time the transition of the AOUT output to a DC level by LEV command is in progress: This transition operation is temporarily stopped and will be continued after the release of the power-down state. The end of the transition to a DC level can be verified by checking the BUSY bit.

Record/Playback Control Modes

There are four types of record/playback mode: flex record/playback, ROM playback by inputting address codes, direct record/playback, and direct ROM playback modes. A desired record/playback control mode can be selected by the command mode set in the SAMP command.

Record/ playback control mode	**Flex record/playback**	**ROM playback by input of address code**	**Direct record/playback**	**Direct ROM playback**
Command mode	Mode 0	Mode 1	Mode 2	Mode 3
Number of phrases	63	255	64 (expandable)	As required
Addressing	Indirect addressing by phrase designation	Indirect addressing by phrase designation	Direct addressing by ADRWR command	Direct addressing by ADRWR command
Setting of recording time	Setting by BLKWR command	—	Setting by ADRWR command	—

1. Flex record/playback

The recording area for each phrase is indirectly specified by phrase designation (CA0–CA5, 63 phrases). The recording area for each phrase is controlled by the MSM6688/6688L, so that the address control load of the microcontroller can be reduced.

The recording time is specified by the BLKWR command. During recording operation, the MSM6688/6688L searches the memory areas that are not used by other phrases and writes the voice data on them. Therefore, the phrase control by the microcontroller can be performed easily even in applications in which it is required to perform phrase deletion and re-recording frequently.

2. ROM playback by input of address codes

The playback area of each phrase of the fixed message is indirectly specified by phrase designation (CA0–CA7, 255 phrases).
The table containing the start address and stop address that indicate the playback area, sampling frequency and ADPCM bit length, is written in the index area of the serial voice ROM.

3. Direct record/playback

The recording area for each phrases is specified directly by inputting the address set in the ADRWR command from the microcontroller after a desired phrase has been specified by phrase designation (CA0–CA5, 64 phrases). This means that the address control such as the allocation of memory capacity (recording time) for each phrases is performed by the microcontroller.

This direct record/playback mode is suitable for the case where the number of phrases and the recording time allocated to each phase are fixed. If the table containing the start address and stop address of each phrase is stored in the microcontroller or an external circuit, it becomes possible to perform record/playback of 65 or more phrases.

4. Direct ROM playback

The playback area of each phrase for a fixed message is specified directly by inputting the address set in the ADRWR command from the microcontroller. In this case, it is required to store the table containing the start and stop addresses of each phrase, sampling frequency and ADPCM bit length in the microcontroller and the external ROM.
If a serial voice ROM products for the MSM6388/MSM6588/6588L ADPCM solid state recorders are used for the MSM6688/6688L, this direct ROM playback mode is applied.

Data Configuration of External Serial Registers

The external RAM constitutes a virtual memory with a address space of (X addresses in the word direction) × (depth of 1kbits) through the DRAM interface (MSM6791).
This virtual memory is addressable only for X addresses in the word direction.
The external RAM is divided into the channel index area that stores the data for address control of each phrase and the voice (ADPCM) data area.
The address space and channel index area in the flex record/playback mode are different from those in the direct record/playback mode.

1. Address space allocation of external serial registers

1.1 Address space for the flex record/playback mode

In the flex record/playback mode, the total memory capacity of external serial registers is equally divided into 256 blocks that are addressable by 00h–FFh.

Each block is composed of multiple words each having the depth of 1K bits. X addresses in the word direction are offset addresses in the blocks. The memory capacity of one block and the maximum address of X addresses vary depending on the total memory capacity of serial registers externally connected.

RSEL2		L	L	H	H
RSEL1		L	H	L	H
Total memory capacity (Number. of serial registers)		8M bits (1)	16M bits (2)	24M bits (3)	32M bits (4)
Memory capacity of one block		32K bits	64K bits	128K bits	128K bits
Recording time of one block	16kbps	2.0 seconds	4.1 seconds	8.2 seconds	8.2 seconds
	24kbps	1.4 seconds	2.7 seconds	5.5 seconds	5.5 seconds
	32kbps	1.0 second	2.0 seconds	4.1 seconds	4.1 seconds
Number of words of one block [Offset address]		32 words [00h - 1Fh]	64 words [00h - 3Fh]	128 words [00h - 7Fh]	128 words [00h - 7Fh]
Number of initially available blocks		254 (FEh)	255 (FFh)	191 (BFh)	255 (FFh)

The storing method of 1K-bit ADPCM data in the Y direction varies depending on the ADPCM bit length (3-bit ADPCM or 4-bit ADPCM).

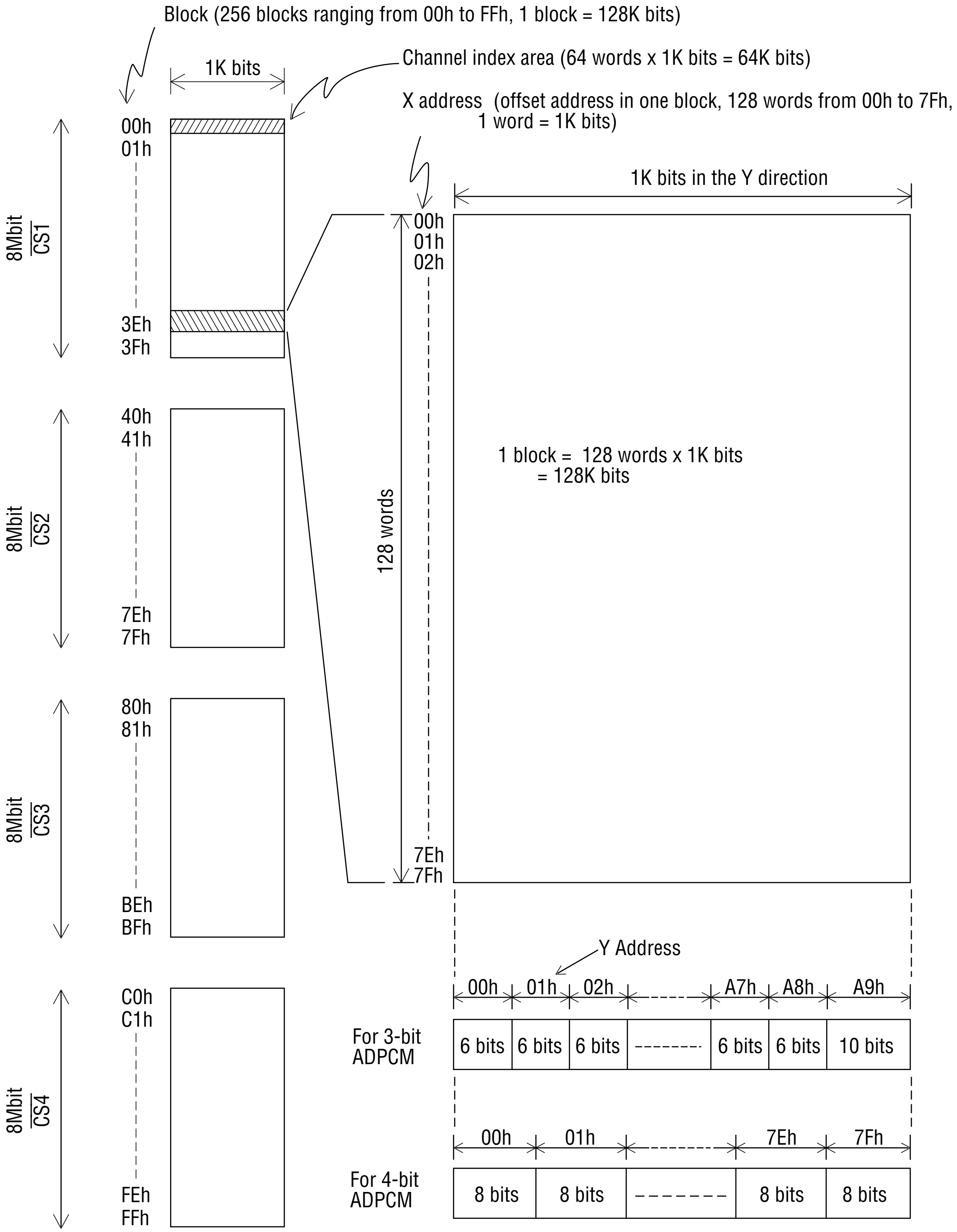
(1) For 3-bit ADPCM, (3 bits × 340 samples + unused 4 bits = 1024 bits) are stored in the 1K-bit memory area.

One Y address is allocated to two ADPCM data samples, so that Y addresses are addressable by 00–A9h

(2) For 4-bit ADPCM, (4 bits × 256 samples = 1024 bits) are stored in the 1K-bit memory area.

One Y address is allocated to two ADPCM data samples, so that Y addresses are addressable by 00–7Fh

Address Space Allocation of RAM
(Flex record/playback, 32M-bit)


Block (256 blocks ranging from 00h to FFh, 1 block = 128K bits)
Channel index area (64 words x 1K bits = 64K bits)
X address (offset address in one block, 128 words from 00h to 7Fh, 1 word = 1K bits)
1K bits
1K bits in the Y direction
8Mbit
CS1
00h
01h
3Eh
3Fh
8Mbit
CS2
40h
41h
7Eh
7Fh
8Mbit
CS3
80h
81h
BEh
BFh
8Mbit
CS4
C0h
C1h
FEh
FFh
128 words
00h
01h
02h
7Eh
7Fh
1 block = 128 words x 1K bits
= 128K bits
Y Address
00h
01h
02h
A7h
A8h
A9h
For 3-bit ADPCM
6 bits
6 bits
6 bits
6 bits
6 bits
10 bits
00h
01h
7Eh
7Fh
For 4-bit ADPCM
8 bits
8 bits
8 bits
8 bits

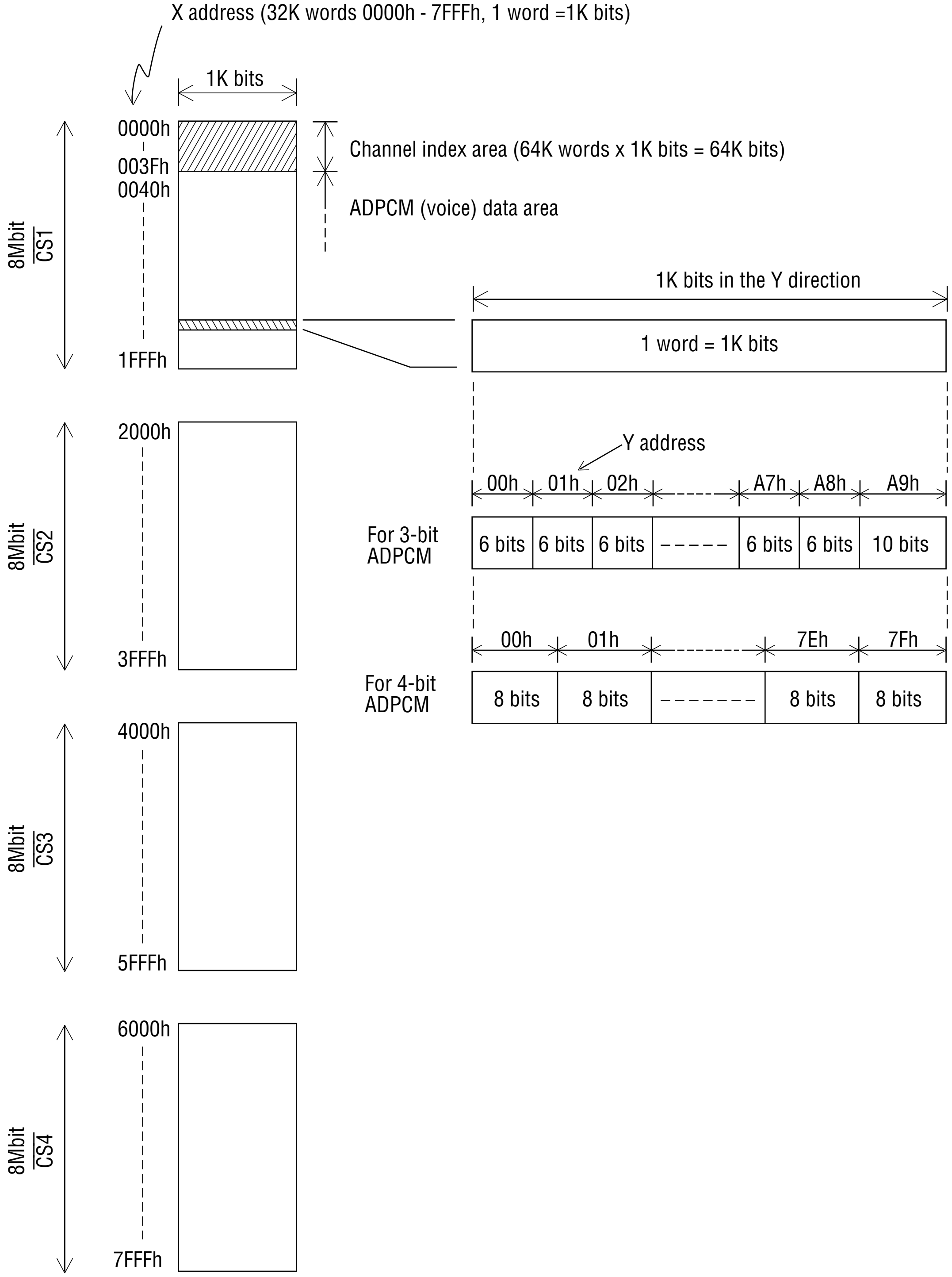
1.2 Address space allocation in the direct record/playback mode

In the direct record/playback mode, address control is performed by (X addresses in the word direction) x (1K bit depth in the Y direction). The maximum address of X addresses in the word direction varies depending on the total memory capacity of RAM externally connected. The header 64 words (64K bits) of the RAM are used as the channel index area. Therefore, addresses after X address 0040h can be used as the voice data area.

RSEL2	L	L	L	H	H
RSEL1	L	L	H	L	H
Total memory capacity	4M bits	8M bits	16M bits	24M bits	32M bits
No. of words	4K words	8K words	16K words	24K words	32K words
X address	0000h - 0FFFh	0000h - 1FFFh	0000h - 3FFFh	0000h - 5FFFh	0000h - 7FFFh

The storage method of 1K-bit ADPCM data in the Y direction is identical to that for the flex record/ playback mode. For 3-bit ADPCM data, the storage locations are addressable by 00h–A9h, For 4-bit ADPCM data, the storage locations are addressable by 00h–7Fh.

Address Space Allocation of RAM
(Direct record/playback)


X address (32K words 0000h - 7FFFh, 1 word =1K bits)
1K bits
0000h
003Fh
0040h
1FFFh
Channel index area (64K words x 1K bits = 64K bits)
ADPCM (voice) data area
8Mbit
$\overline{CS1}$
1K bits in the Y direction
1 word = 1K bits
2000h
3FFFh
8Mbit
$\overline{CS2}$
Y address
00h
01h
02h
A7h
A8h
A9h
For 3-bit ADPCM
6 bits
6 bits
6 bits
6 bits
6 bits
10 bits
00h
01h
7Eh
7Fh
For 4-bit ADPCM
8 bits
8 bits
8 bits
8 bits
4000h
5FFFh
8Mbit
$\overline{CS3}$
6000h
7FFFh
8Mbit
$\overline{CS4}$

2. Channel index area of serial registers

2.1 Channel index area in the flex record/playback mode

In the flex record/playback mode, the channel index area for one phrase (1K bits) consists of 64K-bit address data, 704-bit user data, and 256-bit address control block table. The address data consists of the number of blocks, stop Y address, stop X address, start block, stop block, and PRED block. In the following, these areas are summarized.

(1) Number of blocks: This area stores the number of blocks (recorded time) used for recording of one phrase. Address ch00 stores the number of unused blocks (available blocks). This number of blocks can be read by the BLKRD command. The recorded time for one phase and the unused capacity (available recording time) of memory can be obtained.

(2) Stop Y address: This area stores the stop Y address of the phrase. A Y address location is addressable by one of 00h–A9h for 3-bit ADPCM, and by one of 00h–7Fh for 4-bit ADPCM.

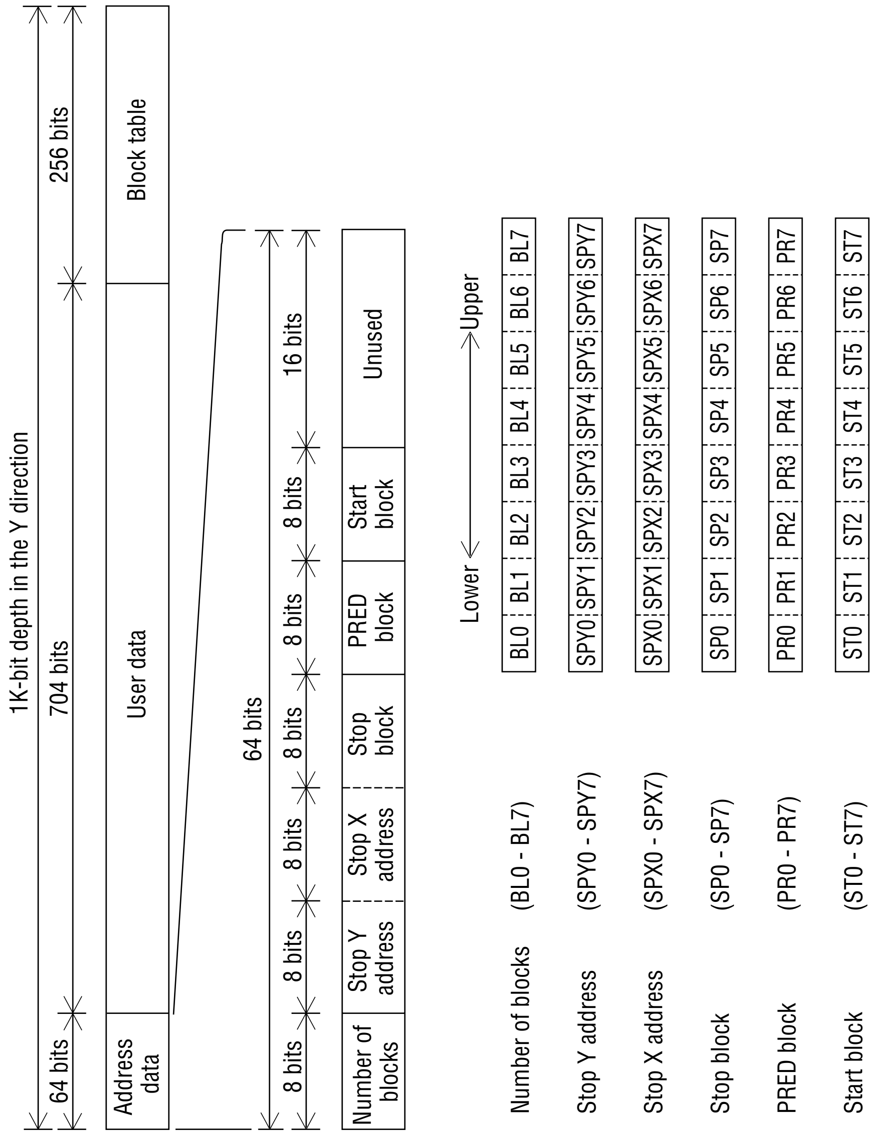
(3) Stop X address: This area stores the stop X address of a phrase. This X address is offset address of the block. One X address has a 1K-bit memory area. The memory capacity of one block varies depending on the number of serial registers connected externally, and addressing also varies accordingly.

(4) Start block and stop block: The total memory capacity of serial registers is equally divided into 256 blocks. Addresses 00h–FFh are assigned to these blocks. The start block and stop block are stored in the start block area and stop block area, respectively.

(5) PRED block: This area stores the address of a block immediately before the stop block. In the flex record/playback mode, each recording area is controlled on a per-block basis. Therefore, a phrase is not always stored continuously in serial registers. For example, if a phrase is recorded in three blocks 03h, 04h and 07h. The PRED block stores 04h. This PRED block is used to change the stop block and stop X address for deleting a tail part of the recorded phrase.

(6) User data: This user data area can be used by the user. The data can be written to and read from this area by the CHRW command.
This user data area is provided independently for each phrase, so that it is useful to store the sampling frequency, ADPCM bit length and recorded time.

(7) Block table: The block table is an area used for the block control.

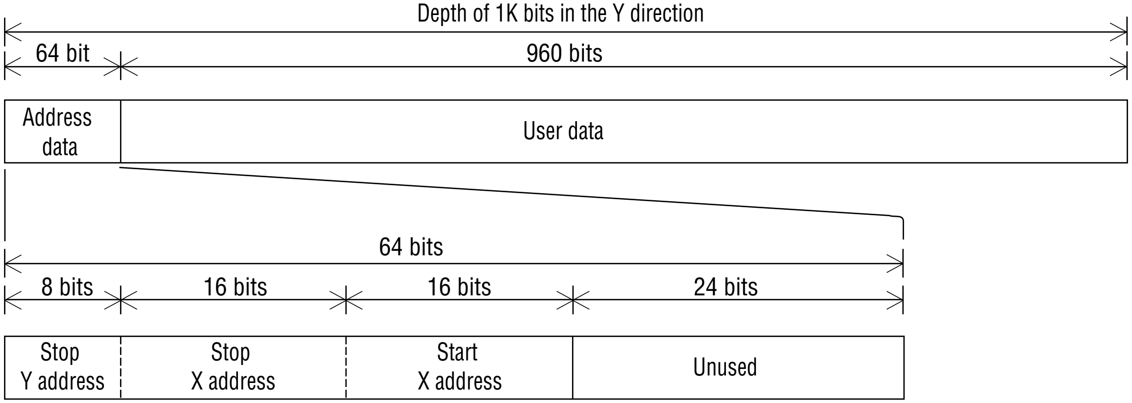

1K-bit depth in the Y direction
256 bits
704 bits
64 bits
Block table
User data
Address data
64 bits
16 bits
8 bits
8 bits
8 bits
8 bits
8 bits
8 bits
Unused
Start block
PRED block
Stop block
Stop X address
Stop Y address
Number of blocks
Lower
Upper
BL0 BL1 BL2 BL3 BL4 BL5 BL6 BL7
SPY0 SPY1 SPY2 SPY3 SPY4 SPY5 SPY6 SPY7
SPX0 SPX1 SPX2 SPX3 SPX4 SPX5 SPX6 SPX7
SP0 SP1 SP2 SP3 SP4 SP5 SP6 SP7
PR0 PR1 PR2 PR3 PR4 PR5 PR6 PR7
ST0 ST1 ST2 ST3 ST4 ST5 ST6 ST7
Number of blocks (BL0 - BL7)
Stop Y address (SPY0 - SPY7)
Stop X address (SPX0 - SPX7)
Stop block (SP0 - SP7)
PRED block (PR0 - PR7)
Start block (ST0 - ST7)

2.2 Channel index area in the direct record/playback mode

In the direct record/playback mode, the channel index area for one phrase (1K bits) consists of 64-bit address data and 960-bit user data. The address data consists of the stop Y address, stop X address, start X address, and unused area.

(1) Stop Y address: In the same manner as in the direct record/playback mode, the stop address can be specified by one of 00h–A9h for 3-bit ADPCM and 00h–7Fh for 4-bit ADPCM.
(2) Start X address and stop X address: An X address is specified by 16 bits (15 effective bits). The 32K-word X address space can be addressed by 000h–7FFFh.

(3) User data: In the same manner as in the direct record/playback mode, this user data area can be used by the user. The data can be written to and read from this area by the CHRW command.


Depth of 1K bits in the Y direction
64 bit
960 bits
Address data
User data
64 bits
8 bits
16 bits
16 bits
24 bits
Stop Y address
Stop X address
Start X address
Unused

Lower ⟷ Upper

Stop Y address	(SPY0 - SPY7)	SPY0	SPY1	SPY2	SPY3	SPY4	SPY5	SPY6	SPY7								
Stop X address	(SPX0 - SPX15)	SPX0	SPX1	SPX2	SPX3	SPX4	SPX5	SPX6	SPX7	SPX8	SPX9	SPX10	SPX11	SPX12	SPX13	SPX14	SPX15
Start X address	(STX0 - STX15)	STX0	STX1	STX2	STX3	STX4	STX5	STX6	STX7	STX8	STX9	STaX10	STX11	STX12	STX13	STX14	STX15

Data Configuration of External Serial Voice ROMs

The external serial voice ROMs are composed of (X addresses in the word direction) × (depth of 1K bits). The addressing is possible only for X addresses in the word direction. The maximum address of the X addresses in the word direction varies depending on the total memory capacity of the serial voice ROMs externally connected. In the ROM playback by input of address code, the header 16 words (16K bits) are used as the channel index area, so that the addresses after address 010h can be used as the voice data area.

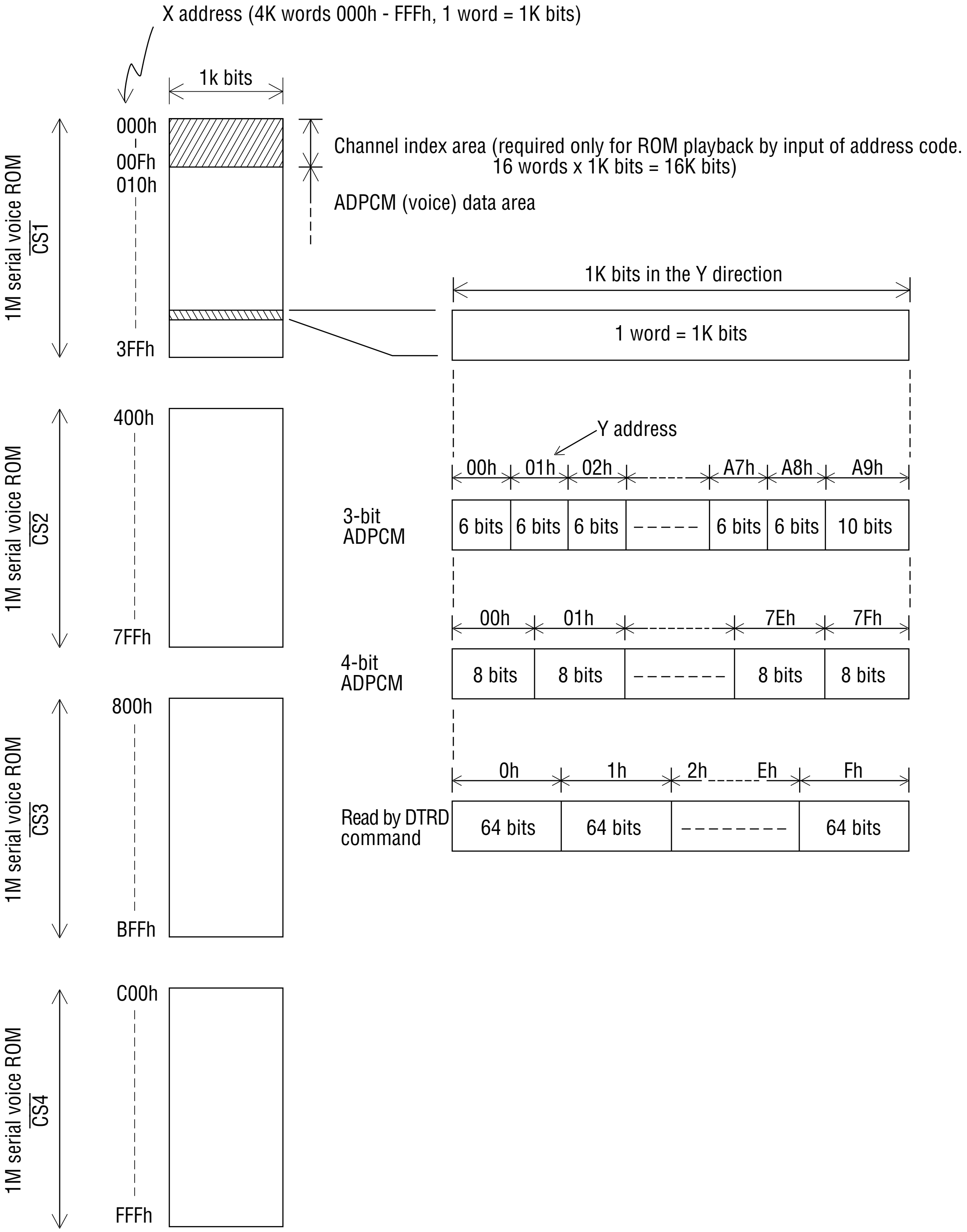
Total memory capacity (Number of ROMs)		**1M bits (1)**	**2M bits (2)**	**3M bits (3)**	**4M bits (4)**
ROM playback by input of address code	Number of words	1008 words	2032 words	3056 words	4080 words
	X address	010h - 3FFh	010h - 7FFh	010h - BFFh	010h - FFFh
Direct ROM playback DTRD command	Number of words	1024 words	2048 words	3072 words	4096 words
	X address	000h - 3FFh	000h - 7FFh	000h - BFFh	000h - FFFh

The method for storing the ADPCM data of 1K bits in the Y direction is identical to that for the record/ playback mode.

Addressing can be made by 00h–A9h for 3-bit ADPCM and 00h–7Fh for 4-bit ADPCM.

When reading data in the serial voice ROMs by the DTRD command, specify the X address and Y address and then perform the read access operation. The address locations can be specified by 000h–FFFh in the same manner as in the ROM playback. The area of 1K bits in the Y direction is equally divided into 16 of 64K bits each, so that addressing can be performed by 0h–Fh.

Address space allocation of serial voice ROMs.


X address (4K words 000h - FFFh, 1 word = 1K bits)
1k bits
000h
00Fh
010h
3FFh
1M serial voice ROM $\overline{CS1}$
Channel index area (required only for ROM playback by input of address code. 16 words x 1K bits = 16K bits)
ADPCM (voice) data area
1K bits in the Y direction
1 word = 1K bits
Y address
00h
01h
02h
A7h
A8h
A9h
3-bit ADPCM
6 bits
6 bits
6 bits
6 bits
6 bits
10 bits
00h
01h
7Eh
7Fh
4-bit ADPCM
8 bits
8 bits
8 bits
8 bits
0h
1h
2h
Eh
Fh
Read by DTRD command
64 bits
64 bits
64 bits
400h
7FFh
1M serial voice ROM $\overline{CS2}$
800h
BFFh
1M serial voice ROM $\overline{CS3}$
C00h
FFFh
1M serial voice ROM $\overline{CS4}$

Command Description

The MSM6688/6688L is controlled by 19 types of commands via D0-D3 pins constituting the data bus and $\overline{\text{WR}}$, $\overline{\text{RD}}$, $\overline{\text{CE}}$, and CE control pins. The state of the MSM6688/6688L can be know by obtaining the contents of the internal status register via the data bus or the output pins.

There are four command modes available: mode 0, mode 1, mode 2, and mode 3.. Some commands need to set the command mode before inputting them. The command mode can be selected by setting MOD0 bit and MOD1 bit of the SAMP command.

1. Command list

Command	Code				Command function	
	D3	D2	D1	D0		
NOP	0	0	0	0	(NON OPERATION).	Has no function.
PAUSE	0	0	0	1	(PAUSE).	Suspends record/playback temporarily.
PLAY	0	0	1	0	(PLAYBACK).	Sets playback mode.
REC	0	0	1	1	(RECORD).	Sets recording mode.
START	0	1	0	0	(START).	Starts record/playback.
STOP	0	1	0	1	(STOP). Stops execution of CHRW, DTRW, DTRD, and EXT commands.	Stops record/playback.
SAMP	0	1	1	0	(SAMPLING FREQUENCY).	Specifies the command mode and sampling frequency, in conjunction with 1 nibble following this command.
CHAN	0	1	1	1	(CHANNEL).	Specifies a phrase, in conjunction with 2 nibbles following this command.
BLKWR	1	0	0	0	(BLOCK WRITE).	Sets the number of recording blocks (recording time) for the phrase, in conjunction with 2 nibble following this command.
BLKRD	1	0	0	1	(BLOCK READ).	Reads the number of blocks (recording time) for the phrase stored in the channel index area, in conjunction with 2 nibbles following this command. During execution of this command, the contents of the status register cannot be read.
ADRWR	1	0	0	0	(ADDRESS WRITE).	Stores the start address and the stop address to the channel index area, in conjunction with 10 nibbles following this command.
ADRRD	1	0	0	1	(ADDRESS READ).	Reads out the start address and the stop address stored in the channel index area, in conjunction with 10 nibbles following this command. During execution of this command, the contents of the status register cannot be read.

Command	Code				Command function
	D3	D2	D1	D0	
CHRW	1	0	1	0	(CHANNEL READ WRITE). Reads out the user data stored in the channel index area or writes the user data to the channel index area by the read/write access operation following this command.
DTRW	1	0	1	0	(DATA READ WRITE). Transfers data to or from the external serial registers through the data bus, by the address designation in 5 nibbles following this command and the read/write access operation.
DTRD	1	0	1	0	(DATA READ). Reads the data in the external serial voice ROMs through the data bus, by the address designation in 5 nibbles following this command and the read/write access operation.
EXT	1	0	1	1	(EXTERNAL). Performs record/playback by inputting/outputting ADPCM data through the data bus, in conjunction with the read/write access operation. This command will be used when an SRAM or a hard disk is used for storing voice data. Does not control external serial registers and addresses.
VDS	1	1	0	0	(VOICE DETECT SELECT). Selects the ADPCM bit length and voice triggered starting function, in conjunction with 1 nibble following this command.
DEL	1	1	0	1	(DELETE). Deletes the phrase specified by the CHAN command. When ch00 is specified by the CHAN command, all phrases are deleted by this command.
LEV	1	1	1	0	(LEVEL) Specifies the playback output level and the transition of analog output (AOUT pin) to the DC level, in conjunction of 1 nibble following this command. This level is initialized by the RESET input.
NOP	1	1	1	1	(NON OPERATION). Has no function.

2. Command format

MOD1					0	0	1	1
MOD0					0	1	0	1
Code					Mode 0	Mode 1	Mode 2	Mode 3
D3	D2	D1	D0	HEX				
0	0	0	0	0h	NOP	NOP	NOP	NOP
0	0	0	1	1h	PAUSE	PAUSE	PAUSE	PAUSE
0	0	1	0	2h	PLAY	PLAY	PLAY	PLAY
0	0	1	1	3h	REC	REC	REC	REC
0	1	0	0	4h	START (Flex record/ playback)	START (ROM playback by input of address code)	START (Direct record/ playback)	START (Direct ROM playback)
0	1	0	1	5h	STOP	STOP	STOP	STOP
0	1	1	0	6h	SAMP	SAMP	SAMP	SAMP
0	1	1	1	7h	CHAN	CHAN	CHAN	CHAN
1	0	0	0	8h	BLKWR	BLKWR	ADRWR	ADRWR
1	0	0	1	9h	BLKRD	BLKRD	ADRRD	ADRRD
1	0	1	0	Ah	CHRW	CHRW	DTRW	DTRD
1	0	1	1	Bh	EXT	EXT	EXT	EXT
1	1	0	0	Ch	VDS	VDS	VDS	VDS
1	1	0	1	Dh	DEL	DEL	DEL	DEL
1	1	1	0	Eh	LEV	LEV	LEV	LEV
1	1	1	1	Fh	NOP	NOP	NOP	NOP

3. Command data format

Command	Code HEX		D3	D2	D1	D0	Note
NOP	0h		0	0	0	0	1-nibble command
PAUSE	1h		0	0	0	1	1-nibble command
PLAY	2h		0	0	1	0	1-nibble command
REC	3h		0	0	1	1	1-nibble command
START	4h		0	1	0	0	1-nibble command
STOP	5h		0	1	0	1	1-nibble command
SAMP	6h	1st nibble	0	1	1	0	2-nibble command
		2nd nibble	MOD1	MOD0	SA1	SA0	Command mode, sampling frequency

MOD1	MOD0	Command mode
0	0	Mode 0
0	1	Mode 1
1	0	Mode 2
1	1	Mode 3

SA1	SA0	Sampling frequency
0	0	f_{OSC}/1024 (4.0kHz)
0	1	f_{OSC}/768 (5.3kHz)
1	0	f_{OSC}/640 (6.4kHz)
1	1	f_{OSC}/512 (8.0kHz)

Values in parentheses are for fosc = 4.096 MHz.

Command	Code HEX		D3	D2	D1	D0	Note
CHAN	7h	1st nibble	0	1	1	1	3-nibble command
		2nd nibble	CA3	CA2	CA1	CA0	Phrase No.
		3rd nibble	CA7	CA6	CA5	CA4	

CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0	Phrase No.
0	0	0	0	0	0	0	0	ch00
0	0	0	0	0	0	0	1	ch01
0	0	0	0	0	0	1	0	ch02
0	0	0	0	0	0	1	1	ch03
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	1	0	chFE
1	1	1	1	1	1	1	1	chFF

Command	Code HEX		D3	D2	D1	D0	Note
BLKWR	8h	1st nibble	1	0	0	0	3-nibble command
		2nd nibble	BL3	BL2	BL1	BL0	Number of blocks
		3rd nibble	BL7	BL6	BL5	BL4	
BLKRD	9h	1st nibble	1	0	0	1	3-nibble command
		2nd nibble	BL3	BL2	BL1	BL0	Number of blocks
		3rd nibble	BL7	BL6	BL5	BL4	
ADRWR	8h	1st nibble	1	0	0	0	11-nibble command
		2nd nibble	SPY3	SPY2	SPY1	SPY0	Stop Y address
		3rd nibble	SPY7	SPY6	SPY5	SPY4	
		4th nibble	SPX3	SPX2	SPX1	SPX0	Stop X address
		5th nibble	SPX7	SPX6	SPX5	SPX4	
		6th nibble	SPX11	SPX10	SPX9	SPX8	
		7th nibble	SPX15	SPX14	SPX13	SPX12	
		8th nibble	STX3	STX2	STX1	STX0	Start X address
		9th nibble	STX7	STX6	STX5	STX4	
		10th nibble	STX11	STX10	STX9	STX8	
		11th nibble	STX15	STX14	STX13	STX12	
ADRRD	9h	1st nibble	1	0	0	1	11-nibble command
		2nd nibble	SPY3	SPY2	SPY1	SPY0	Stop Y address
		3rd nibble	SPY7	SPY6	SPY5	SPY4	
		4th nibble	SPX3	SPX2	SPX1	SPX0	Stop X address
		5th nibble	SPX7	SPX6	SPX5	SPX4	
		6th nibble	SPX11	SPX10	SPX9	SPX8	
		7th nibble	SPX15	SPX14	SPX13	SPX12	
		8th nibble	STX3	STX2	STX1	STX0	Start X address
		9th nibble	STX7	STX6	STX5	STX4	
		10th nibble	STX11	STX10	STX9	STX8	
		11th nibble	STX15	STX14	STX13	STX12	

Command	Code HEX		D3	D2	D1	D0	Note
CHRW	Ah		1	0	1	0	1-nibble command + read/write access + STOP command
DTRW	Ah	1st nibble	1	0	1	0	6-nibble command + read/write access + STOP command
		2nd nibble	0	0	0	0	Dummy nibble
		3rd nibble	X3	X2	X1	X0	X address
		4th nibble	X7	X6	X5	X4	
		5th nibble	X11	X10	X9	X8	
		6th nibble	X15	X14	X13	X12	
DTRD	Ah	1st nibble	1	0	1	0	6-nibble command + read access + STOP command
		2nd nibble	Y3	Y2	Y1	Y0	Y address
		3rd nibble	X3	X2	X1	X0	X address
		4th nibble	X7	X6	X5	X4	
		5th nibble	X11	X10	X9	X8	
		6th nibble	0	0	0	0	Dummy nibble
EXT	Bh		1	0	1	1	1-nibble command + read/write access + STOP command
VDS	ch	1st nibble	1	1	0	0	2-nibble command
		2nd nibble	0	BIT	VD1	VD0	ADPCM bit length, voice triggered starting condition

BIT	ADPCM bit length
0	3 bits
1	4 bits

VD1	VD0	Voice detection level V_{VDS}	
		MSM6688 (5 V version)	MSM6688L (3 V version)
0	0	Voice triggered starting disabled	Voice triggered starting disabled
0	1	$\pm V_{DD}/64$ ($\pm$80mV)*	$\pm V_{DD}/128$ ($\pm$24mV)**
1	0	$\pm V_{DD}/32$ ($\pm$160mV)*	$\pm V_{DD}/64$ ($\pm$48mV)**
1	1	$\pm V_{DD}/16$ ($\pm$320mV)*	$\pm V_{DD}/32$ ($\pm$96mV)**

* Values in parentheses are for V_{DD} = 5.12 V.
** Values in parentheses are for V_{DD} = 3.072 V.

<table>
<tr><th>Command</th><th>Code HEX</th><th></th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Note</th></tr>
<tr><td rowspan="2">DEL</td><td rowspan="2">Dh</td><td></td><td>1</td><td>1</td><td>0</td><td>1</td><td>1-nibble command</td></tr>
<tr><td></td><td colspan="5">ch00: Deletion of all phrases
ch01 - chFF: Deletion of a specified phrase</td></tr>
<tr><td rowspan="3">LEV</td><td rowspan="3">Eh</td><td>1st nibble</td><td>1</td><td>1</td><td>1</td><td>0</td><td>2-nibble command</td></tr>
<tr><td>2nd nibble</td><td>LV1</td><td>LV0</td><td>PN1</td><td>PN0</td><td>Playback level, transition to DC level</td></tr>
<tr><td></td><td colspan="5">
<table>
<tr><th>LV1</th><th>LV0</th><th>Playback level</th></tr>
<tr><td>0</td><td>0</td><td>0dB</td></tr>
<tr><td>0</td><td>1</td><td>0dB</td></tr>
<tr><td>1</td><td>0</td><td>–6dB</td></tr>
<tr><td>1</td><td>1</td><td>–12dB</td></tr>
</table>
<table>
<tr><th>PN1</th><th>PN0</th><th>Transition to DC level</th></tr>
<tr><td>0</td><td>0</td><td>Disabled</td></tr>
<tr><td>0</td><td>1</td><td>Disabled</td></tr>
<tr><td>1</td><td>0</td><td>Transition from GND to 1/2 V_{DD}.</td></tr>
<tr><td>1</td><td>1</td><td>Transition from 1/2 V_{DD} to GND.</td></tr>
</table>
</td></tr>
<tr><td>NOP</td><td>Fh</td><td></td><td>1</td><td>1</td><td>1</td><td>1</td><td>1-nibble command</td></tr>
</table>

4. Relationship between record/playback control modes and commands

Record/playback mode Command	Flex record/ playback	ROM playback by input of address code	Direct record/ playback	Direct ROM playback	EXT command record/playback
NOP	—	—	—	—	—
PAUSE	○	○	○	○	—
PLAY	◎	—	◎	—	◎
REC	◎	—	◎	—	◎
START	◎	◎	◎	◎	—
STOP	○	○	○	○	◎
SAMP	◎	◎	◎	◎	◎
Command mode	◎	◎	◎	◎	◎
Sampling frequency	◎	—	◎	◎	◎
CHAN	◎	◎	◎	◎	—
BLKWR	◎	—	—	—	—
BLKRD	○	—	—	—	—
ADRWR	○	—	◎	◎	—
ADRRD	○	—	○	—	—
CHRW	Data transfer command				
DTRW	Data transfer command				
DTRD	Data transfer command				
EXT	—	—	—	—	◎
VDS	◎	—	◎	◎	◎
ADPCM bit length	◎	—	◎	◎	◎
Voice triggered starting condition	◎	—	◎	—	—
DEL	◎	—	○	—	—
Deletion of all phrases	◎	—	○	—	—
Deletion of a specified phrase	○	—	○	—	—
LEV	○	○	○	○	○

Note: ◎ : Required command ○ : Effective command — : Unnecessary command

Status Register

The status register used in the MSM6688/6688L is a 4-bit status register. When a low level is applied to the $\overline{\text{RD}}$ pin, the contents of the status register are output to D0–D3 pins to indicate the internal state of the MSM6688/6688L. The contents of the status register are also output to the BUSY, RPM, VPM, and NAR pins.

D3	D2	D1	D0
NAR	VPM	RPM	BUSY

(1) BUSY bit

The BUSY bit set to a high level indicates that the MSM6688/6688L is executing RESET operation or command processing operation. When BUSY bit is high, do not input any command from the microcontroller. While any of data read commands is being executed, the state of the BUSY bit cannot be verified by inputting the $\overline{\text{RD}}$ pulse. In this case, input a read command either after waiting a time longer than the duration of BUSY state or after verifying the end of the busy state by the BUSY pin.

While the RESET operation is being executed, the BUSY bit is set to a high level, and it returns to a low level after the end of the RESET operation. After a high level pulse is applied to the RESET pin to perform the RESET operation, the BUSY bit is set to a high level during execution of the RESET operation. It goes to a low level after the end of the RESET operation.

(2) RPM bit

The RPM bit goes to a high level during record/playback operation. While the RPM bit is high, do not input any command except those indicated below. Otherwise, the state of the MSM6688/6688L becomes undefined.

NOP, PAUSE, STOP commands, START command for release of temporary stop and playback of next phrase, CHAN command for specifying the next phrase during playback and LEV command for designation of playback output level.

After a high level pulses is applied to the RESET pin to perform the RESET operation, the RPM bit goes to a low level that is the initial state.

(3) VPM bit

The VPM bit goes to a high level during standby for voice after start of the voice triggered recording and during the time that record/playback is temporarily stopped by the PAUSE command.

When the VPM bit is high, do not apply any command except the STOP command and the START command for release of temporary stop. Otherwise, the state of the MSM6688/6688L becomes undefined.

After a high level pulse is applied to the RESET pin to perform the reset operation, the VPM bit goes to a low level that is the initial state.

(4) NAR bit

The NAR bit indicate the enabled or disabled state for phrase designation. When this bit is high, the phrase designation by the CHAN command is enabled.

If it is desired to play back different phrases continuously during ROM playback, specify the next phrase and input the START command after verifying that the NAR bit becomes high.

After a high level pulse is applied to the RESET pin to perform the reset operation, the NAR bit goes to a high level that is the initial state.

BUSY causing conditions	Symbol	BUSY state duration	BUSY bit verification	Note
Release of reset operation	t_{REX}	(Note 2) 1 ms	Possible	Input of RESET pulse
Input of 1-nibble command	t_{B1}	16 µs	Possible	NOP, PAUSE, PLAY, REC, START, STOP
Input of 2-nibble command	t_{B2}	16 µs	Possible	SAMP, VDS, LEV
Input of 3-nibble command	t_{B3}	16 µs	Possible	CHAN, BLKWR
Input of 2-nibble or 3-nibble command data	t_{BD}	16 µs	Possible	SAMP, VDS, LEV, CHAN, BLKWR
BLKRD command				
Input of command	t_{WBR}	270 µs	Impossible	
Output of block data	t_{WDR}	50 µs	Impossible	
ADRWR command				
Input of command	t_{BAW}	270 µs	Possible	
Input of address data	t_{BAD}	50 µs	Possible	
ADRRD command				
Input of command	t_{WAR}	270 µs	Impossible	
Output of address data	t_{WDR}	50 µs	Impossible	
CHRW command				
Input of command	t_{WCRW}	770 µs	Possible	
Input of REC command	t_{WRC}	16 µs	Possible (Note 1)	
Input of write data	t_{WWD}	50 µs	Possible (Note 1)	
Input of PLAY command	t_{WPL}	50 µs	Impossible	
Input of STOP command	t_{WSP}	50 µs	Possible (Note 1)	
DTRW and DTRD commands				
Input of command	t_{WRW}	16 µs	Possible	
Input of address (2nd ~ 5th nibbles)	t_{WA1}	16 µs	Possible	
Input of address (6th nibble)	t_{WA2}	270 µs	Possible	
Input of REC command	t_{WRC}	16 µs	Possible (Note 1)	
Input of write data	t_{WWD}	50 µs	Possible (Note 1)	
Input of PLAY command	t_{WPL}	50 µs	Impossible	
Input of STOP command	t_{WSP}	50 µs	Possible (Note 1)	
Input of DEL command (all phrases)	t_{WBLA}	550 ms	Possible	
Input of DEL command (a specified phrase)	t_{WBL1}	70 ms	Possible	

Note:
1. The BUSY state can be verified by the BUSY bit when only the data write access operation is executed after the CHRW or DTRW command is input.
2. The BUSY state duration after release of RESET operation includes the oscillation startup stabilization time. This oscillation startup stabilization time is several tens of milliseconds for crystal oscillators and is several hundreds of microseconds for ceramic oscillators.

Inputting the Commands

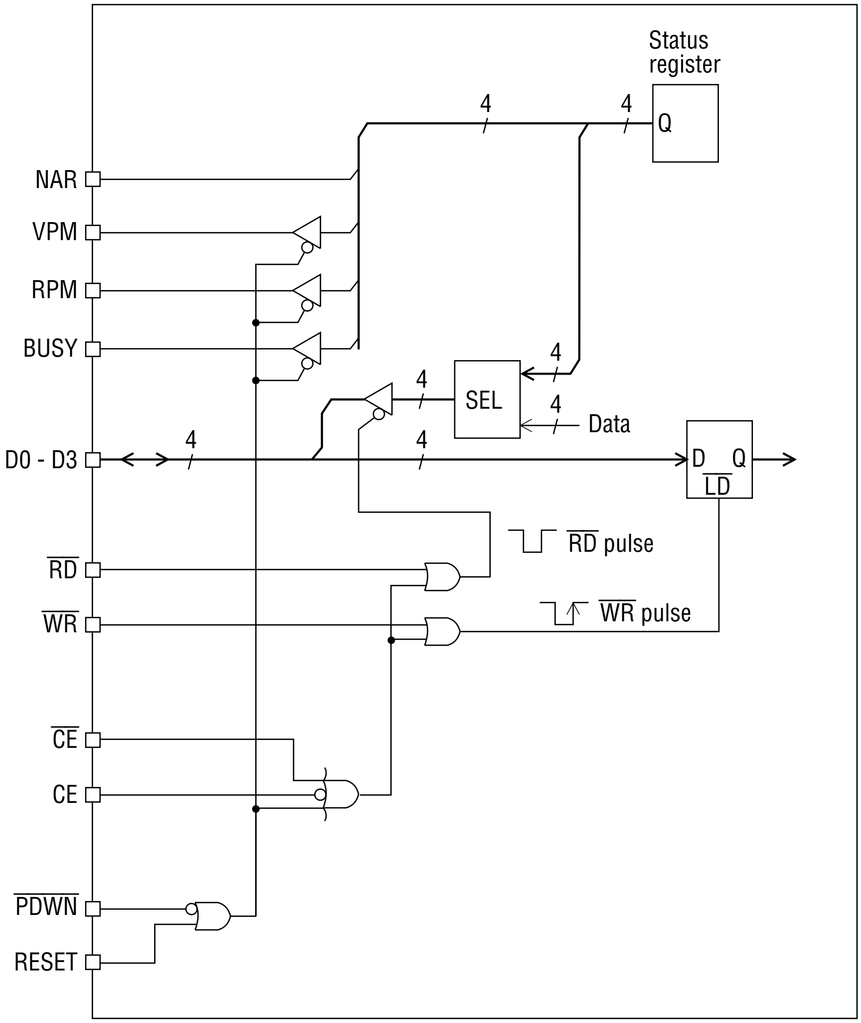
To input a command or data, apply the command or data to D0–D3 pins and then apply a low level pulse ($\overline{\text{WR}}$ pulse) to the $\overline{\text{WR}}$ pin.

By inputting a low level pulse ($\overline{\text{RD}}$ pulse) to the $\overline{\text{RD}}$ pin, the contents of the status register or data will be output via D0–D3 pins.

The $\overline{\text{CE}}$ pin is used to enable or disable the $\overline{\text{WR}}$ pulse and $\overline{\text{RD}}$ pulse. When a low-level is applied to this $\overline{\text{CE}}$ pin, the enable state is present, so that $\overline{\text{WR}}$ and $\overline{\text{RD}}$ pulses can be accepted. When a high level is applied to this $\overline{\text{CE}}$ pin, the disable state is present, so that $\overline{\text{WR}}$ and RD pulses cannot be accepted and, at the same time, D0–D3 pins are placed in the high-impedance state.

The CE pin also has the same function as the $\overline{\text{CE}}$ pin. However, when high, this CE pin gives the enable state for the $\overline{\text{WR}}$ and $\overline{\text{RD}}$ pulses, and when low, it gives the disable state. When D0–D3 pins are used exclusively for the MSM6688/6688L, $\overline{\text{CE}}$ and CE pins can be fixed to a low level and a high level, respectively.

An equivalent circuit of the microcontroller interface section of the MSM6688/6688L is shown below.

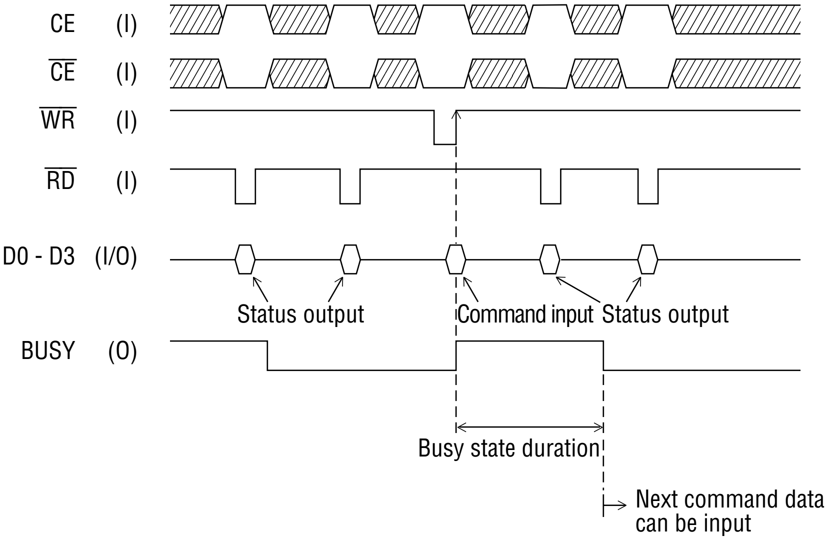

Status register
4
4
Q
NAR
VPM
RPM
BUSY
4
4
SEL
4
Data
D0 - D3
4
4
D Q
$\overline{\text{LD}}$
$\overline{\text{RD}}$ pulse
$\overline{\text{WR}}$ pulse
$\overline{\text{RD}}$
$\overline{\text{WR}}$
$\overline{\text{CE}}$
CE
$\overline{\text{PDWN}}$
RESET

The steps for inputting the commands are described below.

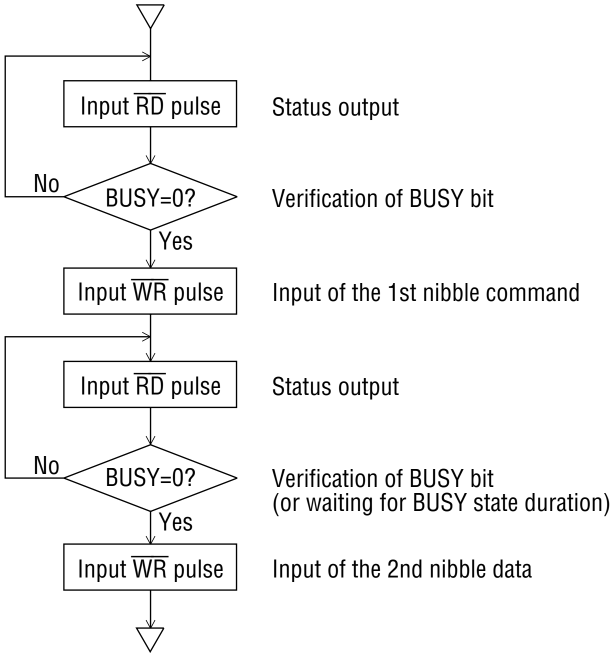
(1) Output the contents of the status register by applying the $\overline{\text{RD}}$ pulse (namely, by applying a low level pulse to the $\overline{\text{RD}}$ pin). Verify that the BUSY bit is 0. If the BUSY bit is 1, input the $\overline{\text{RD}}$ pulse repeatedly until the BUSY bit goes to 0. The BUSY state can also be verified through the BUSY pin.

(2) Set a command to D0–D3 pin and input the $\overline{\text{WR}}$ pulse.

(3) In case of a 2-nibble or 3-nibble command, verify that the BUSY bit of the status register is 0 in the same way as in (1). Then, set the command data to D0–D3 pins and input the $\overline{\text{WR}}$ pulse. In this case, the $\overline{\text{WR}}$ pulse can also be input after the waiting time that is longer than the BUSY state duration, instead of verifying the BUSY bit of the status register.


CE (I)
$\overline{\text{CE}}$ (I)
$\overline{\text{WR}}$ (I)
$\overline{\text{RD}}$ (I)
D0 - D3 (I/O)
Status output
Command input
Status output
BUSY (O)
Busy state duration
Next command data can be input

1. Inputting a 2-nibble command


Input $\overline{\text{RD}}$ pulse
Status output
No
BUSY=0?
Verification of BUSY bit
Yes
Input $\overline{\text{WR}}$ pulse
Input of the 1st nibble command
Input $\overline{\text{RD}}$ pulse
Status output
No
BUSY=0?
Verification of BUSY bit
(or waiting for BUSY state duration)
Yes
Input $\overline{\text{WR}}$ pulse
Input of the 2nd nibble data

Changes of Record/Playback Conditions

Record/playback condition	POWER ON	RESET input	$\overline{\text{PDWN}}$ input	Command input
Record/playback mode	Undefined	Unchanged (Note 1)	Unchanged	REC command → Record mode PLAY command → Playback mode
Command mode	Undefined	Unchanged (Note 1)	Unchanged	Set by SAMP command
Sampling frequency	Undefined	Unchanged (Note 1)	Unchanged	Set by SAMP command
Phrase No.	Undefined	Unchanged (Note 1)	Unchanged	Set by CHAN command
Number of phrase recording blocks	Undefined	Unchanged (Note 1)	Unchanged	Set by BLKWR command
ADPCM bit length	Undefined	Unchanged (Note 1)	Unchanged	Set by VDS command
Voice triggered starting	Undefined	Unchanged (Note 1)	Unchanged	Set by VDS command
Playback level	Undefined	0dB	Unchanged	Set by LEV command
Data in serial registers	Undefined	Unchanged (Note 1)	Unchanged	—

Note: 1. RESET is performed without synchronization with the clock.
When the RESET pulse is input during standby for commands, record/playback condition will not be changed. When the RESET pulse is input during execution of a command, all record/playback conditions may be changed and the data may become undefined.

Setting and Confirming the Record/Playback Conditions

1. Specifying the control mode for record/playback (by the SAMP command)

Specify the control mode for record / playback by setting the command mode (using MOD1 and MOD0 bits) as shown in the following table.

MOD1	MOD0	Command mode	Control mode for record/playback
0	0	Mode 0	Flex record/playback
0	1	Mode 1	ROM playback by input of address code
1	0	Mode 2	Direct record/playback
1	1	Mode 3	Direct ROM playback

2. Specifying the sampling frequency (by the SAMP command)

Specify the sampling frequency by setting SA0 and SA1 bit data of the SAMP command. The relationship between the master oscillator frequency (f_{OSC}), and sampling frequency (f_{SAMP}) depends on the SA0 and SA1 bit data of the SAMP command as shown in the following table.

SA1	SA0	Sampling frequency fsamp
0	0	f_{OSC}/1024 (4.0kHz)
0	1	f_{OSC}/768 (5.3kHz)
1	0	f_{OSC}/640 (6.4kHz)
1	1	f_{OSC}/512 (8.0kHz)

( ) Values in parentheses are for f_{OSC}=4.096MHz.

3. Specifying the ADPCM bit length (by the VDS command)

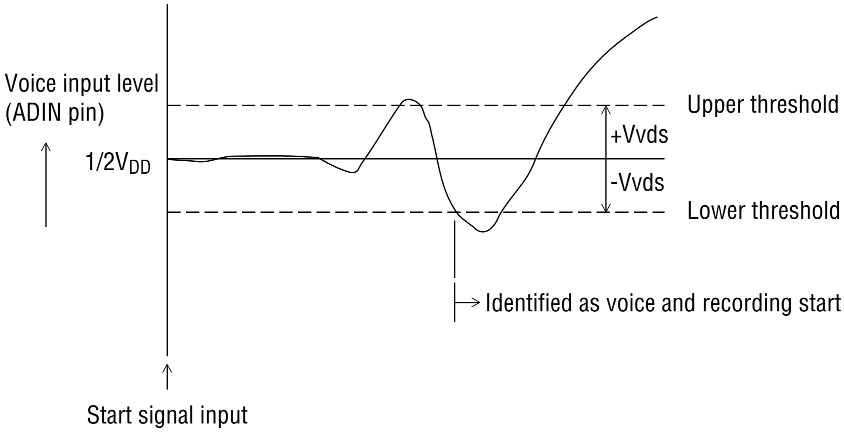
Specify the ADPCM bit length by setting the BIT bit data of the VDS command as shown in the following table.

BIT	ADPCM bit length
0	3 bits
1	4 bits

4. Specifying the voice triggered starting (by the VDS command)

This MSM6688/6688L has the voice triggered starting function that starts recording when the level of voice input exceeds a preset amplitude. Using the voice activated function, the unvoiced part prior to voice detection will not be recorded, so that the memory capacity can be utilized efficiently.

The unvoiced parts in the middle of recording are not eliminated. In the voice triggered starting mode, recording is started when a voice input exceeds the preset thresholds. Therefore, a consonant part with a low level may not be recorded.

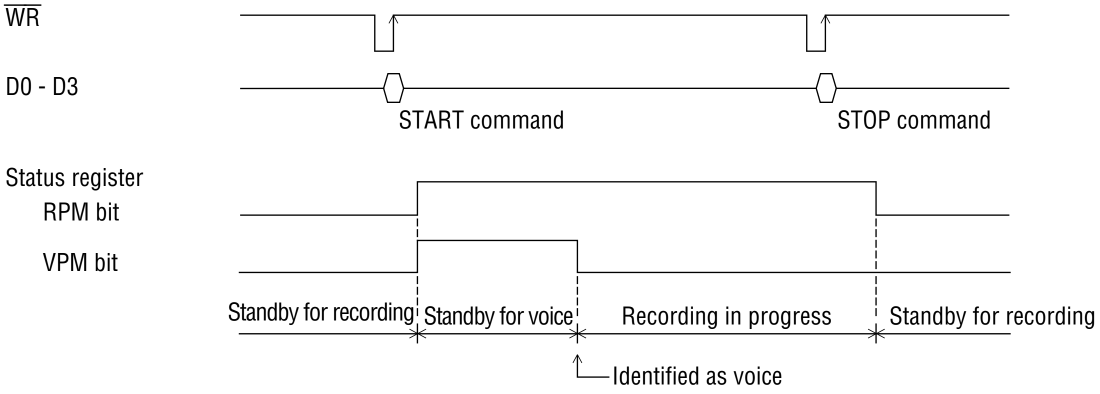

Voice input level
(ADIN pin)
1/2V$_{DD}$
Upper threshold
+Vvds
-Vvds
Lower threshold
Identified as voice and recording start
Start signal input

Specify the enable/disable of the voice triggered starting function and the voice detection level by VD0 and VD1 bit data of the VDS command as shown in the following table.

VD1	VD0	Voice detection level, V_{vds}	
		MSM6688 (5 V version)	MSM6688L (3 V version)
0	0	Voice triggered starting disabled	Voice triggered starting disabled
0	1	$\pm V_{DD}/64$ (±80mV)*	$\pm V_{DD}/128$ (±24mV)**
1	0	$\pm V_{DD}/32$ (±160mV)*	$\pm V_{DD}/64$ (±48mV)**
1	1	$\pm V_{DD}/16$ (±320mV)*	$\pm V_{DD}/32$ (±96mV)**

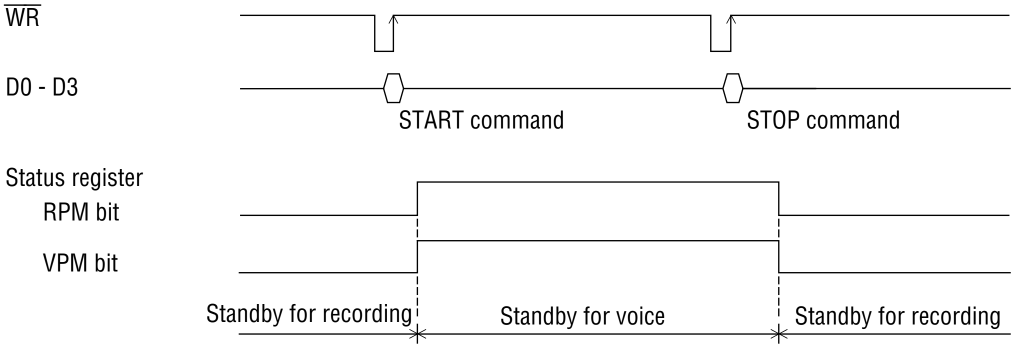
* Values in parentheses are for V_{DD}=5.12 V.
** Values in parentheses are for V_{DD}=3.072 V.

During standby for voice, the VPM bit of the status register is 1. This bit returns to 0 at the start of recording after detection of voiced signal. The RPM bit is 1 during standby for voice and during recording.


WR
D0 - D3
START command
STOP command
Status register
RPM bit
VPM bit
Standby for recording
Standby for voice
Recording in progress
Standby for recording
Identified as voice

When the STOP command is input during standby for voice, standby for voice will be finished and changed to standby for recording,

If in the flex record/playback mode, the STOP command is input during standby for voice, the contents of the specified phrase will be deleted.


WR
D0 - D3
START command
STOP command
Status register
RPM bit
VPM bit
Standby for recording
Standby for voice
Standby for recording

5. Specifying a phrase (by the CHAN command)

Specify a phrase by CA0–CA7 bit data of the CHAN command as shown in the following table.

CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0	Phrase No.	Flex record/ playback	ROM playback by input of address code	Direct record/ playback	Direct ROM playback
0	0	0	0	0	0	0	0	ch00	(Note 1)	Disabled	Enable (64 phrases)	Enable (Note 2)
0	0	0	0	0	0	0	1	ch01	Enable (63 phrases)	Enable (255 phrases)		
0	0	0	0	0	0	1	0	ch02				
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮				
0	0	1	1	1	1	1	0	ch3E				
0	0	1	1	1	1	1	1	ch3F				
0	1	0	0	0	0	0	0	ch40	Inhibit		Inhibit	Inhibit
0	1	0	0	0	0	0	1	ch41				
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮				
1	1	1	1	1	1	1	0	chFE				
1	1	1	1	1	1	1	1	chFF				

Note:

1. In the flex record/playback mode, ch00 cannot be used for recording/playback. This is a special phrase only used for deletion of all phrases and control of unused blocks.

2. In the direct ROM playback mode, playback will be started after transferring the address data to the channel index area of the serial registers. Therefore, it is required for direct ROM playback to use a phase unused for record/playback operation. Normally, phrase ch3FH is used as the phrase dedicated for direct ROM playback.

6. Specifying the number of phrase recording blocks (by the BLKWR command)

In the flex record/playback mode, set the number of blocks before starting the recording to specify the recording time for a phrase. In this mode, the total memory capacity of serial registers connected externally is divided equally into 256 blocks. Therefore, the memory capacity of one block varies depending on the number of serial registers connected externally.

For example, when one 8M bit serial register is connected and recording is performed by 4-bit ADPCM and 8-kHz sampling, the memory capacity of one block and the recording time of one block are obtained as follows.

$$\text{Memory capacity of one block} = \frac{\text{8M bits}}{256} = \text{32K bits}$$

$$\text{Recording time/block} = \frac{\text{Memory capacity of one block}}{\text{Sampling frequency} \times \text{ADPCM bit length}}$$

$$= \frac{32 \times 1024 \times \text{bits}}{8000\ \text{Hz} \times 4\ \text{bits}} = \text{Approximately 1 second}$$

If it is desired to make recording for 10 seconds on a phrase in this example, 10 (0Ah) phrase recording blocks are required.

The number of phrase recording blocks can be specified by the BLKWR command and is stored in the (corresponding) register in the MSM6688/6688L. The BLKWR command is enabled for command mode 0 or 1. Therefore, before inputting this BLKWR command, it is required to set the corresponding command mode using the SAMP command.

BL7	BL6	BL5	BL4	BL3	BL2	BL1	BL0	Number of phrase recording blocks (HEX)
0	0	0	0	0	0	0	0	Input inhibit
0	0	0	0	0	0	0	1	1 (01h)
0	0	0	0	0	0	1	0	2 (02h)
0	0	0	0	0	0	1	1	3 (03h)
¦	¦	¦	¦	¦	¦	¦	¦	¦
1	1	1	1	1	1	1	0	254 (FEh)
1	1	1	1	1	1	1	1	255 (FFh)

7. Reading the number of phrase recording blocks (by the BLKRD command)

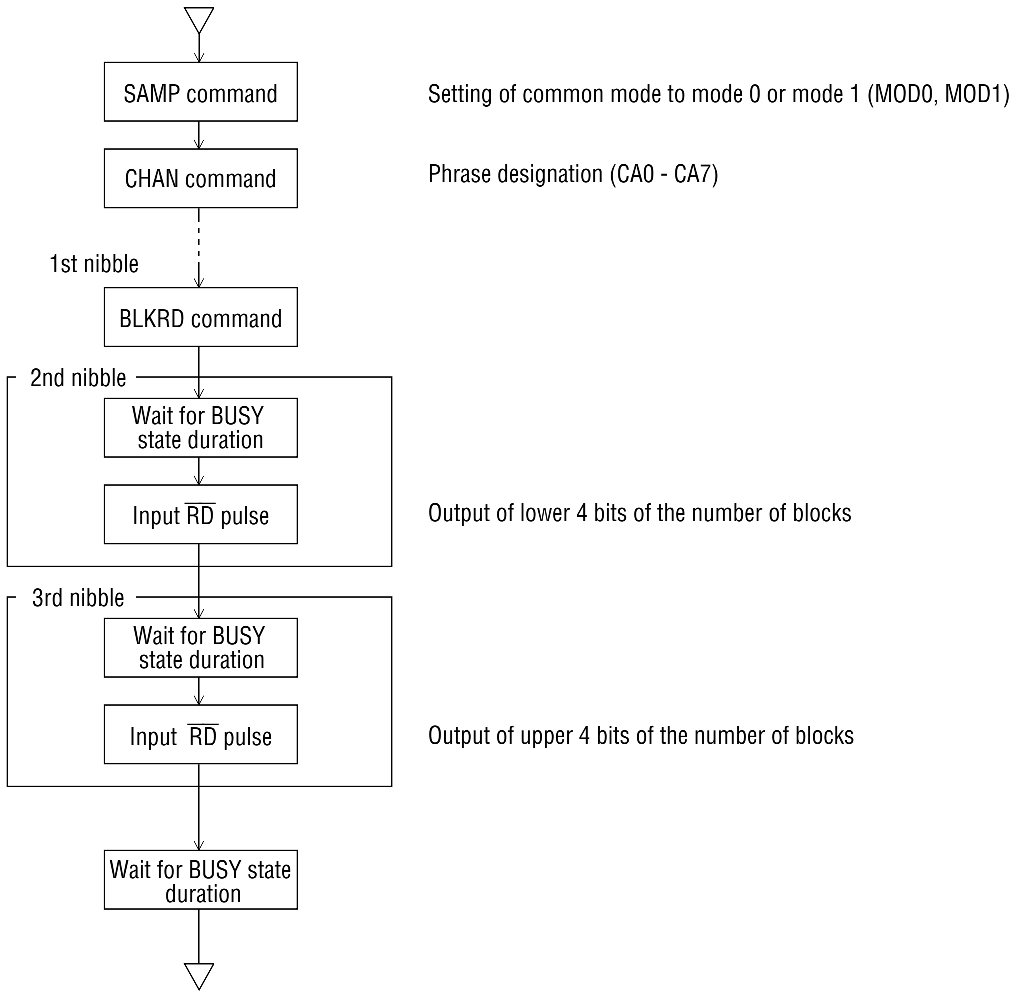
The number of blocks for each phrase stored in the channel index area can be read by the read access operation using the BLKRD command and two nibbles following this BLKRD command. In the flex record/playback mode, the number of blocks (namely, the recording time) of the specified phrase can be obtained. In the BLKRD command, the number of blocks is specified by a binary number consisting of BL0–BL7 in the same way as in the BLKWR command.

Before inputting the BLKRD command, the command mode must be set to either mode 0 or mode 1 by using the SAMP command.

(1) When ch00 phrase is specified: The number of unused blocks (or available blocks) is stored in address ch00 of the channel index area. Therefore, the unused and available memory capacity (or available recording time) can be obtained.

(2) When one of ch01–ch3F is specified as a phrase: The number of blocks (or recording time) used by the specified phrase can be obtained.

BLKRD command flow chart


SAMP command
Setting of common mode to mode 0 or mode 1 (MOD0, MOD1)
CHAN command
Phrase designation (CA0 - CA7)
1st nibble
BLKRD command
2nd nibble
Wait for BUSY state duration
Input $\overline{\text{RD}}$ pulse
Output of lower 4 bits of the number of blocks
3rd nibble
Wait for BUSY state duration
Input $\overline{\text{RD}}$ pulse
Output of upper 4 bits of the number of blocks
Wait for BUSY state duration

During execution of the BLKRD command, verification of the status register cannot be performed by input of the $\overline{\text{RD}}$ pulse. When inputting the $\overline{\text{RD}}$ pulse for the 2nd nibble or 3rd nibble or inputting the next command after the BLKRD command, input the $\overline{\text{RD}}$ pulse either after the waiting time longer than the BUSY state duration or after verifying that the BUSY status is not present via the BUSY pin.

8. Inputting/outputting the address data (by the ADRWR/ADRRD command)

In the direct record/playback mode or direct ROM playback, input the start address and stop address of a phrase directly into the channel index area in the RAM by the ADRWR command.

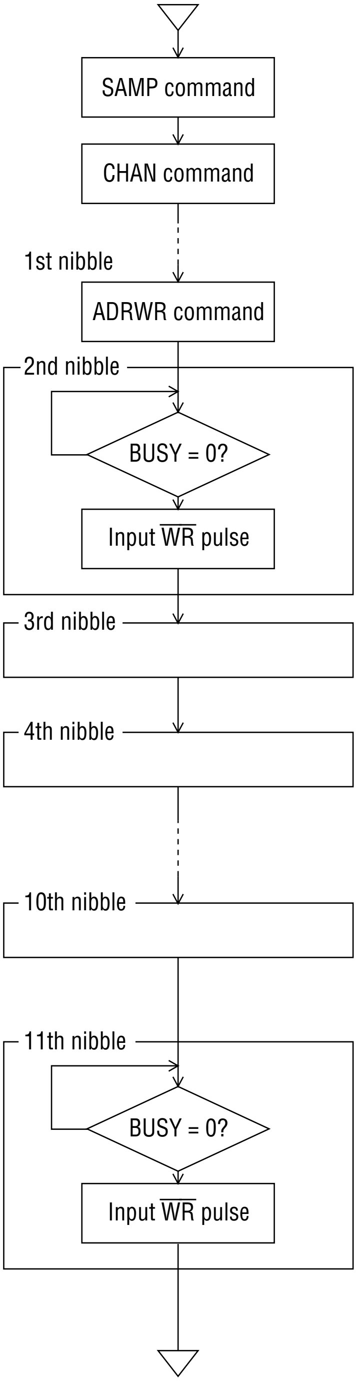
The ADRRD command is used to read the address data stored in the channel index area.

The header 40 bits of each phrase of the channel index area can be accessed by the ADRWR or ADRRD command. In the flex record/playback mode, these commands can be used to change the address data for deleting the tail part of a recorded phrase.

	Direct record/playback and direct ROM playback					**Flex record/playback**				
	D3	**D2**	**D1**	**D0**	**Contents**	**D3**	**D2**	**D1**	**D0**	**Contents**
1st nibble	1	0	0	*	Command	1	0	0	*	Command
2nd nibble	SPY3	SPY2	SPY1	SPY0	Stop Y address	BL3	BL2	BL1	BL0	Number of blocks
3rd nibble	SPY7	SPY6	SPY5	SPY4		BL7	BL6	BL5	BL4	
4th nibble	SPX3	SPX2	SPX1	SPX0	Stop X address	SPY3	SPY2	SPY1	SPY0	Stop Y address
5th nibble	SPX7	SPX6	SPX5	SPX4		SPY7	SPY6	SPY5	SPY4	
6th nibble	SPX11	SPX10	SPX9	SPX8		SPX3	SPX2	SPX1	SPX0	Stop X address
7th nibble	SPX15	SPX14	SPX13	SPX12		SPX7	SPX6	SPX5	SPX4	
8th nibble	STX3	STX2	STX1	STX0	Start X address	SP3	SP2	SP1	SP0	Stop block
9th nibble	STX7	STX6	STX5	STX4		SP7	SP6	SP5	SP4	
10th nibble	STX11	STX10	STX9	STX8		PR3	PR2	PR1	PR0	PRED block
11th nibble	STX15	STX14	STX13	STX12		PR7	PR6	PR5	PR4	

Note: When the address data is input by the ADRWR command in the direct ROM playback mode, the 7th nibble and the 11th nibble are dummy nibbles. Therefore, input 0h data into SPX12–SPX15 (7th nibble) and STX12–STX15 (11th nibble).

ADRWR command flow chart


SAMP command
CHAN command
1st nibble
ADRWR command
2nd nibble
BUSY = 0?
Input $\overline{WR}$ pulse
3rd nibble
4th nibble
10th nibble
11th nibble
BUSY = 0?
Input $\overline{WR}$ pulse

Setting of command mode to mode 2 or mode 3 (MOD = 1)

Phrase designation(CA0 - CA7)

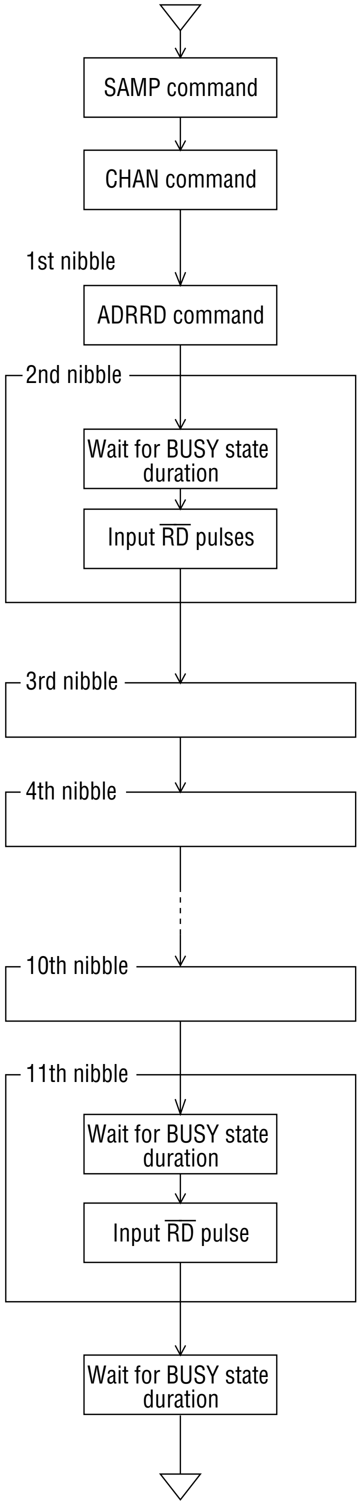
Input of command after verification of BUSY state

BUSY bit verification
(or waiting for BUSY state duration or longer)

Input of address data

Verification of address data

ADDRD command flow chart


SAMP command
CHAN command
1st nibble
ADRRD command
2nd nibble
Wait for BUSY state duration
Input $\overline{\text{RD}}$ pulses
3rd nibble
4th nibble
10th nibble
11th nibble
Wait for BUSY state duration
Input $\overline{\text{RD}}$ pulse
Wait for BUSY state duration

Setting of command mode to mode 2 or mode 3 (MOD0, MOD1)

Phrase designation (CA0 - CA7)

Input of command after verification of BUSY state

Output of address data

Output of address data

During execution of the ADRRD command, verification of the status register cannot be performed by input of the $\overline{\text{RD}}$ pulse. When inputting the $\overline{\text{RD}}$ pulse for the 2nd nibble to 11th nibbles or inputting the next command after the ADRRD command, input the $\overline{\text{RD}}$ pulse either after the waiting time longer than the BUSY state duration or after verifying that the BUSY status is not present via the BUSY pin.

9. Specifying the playback level (by the LEV command)

For playback, one of three output levels 0 dB, –6 dB and –12 dB can be selected. The playback level can be specified by LV0 and LV1 bit data of the LEV command. If the LEV command is input during playback operation, the playback level will be changed at the moment when the command is input. When the RESET pulse is input, the playback output level is set 0 dB that is the initial state.

LV1	LV0	Playback level
0	0	0dB (equal to the voice data amplitude)
0	1	0dB (equal to the voice data amplitude)
1	0	–6dB (one-half of the voice data amplitude)
1	1	–12dB (one-fourth of the voice data amplitude)

Flex Record/Playback Method

1. Deleting phrases

1.1 Deleting all phrases

To delete all phrases, specify ch00 by the CHAN command and input the DEL command. When all phrases are deleted in this manner, "0" data is written into ch01–ch3F addresses of the channel index area of the serial registers to place these addresses in the unrecorded state. The initial data for address control is written in ch00 address. Therefore, whenever the power is turned on, always perform the deletion of all phrases after inputting the RESET pulse.

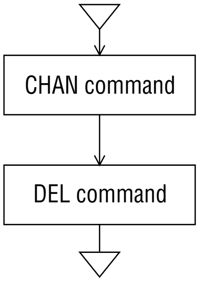
The deletion of all phrases causes the user data area ch00–ch3F to be cleared to all 0s. Note that when the data was transferred to the channel index area by the CHRW command, this data is deleted by the deletion of all phrases.

Phrases No.	**State of the channel index area**		
	Address data	User data	Block table
ch00:	Initial data	Cleared to all 0s	Initial data
ch01-ch3F	Cleared to all 0s		

1.2 Deleting a specified phrase

To delete a specified phrase, specify one of ch0–ch3F by the CHAN command and input the DEL command. The deleted phrase is placed in the unrecorded state. The channel index area for the specified phrase, including the user data, is cleared to all 0s. The data stored in ch00 address for control of unused blocks is updated.

Phrase deletion flow chart



ch00 Deletion of all phrases
ch01 - ch3F: Deletion of a specified phrase

2. Method of recording in the flex record/playback mode

2.1 When only an 8M-bit serial register is used

(1) Before starting the recording operation in the flex record/playback mode, always perform the deletion of all phrases after turning power on and resetting the MSM6688 by input of the RESET pulse. Otherwise, the address control cannot be performed correctly.

(2) Input the record/playback conditions by the corresponding commands as follows.

VDS command:	Specify the ADPCM bit length (BIT) and voice triggered starting (VD0, VD1).
SAMP command:	Set the command mode to mode 0 (MOD0 = 0, MOD1=0) and specify the sampling frequency (SA0, SA1).
CHAN command:	Select phrases (CA0 - CA5) from one of 63 phrases ch01–ch3F.
BLKWR command:	Specify the number of phrase recording blocks (BL0–BL7)
REC command:	Set to the recording mode.

(3) Input the START command to start recording

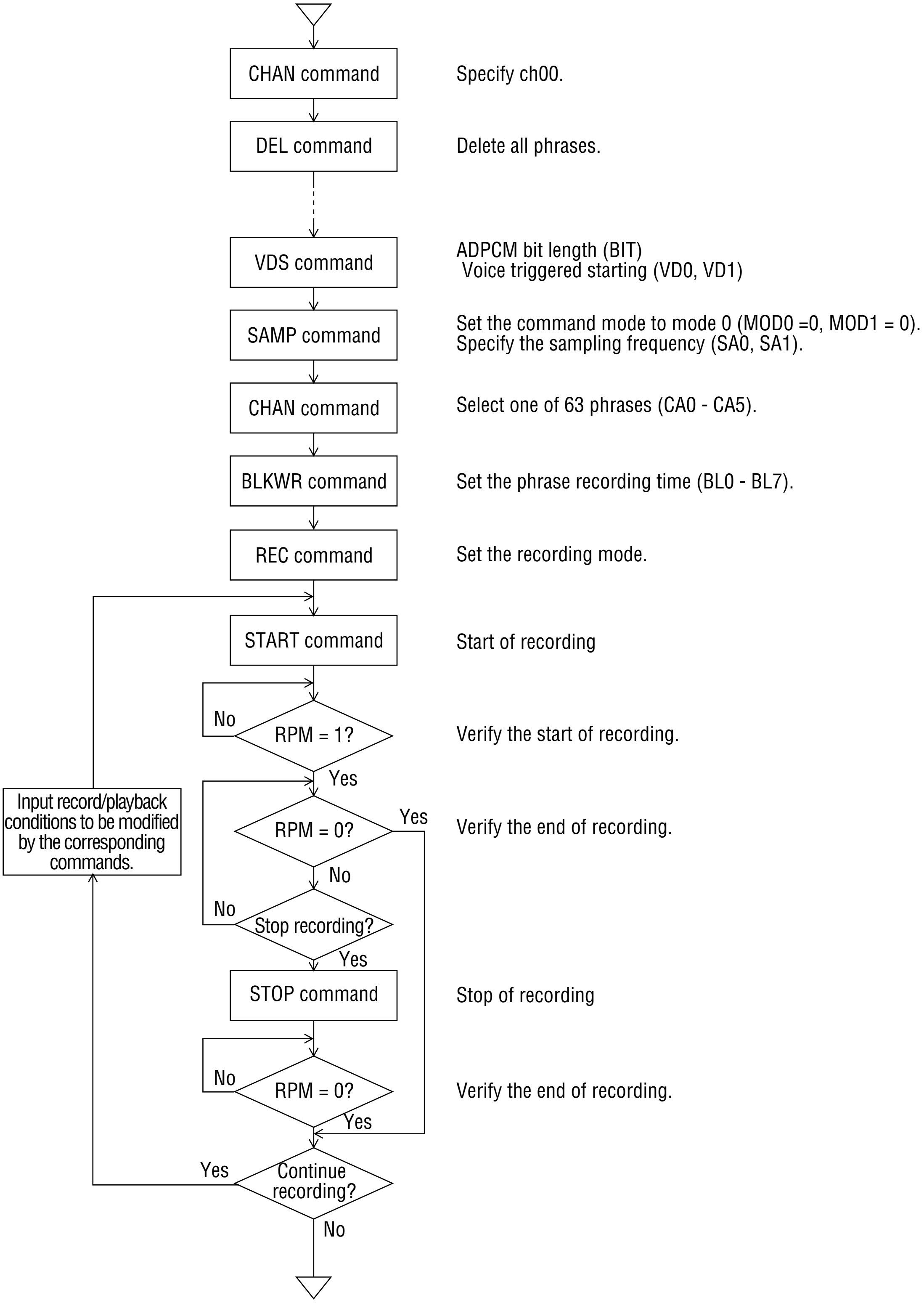
(4) When the number of blocks specified by the BLKWR command is reached or when all available blocks are used for recording, recording is finished. The end of recording can be verified by the RPM bit of the status register.

(5) To stop recording in the middle, input the STOP command. The contents of the block counter and the contents of the address counter at this moment are automatically stored in the channel index area as the stop block and the stop address, respectively.

In this case, make sure that recording is finished by examining the RPM bit before inputting the next command.

(6) To continue recording, specify the record/playback conditions to be modified by the corresponding commands and perform the steps (3)–(5).

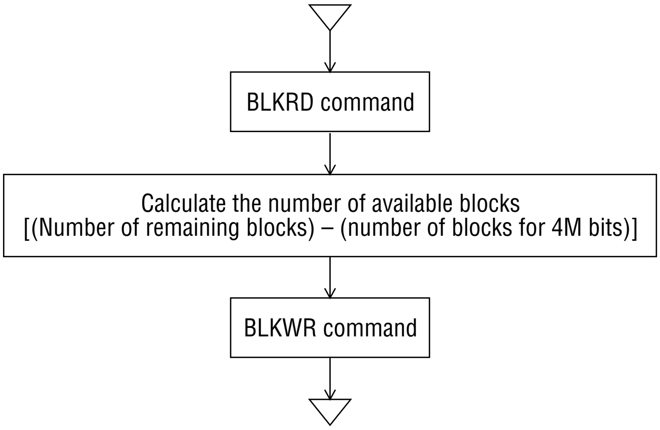
Flow chart of flex recording in the record/playback mode


CHAN command
Specify ch00.
DEL command
Delete all phrases.
VDS command
ADPCM bit length (BIT)
Voice triggered starting (VD0, VD1)
SAMP command
Set the command mode to mode 0 (MOD0 =0, MOD1 = 0).
Specify the sampling frequency (SA0, SA1).
CHAN command
Select one of 63 phrases (CA0 - CA5).
BLKWR command
Set the phrase recording time (BL0 - BL7).
REC command
Set the recording mode.
START command
Start of recording
No
RPM = 1?
Yes
Verify the start of recording.
Input record/playback conditions to be modified by the corresponding commands.
RPM = 0?
Yes
Verify the end of recording.
No
No
Stop recording?
Yes
STOP command
Stop of recording
No
RPM = 0?
Yes
Verify the end of recording.
Yes
Continue recording?
No

2.2 When 4M-bit serial register is used

This IC's memory capacity is divided into 256 blocks for address management. This allows the connection of an 8M-bit serial register only. When connecting a 4M-bit serial register, set pins RSEL1 and RSEL2 as if only an 8M-bit serial register were connected. Then, for actual usage, the 8M-bit serial register is replaced by a 4M-bit serial register. Replacement by the 4M-bit serial register results in the occurrence of an address area prohibited from being used. Thus, the CPU must control the address area so that it is not accessed.

The recording procedure is almost the same as for using only an 8M-bit serial register. Before recording, however, the number of available blocks must be determined, and a number of blocks that does not exceed that value must be set each time by the BLKWR command. The following gives the procedure for this setting.


BLKRD command
Calculate the number of available blocks [(Number of remaining blocks) – (number of blocks for 4M bits)]
BLKWR command

Read the number of remaining blocks.

Calculated by the CPU.

Set a value not more than the number of available blocks as the number of phrase recording blocks.

The following example provides the number of blocks available when one 4M-bit serial register is connected and the erasure of all phrases is followed by the first recording.

$$\begin{aligned}
\text{(Number of available blocks)} &= \text{(number of remaining blocks)} - \text{(number of blocks for 4M bits)} \\
&= \text{(number of remaining blocks)} - \left(\frac{\text{4M bits}}{\text{memory capacity for one block}}\right) \\
&= 254 - \frac{\text{4M bits}}{\text{32K bits}} \\
&= 254 - 128 \\
&= 126\ \text{(7Eh)}
\end{aligned}$$

The following table provides the memory configurations available when a 4M-bit serial register is used for flex record/playback.

RSEL2		L	L	H	H
RSEL1		L	H	L	H
Serial register and corresponding $\overline{\text{CS}}$ signal	$\overline{\text{CS1}}$	4Mbit	8Mbit	8Mbit	8Mbit
	$\overline{\text{CS2}}$	—	4Mbit	8Mbit	8Mbit
	$\overline{\text{CS3}}$	—	—	4Mbit	8Mbit
	$\overline{\text{CS4}}$	—	—	—	4Mbit
Total memory capacity		4Mbit × 1	12Mbit × 2	20Mbit × 3	28Mbit × 4
Memory capacity per block		32Kbit	64Kbit	128Kbit	128Kbit
Number of blocks for 4M bits		128 (80h)	64 (40h)	32 (20h)	32 (20h)
Initially available block (when only an 8M-bit serial register is used)		126 (7Eh) [254 (FEh)]	191 (BFh) [255 (FFh)]	159 (9Fh) [191 (BFh)]	223 (DFh) [255 (FFh)]

3. Playback method in the flex record/playback mode

(1) Input the record/playback conditions by the corresponding commands as follows.

VDS command: Specify the ADPCM bit length (BIT)
The voice triggered starting (VD0, VD1) is invalid for the playback operation.
SAMP command: Set the command mode to mode 0 (MOD0 = 0, MOD1= 0) and specify the sampling frequency (SA0, SA1).
CHAN command: Select one of 63 phrases ch01–ch3F (CA0–CA5).
LEV command: Specify the playback output level (LV0, LV1).
PLAY command: Set to the playback mode.

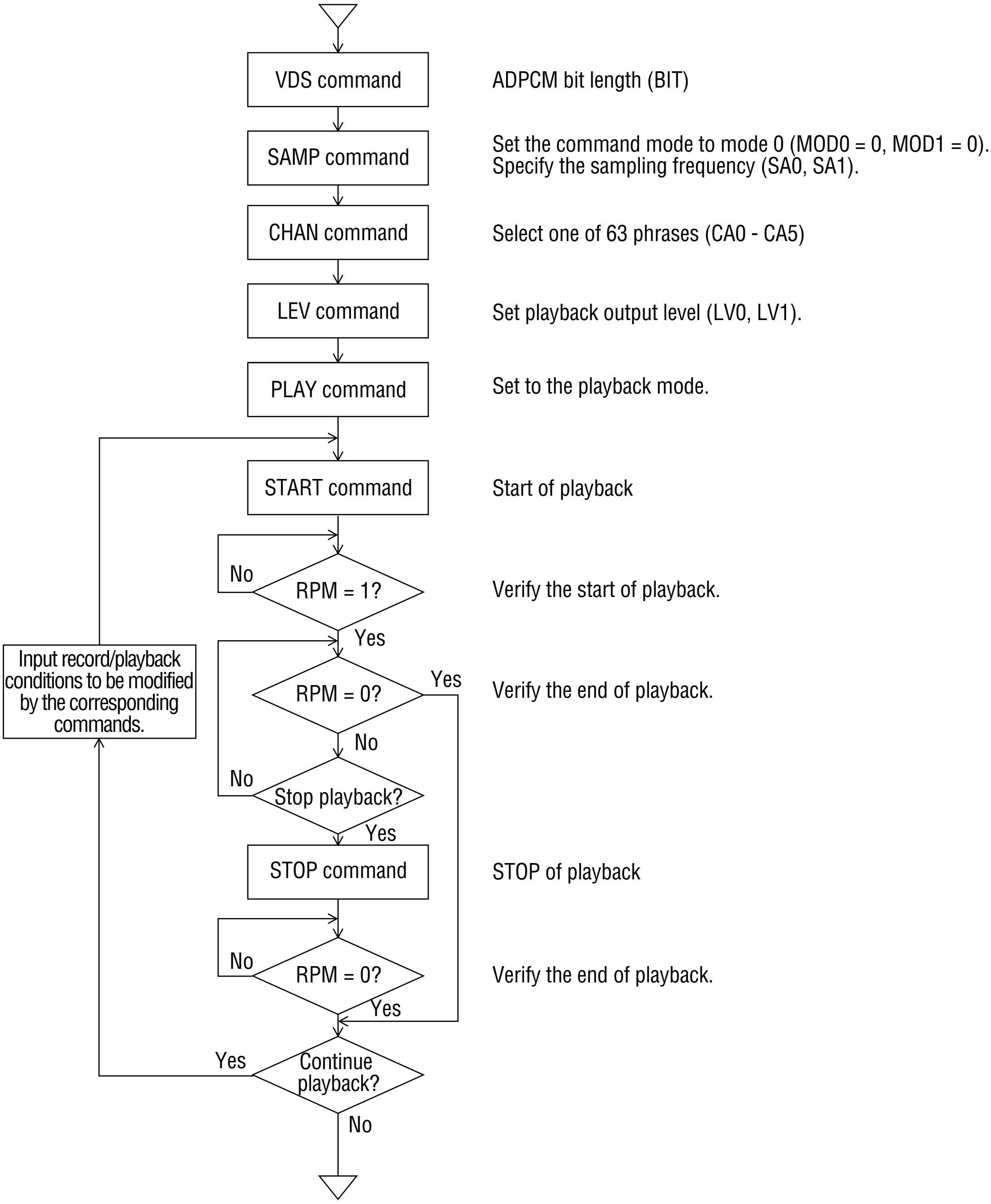
(2) Input the START command to start the playback. The MSM6688/6688L fetches the contents of the block table and the stop address of the specified phrase from the channel index area and starts the playback operation.

(3) When the contents of the address counter coincide with the contents of the stop address register, playback is finished. The end of playback is verified by the RPM bit of the status register.

(4) To stop playback in the middle, input the STOP command. In this case, make sure that playback is finished by examining the RPM bit before inputting the next command.

(5) To continue playback, specify the record/playback conditions to be modified by the corresponding commands and perform steps (2)–(4).

Flow chart of playback in the flex record/playback mode


VDS command
ADPCM bit length (BIT)
SAMP command
Set the command mode to mode 0 (MOD0 = 0, MOD1 = 0).
Specify the sampling frequency (SA0, SA1).
CHAN command
Select one of 63 phrases (CA0 - CA5)
LEV command
Set playback output level (LV0, LV1).
PLAY command
Set to the playback mode.
START command
Start of playback
No
RPM = 1?
Verify the start of playback.
Yes
Input record/playback conditions to be modified by the corresponding commands.
RPM = 0?
Yes
Verify the end of playback.
No
No
Stop playback?
Yes
STOP command
STOP of playback
No
RPM = 0?
Verify the end of playback.
Yes
Yes
Continue playback?
No

This flow chart can apply to the playback operation in the direct record/playback mode, excluding that the command mode is set to mode 2 by the SAMP command and one of 64 phrases (ch00–ch3F) can be selected by the CHAN command in the direct record/playback mode.

Direct Record/Playback Method

1. Recording method in the direct record/playback mode

(1) Input the record/playback conditions by the corresponding commands as follows.

VDS command: Specify the ADPCM bit length (BIT) and voice triggered starting (VD0, VD1).
SAMP command: Set the command mode to mode 2 (MOD = 0, MOD = 1) and specify the sampling frequency (SA0, SA1).
CHAN command: Select one of 64 phases ch00–ch3F (CA0–CA5).
ADRWR command: Input the start address and the stop address.
REC command: Set to the recording mode.

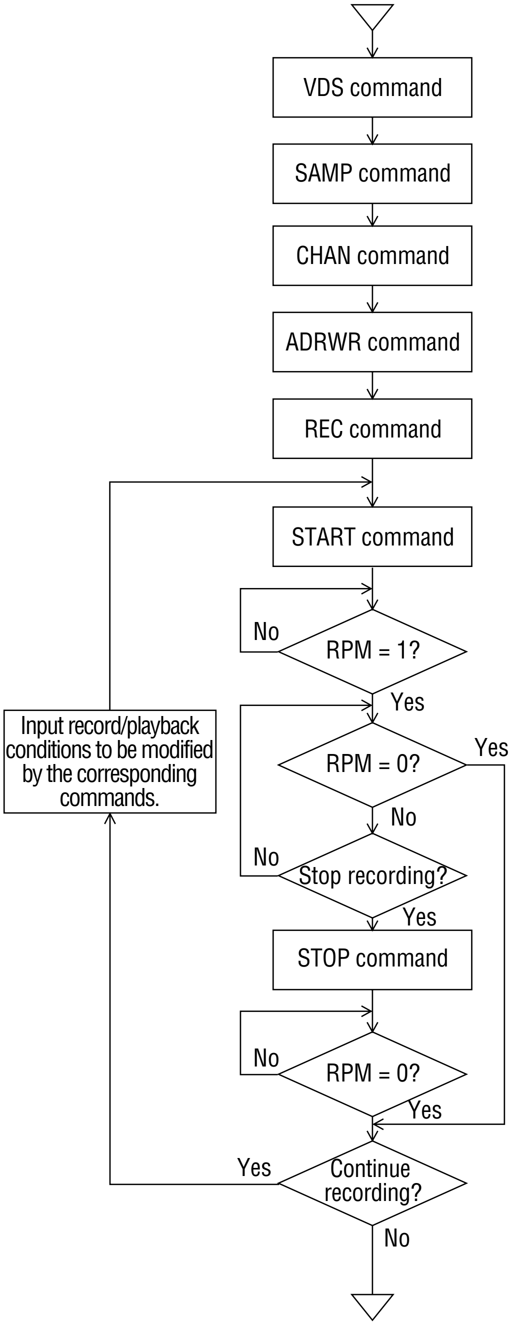
(2) Input the START command to start the recording. The MSM6688/6688L fetches the start address and the stop address of the specified phrase input by the ADRWR from the channel index area and stores them in the address counter and the stop address register, respectively. Then it starts recording.

(3) When the contents of the address counter coincide with the contents of the stop address register, recording is finished. Verity the end of recording by the RPM bit of the status register.

(4) To stop recording in the middle, input the STOP command. In this case, the contents of the address counter is automatically stored in the channel index area as a new stop address. Make sure that recording is finished by examining the RPM bit before inputting the next command.

(5) To continue recording, specify the record/playback conditions to be modified by the corresponding commands and perform steps (2)–(4).

Flow chart of recording in the direct record/playback mode


VDS command
SAMP command
CHAN command
ADRWR command
REC command
START command
RPM = 1?
No
Yes
RPM = 0?
Yes
No
Stop recording?
No
Yes
STOP command
RPM = 0?
No
Yes
Continue recording?
Yes
No
Input record/playback conditions to be modified by the corresponding commands.

ADPCM bit length (BIT)
Voice triggered starting (VD0, VD1)

Set the command mode to mode 2 (MOD0 = 0, MOD1 = 1).
Specify the sampling frequency (SA0, SA1).

Select one of 64 phrases (CA0 - CA5).

Input the start address and stop address.

Set the recording mode.

Start of recording

Verify the start of recording.

Verify the end of recording.

Stop of recording.

Verify the end of recording.

2. Playback method in the direct record/playback mode

The playback method in the direct record/playback mode is similar to that in the flex record/playback mode, excepting that in the direct playback mode, the command mode is specified to mode 2 by the SAMP command and a phrase can be selected from a total of 64 phrases (ch00~ch3F)by the CHAN command.

(1) Input the record/playback conditions by the corresponding commands as follows.

VDS command: Specify the ADPCM bit length (BIT)
The voice triggered starting (VD0, VD1) is invalid for the playback operation.
SAMP command: Set the command mode to mode 2 (MOD = 0, MOD = 1) and specify the sampling frequency (SA0, SA1).
CHAN command: Select one of 64 phrases ch00–ch3F (CA0–CA5).
LEV command: Specify the playback output level (LV0, LV1).
PLAY command: Set the playback mode.

(2) Input the START command to start the playback. The MSM6688/6688L fetches the start address and the stop address of the specified phrase from the channel index area and stores them in the address counter and the stop address register, respectively. Then it starts the playback operation.

(3) When the contents of the address counter coincide with the contents of the stop address register, playback is finished. The end of playback is verified by the RPM bit of the status register.

(4) To stop playback in the middle, input the STOP command. In this case, make sure that playback is finished by examining the RPM bit before inputting the next command.

(5) To continue playback, specify the record/playback conditions to be modified by the corresponding commands and perform steps (2)–(4).

For the flow chart, refer to the flow chart of record/playback in the flex record/playback mode.

ROM Playback by Inputting Address Code

1. Method of inputting commands

(1) Input the record/playback conditions by the corresponding commands as follows.

SAMP command: Set the command mode to mode 1 (MOD0 = 1, MOD1= 0).
The sampling frequency (SA0, SA1) is invalid.
CHAN command: Select one of 255 phrases ch01–chFF (CA0–CA7).
LEV command: Specify the playback output level (LV0, LV1)

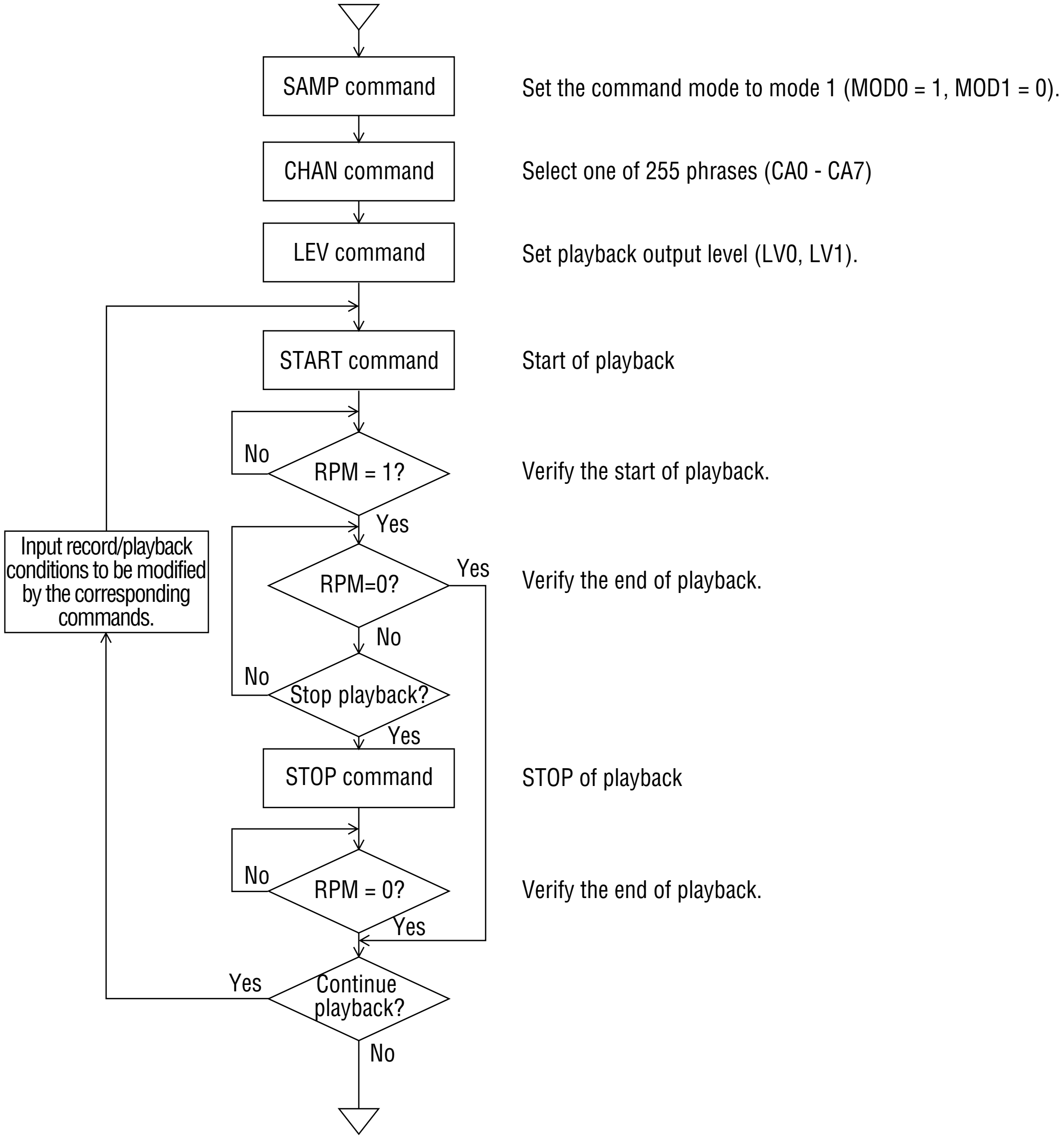
(2) Input the START command to start the playback. The MSM6688/6688L fetches the data of the start address, stop address, sampling frequency, and ADPCM bit length of the specified phrase from the channel index area of the serial voice ROMs and starts the playback operation.

(3) When the contents of the address counter coincide with the contents of the stop address register, playback is finished. The end of playback is verified by the RPM bit of the status register.

(4) To stop playback in the middle, input the STOP command. In this case, make sure that playback is finished by examining the RPM bit before inputting the next command.

(5) To continue playback, specify the record/playback conditions to be modified by the corresponding commands and perform steps (2)–(4).

Flow chart of ROM playback by Input of Address Code


SAMP command
Set the command mode to mode 1 (MOD0 = 1, MOD1 = 0).
CHAN command
Select one of 255 phrases (CA0 - CA7)
LEV command
Set playback output level (LV0, LV1).
START command
Start of playback
No
RPM = 1?
Verify the start of playback.
Yes
Input record/playback conditions to be modified by the corresponding commands.
RPM=0?
Yes
Verify the end of playback.
No
No
Stop playback?
Yes
STOP command
STOP of playback
No
RPM = 0?
Verify the end of playback.
Yes
Yes
Continue playback?
No

2. Continuous ROM playback

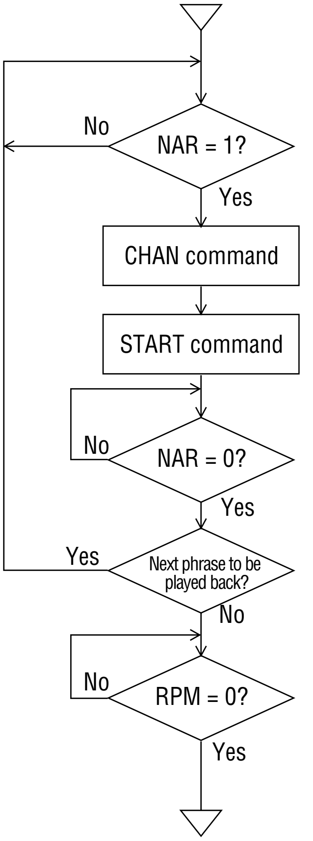
The procedure for playback of different phrases such as the time signal continuously is described below. The command inputting procedure for continuous ROM playback is basically equal to that for a single phrase. In this case, during playback of a phrase, the next phrase to be played back can be specified by the NAR bit of the status register. Continuous playback can also be performed by verifying the end of playback of each phrase using the RPM, instead of use of the NAR bit. To make continuous playback using NAR bit perform the following procedure.

(1) Specify a phrase by the CHAN command and input the START command to start playback. When the START command is accepted, the NAR bit of the status register goes to 0.

(2) When the NAR bit is changed from 0 to 1 to indicate that the next phrase can be specified and inputted, specify the next phrase to be played back by the CHAN command and input the START command. After the START command is accepted, the NAR bit goes to 0 again.

(3) In the same way as mentioned above, repeat the designation of a phrase and input of the START command verifying the state of the NAR bit.

Flow chart of continuous ROM playback


NAR = 1?
No
Yes
CHAN command
START command
No
NAR = 0?
Yes
Yes
Next phrase to be played back?
No
No
RPM = 0?
Yes

Verify whether a phrase can be specified or not.

Specify one of 255 phrases (CA0 - CA7).

The specified phrase is accepted.

Verify whether playback of the specified phrase is accepted or not.

Verify the end playback.

Direct ROM Playback Method

A technique for ROM to be accessed directly is used when the contents of a serial voice ROM prepared for the MSM6388/6588/6588L are played back.

The channel index area is not provided at the header area of serial voice ROMs. Therefore, it is required to prepare a ROM in the microcontroller or an external ROM to store the start and stop addresses, sampling frequency, and ADPCM bit length of each phrase.

The start address and stop address of each phrase consists of 32 bits. These addresses are indicated in the voice address corresponding list of the serial voice ROM.

For example, the addresses to provide the "Message + Cattle Voice (English)" are as shown in the following table.

	Voice words	Start X address STX11 - STX0	Stop X address SPX11 - SPX0	Stop Y address SPY7 - SPY0	Sampling frequency fs	ADPCM bit length
No. 1	Message + Cattle Voice (English)	000h	010h	5Dh	6.4kHz	4bit

Before starting playback, the address data must be transferred to the channel index area of the status register using the ADRWR command. In this case, a phrase that is not used for record/playback must be specified for this direct ROM playback using the CHAN command. When recording a phrase in the flex record/playback mode, ch00 is inhibited to specify. Normally, ch3F address is used as the phrase dedicated for direct ROM playback.

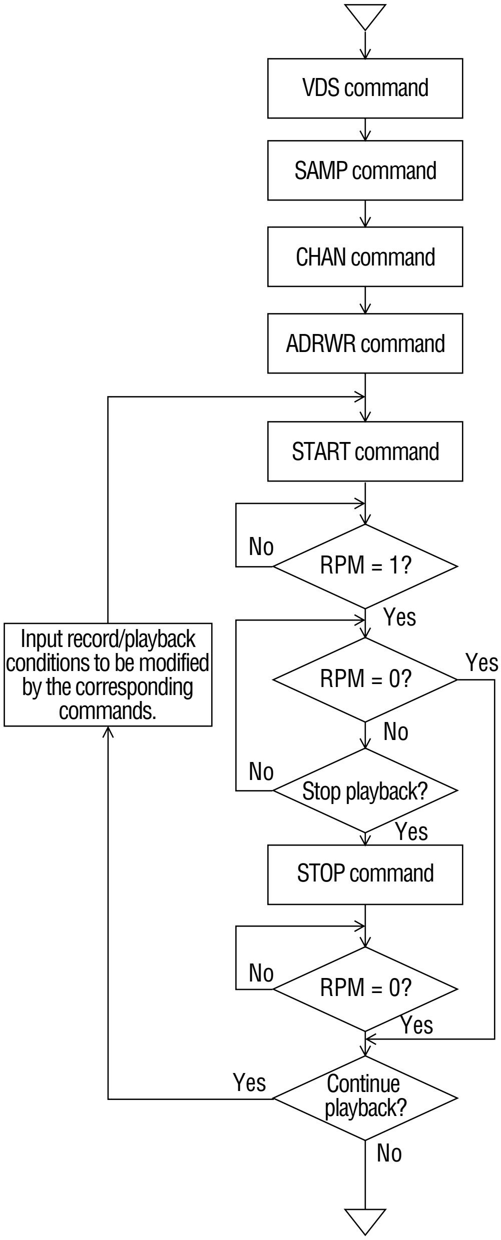
(1) Input the record/playback conditions by the corresponding commands as follows.

VDS command:	Specify the ADPCM bit length (BIT). The voice triggered starting (VD0, VD1) is invalid for the playback operation.
SAMP command:	Set the command mode to mode 3 (MOD1 = 1, MOD0 = 1) and specify the sampling frequency (SA0, SA1).
CHAN command:	Select one of 64 phrases ch00–ch3F (CA0–CA5). Normally ch3F is used for direct ROM playback
ADRWR command:	Specify the start and stop addresses.

(2) Input the START command to start the ROM playback. The MSM6688/6688L fetches the start address and the stop address of the specified phrase from the channel index area of the serial registers. Then it starts the playback operation.

(3) To stop playback in the middle, input the STOP command. In this case, make sure that playback is finished by examining the RPM bit.

Flow chart of direct ROM playback


VDS command
SAMP command
CHAN command
ADRWR command
START command
No
RPM = 1?
Yes
Input record/playback conditions to be modified by the corresponding commands.
RPM = 0?
Yes
No
No
Stop playback?
Yes
STOP command
No
RPM = 0?
Yes
Yes
Continue playback?
No

ADPCM bit length (BIT)

Set the command mode to mode 3 (MOD0 = 1, MOD1 = 1).
Specify the sampling frequency (SA0, SA1).

Select one of 64 phrases (CA0 - CA5). Normally, specify ch3F.

Input the start address and stop address.

Start of playback

Verify the start of playback.

Verify the end of playback.

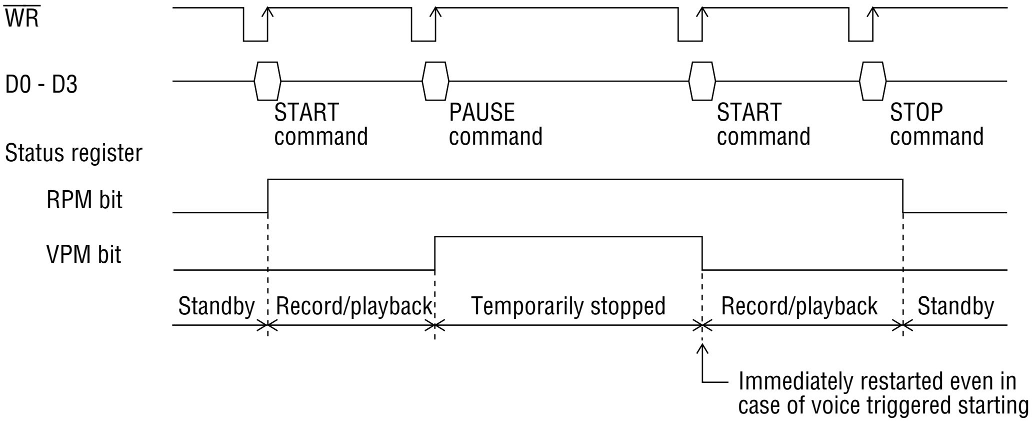
Stop of playback.

Verify the end of playback.

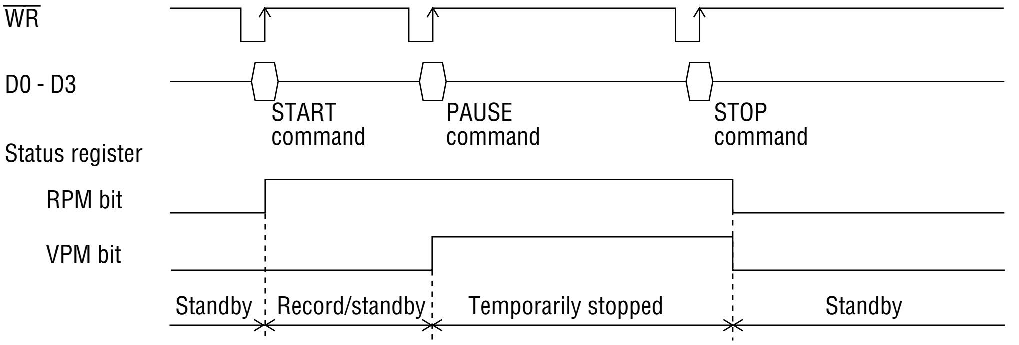
Stopping Record/Playback Temporarily (by the PAUSE Command)

The record/playback operation in progress can be stopped temporarily by inputting the PAUSE command. The record/playback operation stopped using the PAUSE command can be restarted by inputting the START command. During temporary stop state, the VPM bit of the status register is 1 and the RPM bit keeps 1.

If the START command is input to restart the recording operation that is temporarily suspended by the PAUSE command in the voice reiggered starting mode, the recording will be started immediately even in the state of silence. The PAUSE command is invalid during record/playback standby state, temporarily stopped state, and standby state for voice.


WR
D0 - D3
START command
PAUSE command
START command
STOP command
Status register
RPM bit
VPM bit
Standby
Record/playback
Temporarily stopped
Record/playback
Standby
Immediately restarted even in case of voice triggered starting

When the STOP command is input during temporarily stopped state, the record/playback operation is finished and the MSM6688/6688L is placed in the standby state.


WR
D0 - D3
START command
PAUSE command
STOP command
Status register
RPM bit
VPM bit
Standby
Record/standby
Temporarily stopped
Standby

Transferring Data to/from External Memories

1. Method of transferring data to/from external serial registers (by the CHRW command)

The MSM6688/6688L can transfer data to/from the user area in the channel index area of external RAM using the CHRW command. Before starting this data transfer operation, a desired phrase must be specified using the CHAN command. The memory capacity for each phrase is 704 bits (176 nibbles) in the flex record/playback mode and 960 bits (240 nibbles) in the direct record/playback mode. The read/write operation must be performed for the data that does not exceed this memory capacity per phrase.

The contents of the user area for a specified phrase or for all phrases will be cleared to all 0s (0h data) using the CHAN and DEL commands.

The following shows the procedure for inputting the CHRW command.

(1) Set the command mode to mode 0 or mode 1 (MOD1=0) using the SAMP command.

(2) Specify a phrase using the CHAN command.

(3) After inputting the CHAN command, wait for BUSY state duration. The end of the BUSY state duration can also be verified by the BUSY bit of the status register.

(4) To write data, input the REC command and then input the data to be written by applying the $\overline{WR}$ pulse. It is required to wait for the busy state duration between the contiguous $\overline{WR}$ pulses.

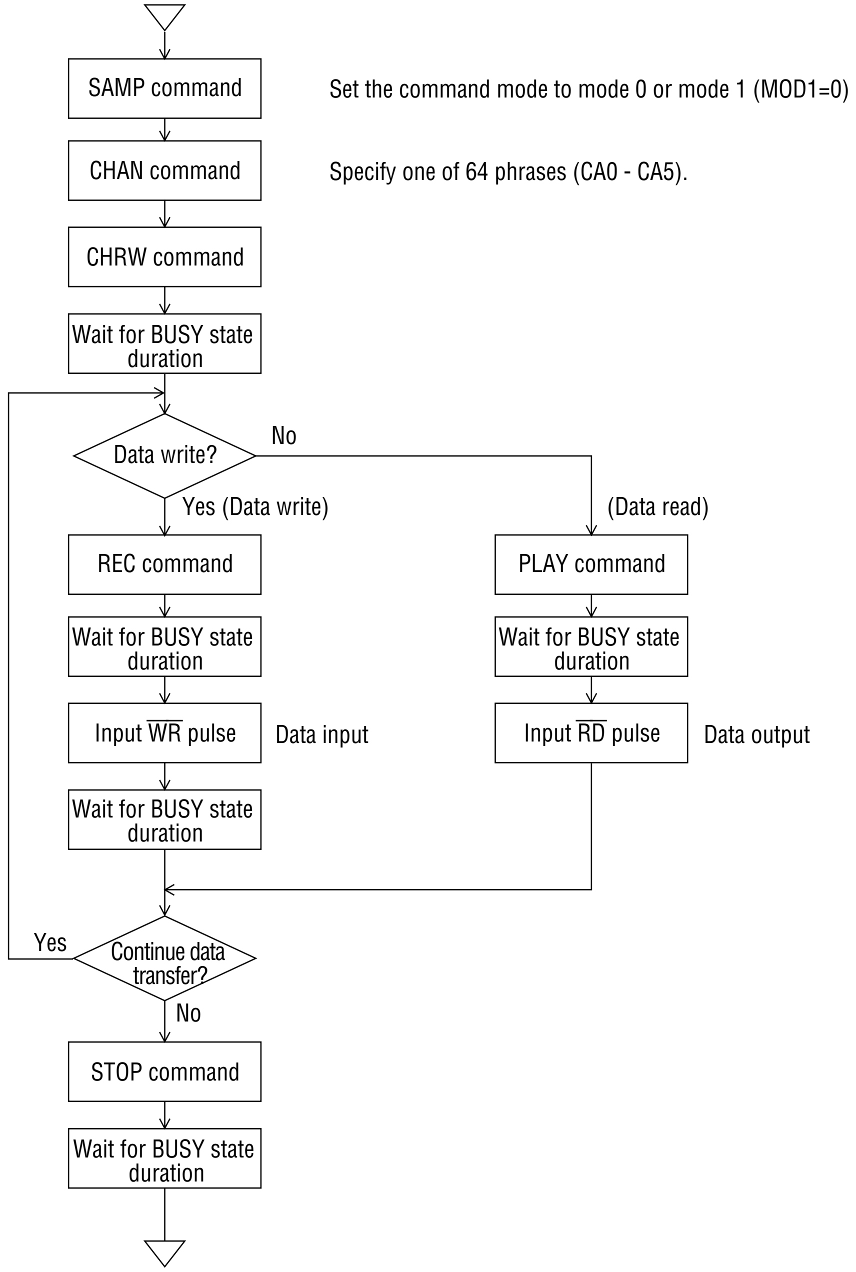
When the data writing operation is performed by inputting a single input of the CHRW command, the state of the BUSY bit of the status register can be verified by inputting the $\overline{RD}$ pulse. When the data read operation is performed with the data write operation, the state of the BUSY bit cannot be verified by inputting the $\overline{RD}$ pulse.

(5) When reading data, wait for the BUSY state duration after inputting the PLAY command and then input the $\overline{RD}$ pulse. With this operation, 4-bit data will be output via the data bus.

(6) To continue the data read or write operation, specify the read or write mode using the PLAY or REC commands.

(7) To stop the data read/write operation, input the STOP command. After waiting for the BUSY state duration, the next command can be input.

Flow chart of data transfer using the CHRW command


SAMP command
Set the command mode to mode 0 or mode 1 (MOD1=0)
CHAN command
Specify one of 64 phrases (CA0 - CA5).
CHRW command
Wait for BUSY state duration
Data write?
No
Yes (Data write)
(Data read)
REC command
Wait for BUSY state duration
Input $\overline{WR}$ pulse
Data input
Wait for BUSY state duration
PLAY command
Wait for BUSY state duration
Input $\overline{RD}$ pulse
Data output
Yes
Continue data transfer?
No
STOP command
Wait for BUSY state duration

2. Method of transferring data to and from external RAM (by the DTRW command)

The data transfer to/from external RAM is performed using the DTRW command. After inputting the DTRW command, specify an address to be accessed for data read/write. The transfer of each 4-bit data is performed from the starting nibble of the specified address. For the address space, refer to Section 1.2 "Address space allocation in the direct record/playback mode" in "Data Configuration of External RAM." The address designation can be made only in the X direction and random address designation cannot be made in the Y direction to select an arbitrary address in the Y direction.

With the input of a single DTRW command, continuous read/write operation can be made in the range of addresses 8Mbit ($\overline{\text{CS1}}$, $\overline{\text{CS2}}$, $\overline{\text{CS3}}$, $\overline{\text{CS4}}$,). When the read/write operation is extended to two or more 8Mbits ($\overline{\text{CS1}}$, $\overline{\text{CS2}}$, $\overline{\text{CS3}}$, $\overline{\text{CS4}}$,), it is necessary to stop temporarily the read/write operation each time the operation is finished for one serial register, and set the address for another serial register using the DTRW command.

(1) Set the common mode to mode 2 (MOD0 = 0, MOD1 = 1)

(2) Input the DTRW command

(3) Specify the X address in a serial register by inputting the $\overline{\text{WR}}$ pulse five times. Wait for the BUSY state duration. The BUSY state can be verified by examining the state of the BUSY bit of the status register. The 2nd nibble of the DTRW command is a dummy nibble. Always input 0h data into the 2nd nibble.

(4) For data writing, input the REC command and input the data to be written by inputting the $\overline{\text{WR}}$ pulse. Wait for the BUSY state duration between the contiguous $\overline{\text{WR}}$ pulses.

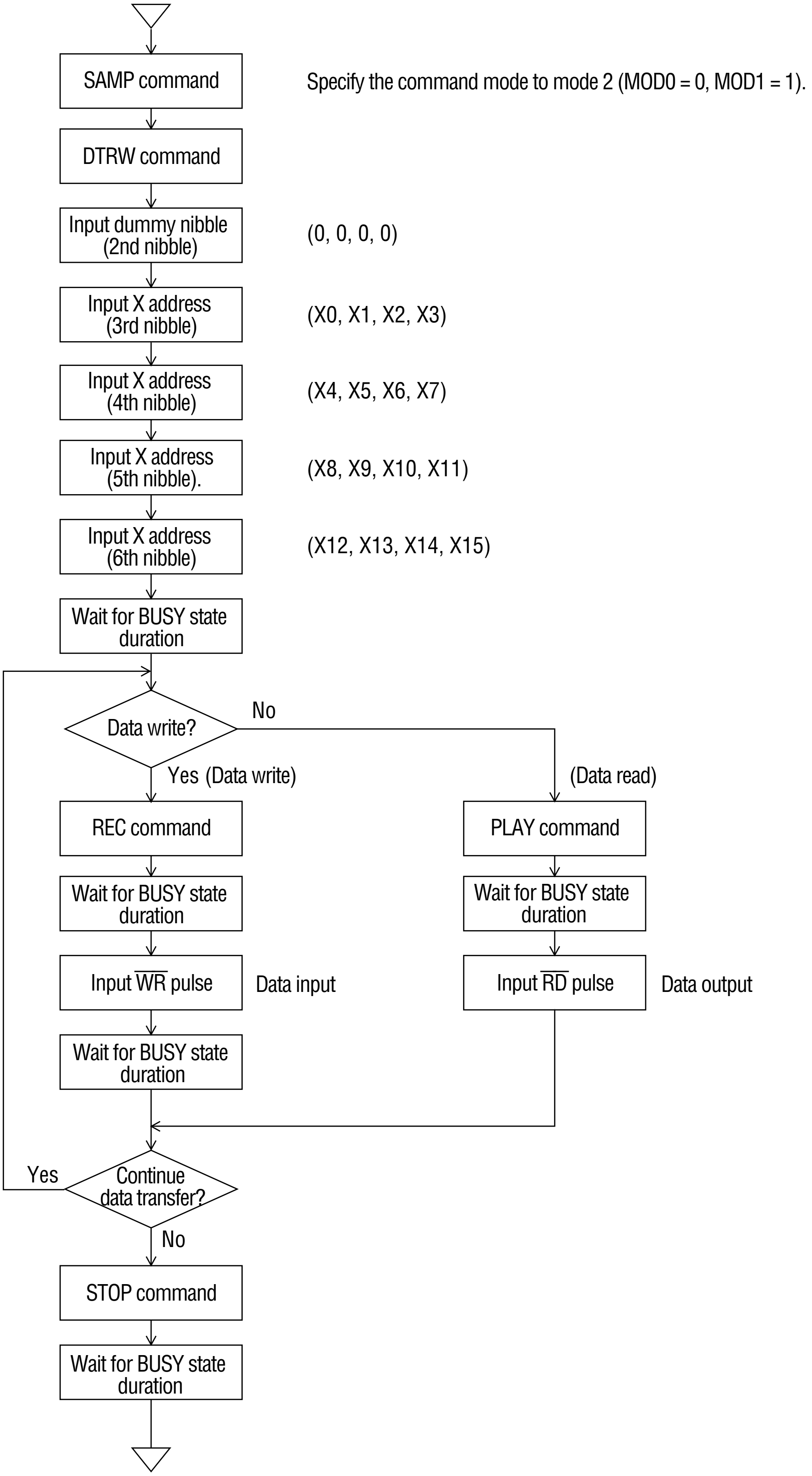
To make the data write operation by a single input of the DTRW command, the state of the BUSY bit can be verified by inputting the $\overline{\text{RD}}$ pulse. When data write and data read operations are performed jointly, the state at the BUSY bit cannot be verified using the $\overline{\text{RD}}$ pulse.

(5) To read data, input the PLAY command and then input the $\overline{\text{RD}}$ pulse after waiting for the BUSY state duration. With this operation, 4-bit data will be output via the data bus.

(6) To continue data read/write operation, specify the read or write mode using the PLAY or REC command and make data transfer operation.

(7) To finish the data read/write operation, input the STOP command. After waiting for the BUSY state duration, the next command can be input.

Flow chart of data transfer using the DTRW command


SAMP command
Specify the command mode to mode 2 (MOD0 = 0, MOD1 = 1).
DTRW command
Input dummy nibble (2nd nibble)
(0, 0, 0, 0)
Input X address (3rd nibble)
(X0, X1, X2, X3)
Input X address (4th nibble)
(X4, X5, X6, X7)
Input X address (5th nibble).
(X8, X9, X10, X11)
Input X address (6th nibble)
(X12, X13, X14, X15)
Wait for BUSY state duration
Data write?
No
Yes (Data write)
(Data read)
REC command
PLAY command
Wait for BUSY state duration
Wait for BUSY state duration
Input WR pulse
Data input
Input RD pulse
Data output
Wait for BUSY state duration
Yes
Continue data transfer?
No
STOP command
Wait for BUSY state duration

3. Method of reading data from external serial voice ROMs (by the DTRD command)

The data from external serial voice ROMs can be read using the DTRD command. After inputting the DTRD command, specify the address to be read. The data is read in groups of 4 bits from the specified address. For the address space, refer to "Data Configuration of External Serial Voice ROMs." The data can be addressed on a 64-bit basis.

With the input of a single DTRD command, continuous read/write operation can be made in the range of addresses assigned to the same serial voice ROM. When the read/write operation is extended to two or more serial voice ROMs, it is necessary to stop temporarily the read/write operation each time the operation is finished for the serial voice ROM, and set the address for another serial voice ROM using the DTRD command.

The following shows the procedure for inputting the DTRD command.

(1) Set the command mode to mode 3 (MOD0 = 1, MOD1 = 1).

(2) Input the DTRD command.

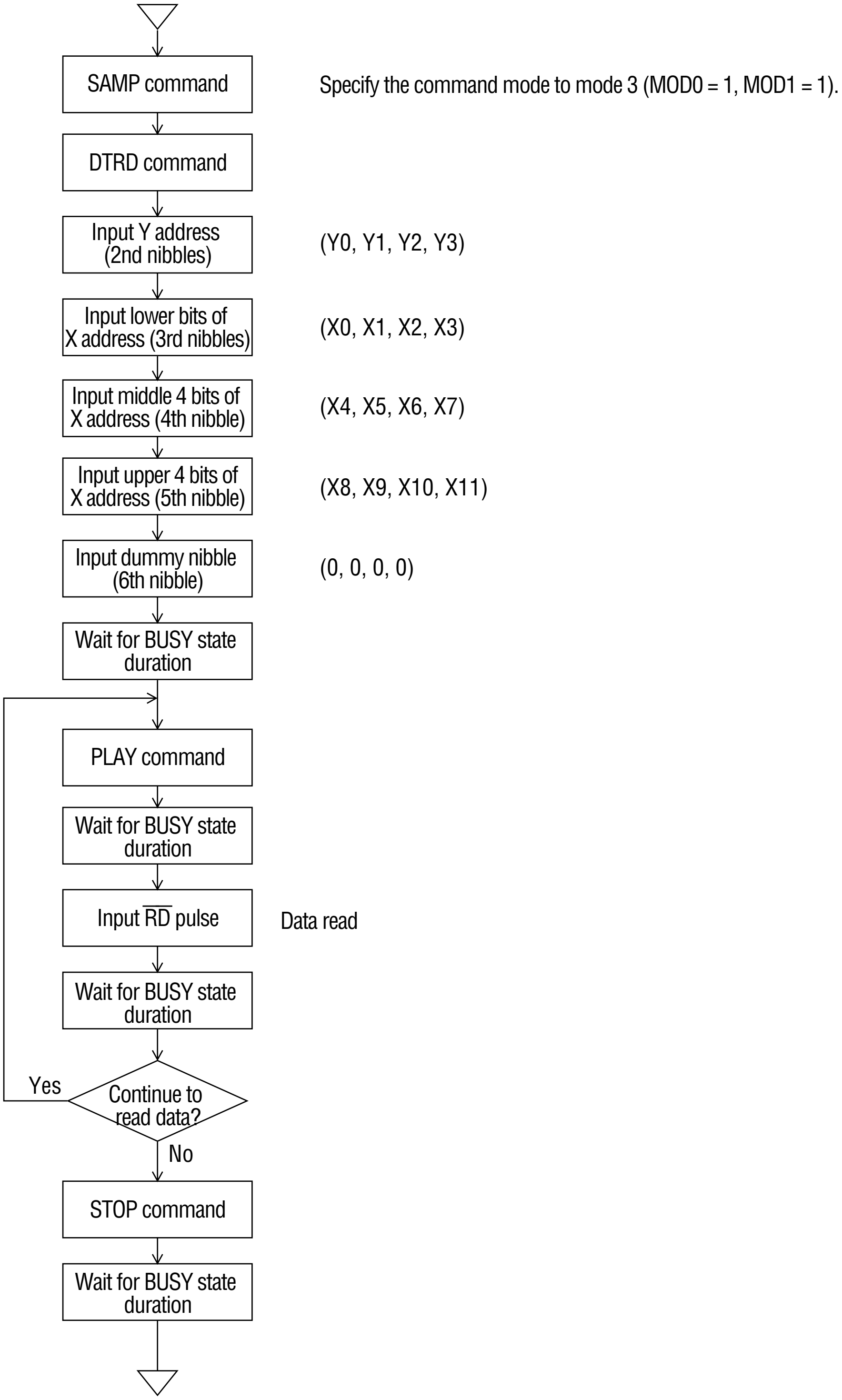
(3) Specify the X address and Y address of the serial voice ROM by inputting the $\overline{\text{WR}}$ pulse five times. Then, wait for the BUSY state duration. The 6th nibble is a dummy nibble. Always input 0h data into this 6th nibble.

(4) Input the PLAY command and wait for the BUSY state duration. Then, input the $\overline{\text{RD}}$ pulse, so that 4-bit data will be output via the data bus.

(5) To continue data read operation, perform the data read operation inputting the PLAY command and $\overline{\text{RD}}$ pulse in the same way as mentioned above.

(6) To finish the data read operation input the STOP command. After waiting for the BUSY state duration, the next command can be input.

Flow chart of data read using the DTRD command


SAMP command
Specify the command mode to mode 3 (MOD0 = 1, MOD1 = 1).
DTRD command
Input Y address (2nd nibbles)
(Y0, Y1, Y2, Y3)
Input lower bits of X address (3rd nibbles)
(X0, X1, X2, X3)
Input middle 4 bits of X address (4th nibble)
(X4, X5, X6, X7)
Input upper 4 bits of X address (5th nibble)
(X8, X9, X10, X11)
Input dummy nibble (6th nibble)
(0, 0, 0, 0)
Wait for BUSY state duration
PLAY command
Wait for BUSY state duration
Input $\overline{RD}$ pulse
Data read
Wait for BUSY state duration
Continue to read data?
Yes
No
STOP command
Wait for BUSY state duration

Record/Playback by Inputting/Outputting Voice Data via Data Bus

When SRAMs (static RAMs) or other hardware memory products are used to store voice data, the record/playback operation will be performed by using the EXT command. In the case of the record/playback using the EXT command, voice data is directly input or output via the data bus in synchronization with the sampling frequency. In this record/playback mode, the address control and the control of external RAM and serial voice ROMs are not performed. Therefore, the microcontroller performs the recording time control and address control. In this mode, temporary stop of record/playback operation by the PAUSE command and the voice triggered starting cannot be performed.

1. Method of recording using the EXT command

(1) Input the record/playback conditions using the corresponding commands as shown below.

VDS command: Set the ADPCM bit length (BIT).
Specify the disabled state of voice triggered starting (VD0 = 0, VD1 = 0)
SAMP command: Specify the sampling frequency (SA0, SA1)
The command mode (MOD0, MOD1) is invalid.
REC command: Set to the recording mode

(2) Input the EXT command to start the recording. The sampling frequency clock is output via the MON pin.

(3) When the MON pin goes high, input the $\overline{\text{RD}}$ pulse to fetch the ADPCM data from the external memory via the data bus. At that time, input the $\overline{\text{RD}}$ pulse to satisfy time t_{ERD} from rise of MON to rise of the $\overline{\text{RD}}$ pulse. In the case of 3-bit ADPCM, the upper 3 bits (D3–D1 pins) are valid and the lower 1 bit (D0 pins) is invalid.

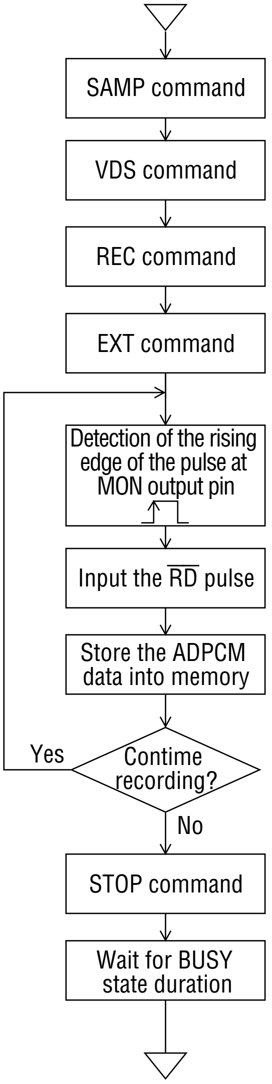
(4) Store the ADPCM data into the external memory such as SRAMs.

(5) Repeat steps (3) and (4) to continue the recording operation.

(6) Input the STOP command to stop the recording operation. Until the STOP command is input, the recording operation will be continued without the limit for the recording time.
When the MON pin becomes "H" level, input the $\overline{\text{RD}}$ pulse to fetch the ADPCM data, and input the STOP command to satisfy time t_{ESP} from rise of MON to input of hte STOP command.

(7) During recording by the EXT command, the contents of the status register cannot be verified by the $\overline{\text{RD}}$ pulse. Therefore, after inputting the STOP command, wait for the BUSY state duration and then input the next command.

Flow chart of recording using the EXT command


SAMP command
VDS command
REC command
EXT command
Detection of the rising edge of the pulse at MON output pin
Input the $\overline{RD}$ pulse
Store the ADPCM data into memory
Contime recording?
Yes
No
STOP command
Wait for BUSY state duration

Specify the sampling frequency (SA0, SA1).

Specify the ADPCM bit length (BIT)

Set to the recording mode

Start the recording by EXT command.

Fetch ADPCM data from memory.

Store the ADPCM data into an external memory such as SRAM.

End of recording by EXT command

2. Method of playback using the EXT command

(1) Input the record/playback conditions using the corresponding commands as shown below.

VDS command:	Set to the ADPCM bit length (BIT) specified for recording. Voice triggered starting becomes invalid.
SAMP command:	Specify the sampling frequency (SA0, SA1) The command mode (MOD0, MOD1) is invalid.
PLAY command:	Set to the playback mode

(2) Input the EXT command to start the playback. The sampling frequency clock is output via the MON pin.

(3) When the MON pin goes high, the ADPCM data is ready to be fetched from an external memory such as an SRAM.

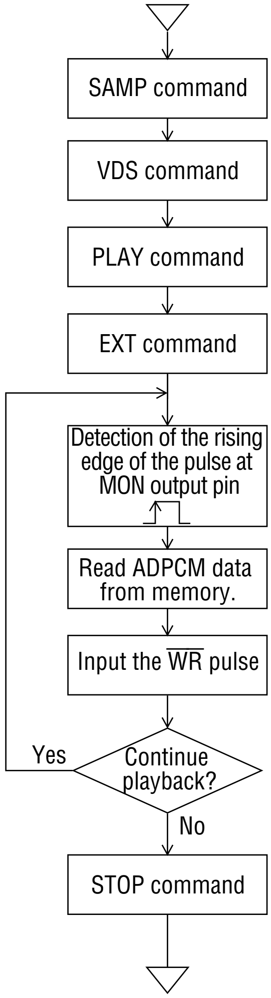
(4) Input the $\overline{WR}$ pulse to fetch the ADPCM data from the external memory via the data bus. At that time, input the $\overline{WR}$ pulse to satisfy time t_{EWR} from rise of MON to rise of the $\overline{WR}$ pulse. In the case of 3-bit ADPCM, the upper 3 bits (D3–D1 pins) are valid and the lower 1 bit (D0 pins) is invalid.

(5) Repeat steps (3) and (4) to continue the playback operation.

(6) Input the STOP command to stop the playback operation.
When the MON pin becomes "H", input the $\overline{WR}$ pulse, input the ADPCM data, and input the STOP command to satisfy time t_{ESP} from rise of MON to input of the STOP command, and interval t_{WE1} between the $\overline{WR}$ pulse and the STOP command pulse.

Note: Input the ADPCM data beginning with the top of a phrase every sampling period sequentially. If the ADPCM data is input beginning with the second or following part of a phrase or with data missing, normal (playback) waveforms cannot be regenerated.

Flow chart of playback using the EXT command


SAMP command
VDS command
PLAY command
EXT command
Detection of the rising edge of the pulse at MON output pin
Read ADPCM data from memory.
Input the $\overline{WR}$ pulse
Continue playback?
Yes
No
STOP command

Specify the sampling frequency (SA0, SA1).

Specify the ADPCM bit length (BIT)

Set to the playback mode

Start the playback by EXT command.

Write the ADPCM data.

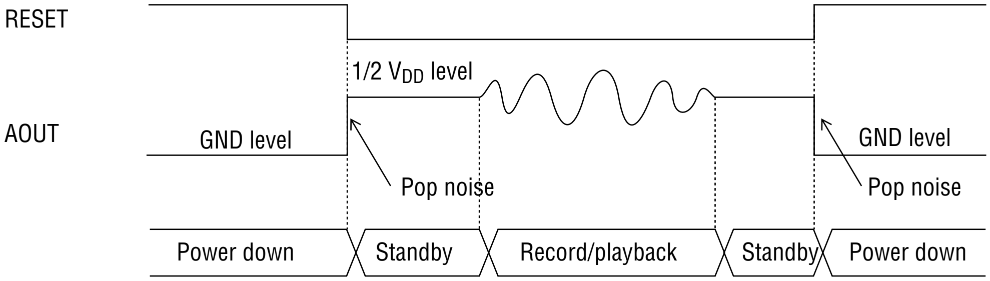
Stop the playback by EXT command.

Suppression of Pop Noise at AOUT Output (by the LEV Command)

The MSM6688/6688L has a on-chip pop noise suppression circuit to prevent pop nose from being generated due to sharp changes of the DC level of the analog output (at the AOUT pin). The enabled or disabled state of this pop noise suppression circuit can be selected using the ACON pin. When the ACON pin is low, this circuit is disabled and when high, this circuit is enabled.

1. When the POP noise suppression circuit is disabled (ACON = low)

When the RESET pin is high, the DC level at the AOUT pin is the ground level, and when the RESET pin is low, the DC level at the AOUT pin is the 1/2 V_{DD} level. Each time the state of the RESET pin is changed, the DC level is changed sharply and pop noise is generated.

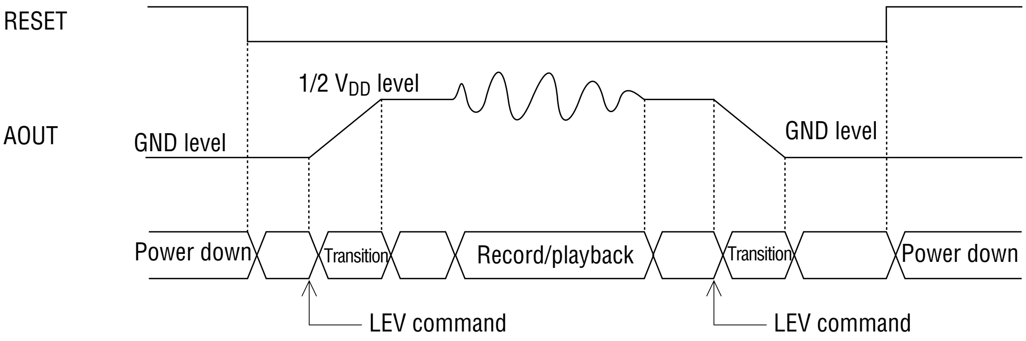

RESET
AOUT
1/2 V_{DD} level
GND level
GND level
Pop noise
Pop noise
Power down
Standby
Record/playback
Standby
Power down

2. When the POP noise suppression circuit is enabled (ACON = high)

The transition of the DC level at the AOUT (analog output) pin is controlled using the LEV command. When the RESET pulse (low) is applied to the RESET pin, the DC level at the AOUT output pin goes to the ground level. If the pop noise suppression circuit is activated using the PN0 and PN1 bits of the 2nd nibble of the LEV command, the DC level at the AOUT output pin will be changed from the ground level to the 1/2 V_{DD} level or from the 1/2 V_{DD} level to the ground level slowly to prevent pop noise from being generated.

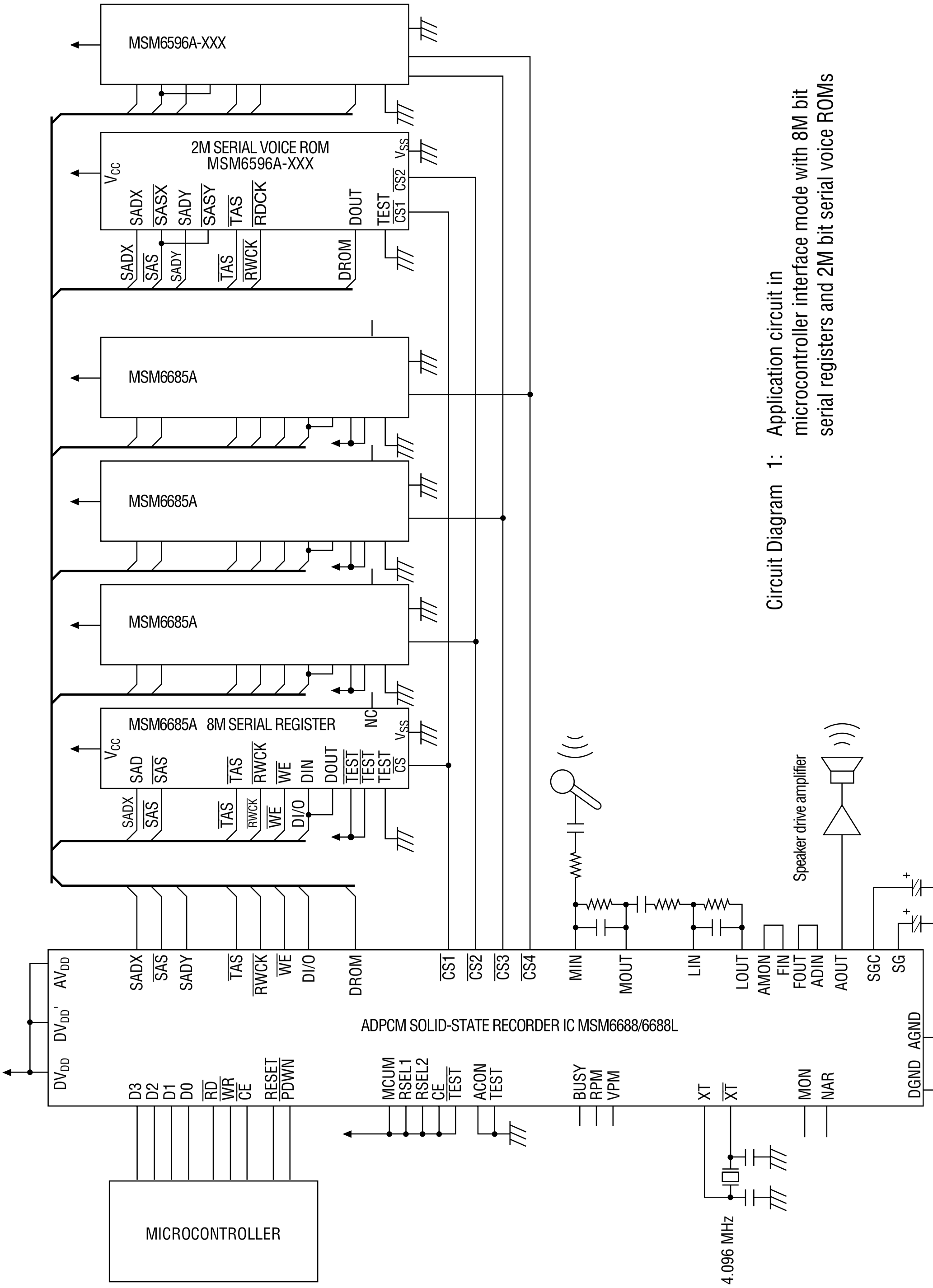
Before starting the record/playback operation, always set the DC level at the AOUT pin to the 1/2 V_{DD} level using the LEV command. When enabling the DC level transition function by the LEV command, first specify the playback mode by the PLAY command and then input the LEV command.

PN1	PN0	DC level transition
0	0	Disabled
0	1	Disabled
1	0	Transition from ground to 1/2 V_{DD}
1	1	Transition from 1/2 V_{DD} to ground


RESET
AOUT
GND level
1/2 V_{DD} level
GND level
Power down
Transition
Record/playback
Transition
Power down
LEV command
LEV command

APPLICATION CIRCUIT

The circuit diagram 1 shows an application circuit example where the MSM6688/6688L is used in the microcontroller interface mode and four 8M bit serial registers and two 2M bit serial voice ROMs are connected.

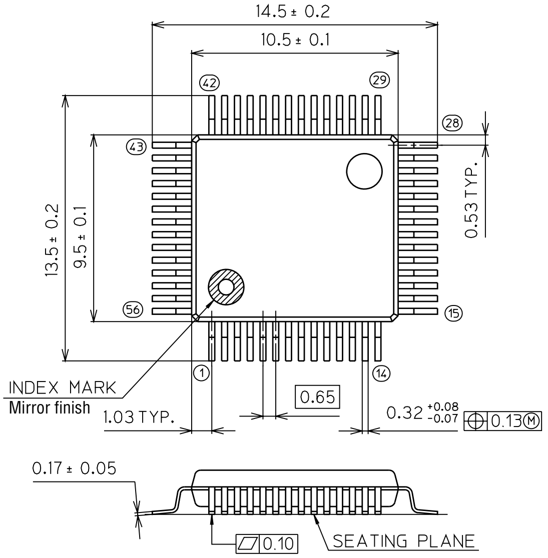

MICROCONTROLLER
ADPCM SOLID-STATE RECORDER IC MSM6688/6688L
DV_DD DV_DD' AV_DD
D3 D2 D1 D0 RD WR CE RESET PDWN
MCUM RSEL1 RSEL2 CE TEST
ACON TEST
BUSY RPM VPM
XT XT
4.096 MHz
MON NAR
DGND AGND
SADX SAS SADY TAS RWCK WE DI/O DROM
CS1 CS2 CS3 CS4
MIN MOUT LIN LOUT AMON FIN FOUT ADIN AOUT SGC SG
Speaker drive amplifier
MSM6685A 8M SERIAL REGISTER
V_CC SAD SAS TAS RWCK WE DIN DOUT TEST TEST TEST CS NC V_SS
SADX SAS TAS RWCK WE DI/O
MSM6685A
MSM6685A
MSM6685A
2M SERIAL VOICE ROM
MSM6596A-XXX
V_CC SADX SASX SADY SASY TAS RDCK DOUT TEST CS1 CS2 V_SS
SADX SAS SADY TAS RWCK DROM
MSM6596A-XXX

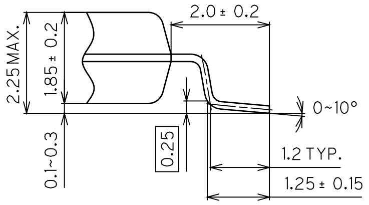
Circuit Diagram 1: Application circuit in microcontroller interface mode with 8M bit serial registers and 2M bit serial voice ROMs

PACKAGE DIMENSIONS

(Unit : mm)

QFP56-P-910-0.65-2K


14.5 ± 0.2
10.5 ± 0.1
42
29
28
43
56
15
1
14
13.5 ± 0.2
9.5 ± 0.1
0.53 TYP.
INDEX MARK
Mirror finish
1.03 TYP.
0.65
0.32 +0.08 -0.07
⌖ 0.13 Ⓜ
0.17 ± 0.05
▱ 0.10
SEATING PLANE


2.0 ± 0.2
2.25 MAX.
1.85 ± 0.2
0~10°
0.1~0.3
0.25
1.2 TYP.
1.25 ± 0.15

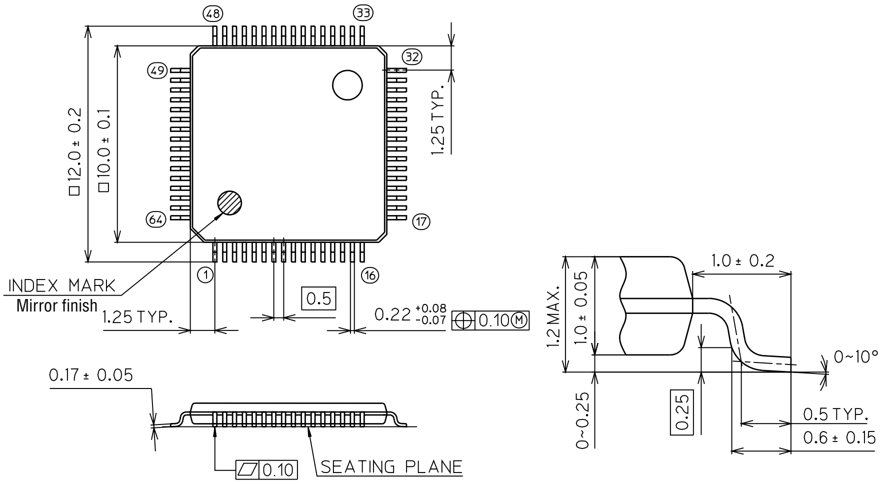
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 µm or more
Package weight (g)	0.43 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, TQFP, LQFP, SOJ, QFJ (PLCC), SHP, and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

TQFP64-P-1010-0.50-K


48
33
32
49
64
17
1
16
□12.0 ± 0.2
□10.0 ± 0.1
1.25 TYP.
INDEX MARK
Mirror finish
1.25 TYP.
0.5
0.22 +0.08 -0.07
0.10 M
0.17 ± 0.05
0.10
SEATING PLANE
1.0 ± 0.2
1.2 MAX.
1.0 ± 0.05
0~10°
0~0.25
0.25
0.5 TYP.
0.6 ± 0.15

Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 µm or more
Package weight (g)	0.26 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, TQFP, LQFP, SOJ, QFJ (PLCC), SHP, and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

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