MJH10012
(See MJ10012)

Complementary Darlington Silicon Power Transistors

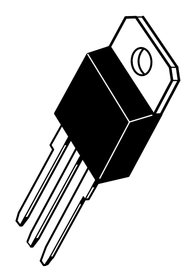
. . . designed for use as general purpose amplifiers, low frequency switching and motor control applications.

- High DC Current Gain @ 10 Adc — h_{FE} = 400 Min (All Types)
- Collector–Emitter Sustaining Voltage
  $V_{CEO(sus)}$ = 150 Vdc (Min) — MJH11018, 17
  = 200 Vdc (Min) — MJH11020, 19
  = 250 Vdc (Min) — MJH11022, 21
- Low Collector–Emitter Saturation Voltage
  $V_{CE(sat)}$ = 1.2 V (Typ) @ I_C = 5.0 A
  = 1.8 V (Typ) @ I_C = 10 A
- Monolithic Construction

PNP
MJH11017*
MJH11019*
MJH11021*
NPN
MJH11018*
MJH11020*
MJH11022*

***Motorola Preferred Device**

15 AMPERE
DARLINGTON
COMPLEMENTARY SILICON
POWER TRANSISTORS
150, 200, 250 VOLTS
150 WATTS



CASE 340D–01

MAXIMUM RATINGS

Rating	Symbol	MJH 11018 11017	MJH 11020 11019	MJH 11022 11021	Unit
Collector–Emitter Voltage	V_{CEO}	150	200	250	Vdc
Collector–Base Voltage	V_{CB}	150	200	250	Vdc
Emitter–Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous — Peak (1)	I_C	15 30			Adc
Base Current	I_B	0.5			Adc
Total Device Dissipation @ T_C = 25°C Derate Above 25°C	P_D	150 1.2			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance. Junction to Case	$R_{\theta JC}$	0.83	°C/W

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

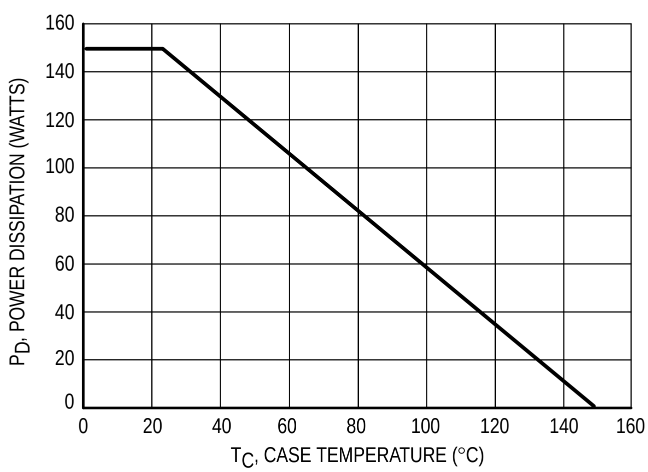


Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

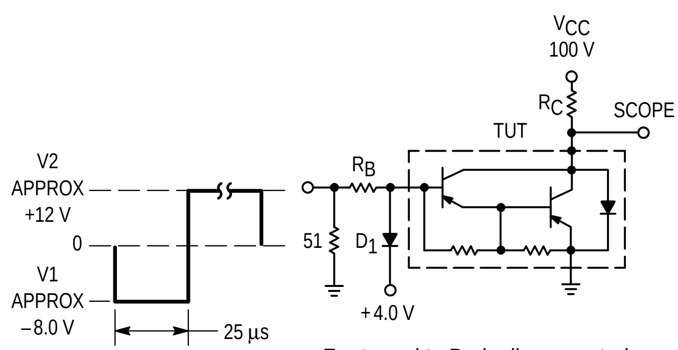
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 0.1 Adc, I_B = 0)	 MJH11017, MJH11018 MJH11019, MJH11020 MJH11021, MJH11022	$V_{CEO(sus)}$	 150 200 250	 — — —	Vdc
Collector Cutoff Current (V_{CE} = 75 Vdc, I_B = 0) (V_{CE} = 100 Vdc, I_B = 0) (V_{CE} = 125 Vdc, I_B = 0)	 MJH11017, MJH11018 MJH11019, MJH11020 MJH11021, MJH11022	I_{CEO}	 — — —	 1.0 1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_J = 150°C)		I_{CEV}	 — —	 0.5 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc I_C = 0)		I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 10 Adc, V_{CE} = 5.0 Vdc) (I_C = 15 Adc, V_{CE} = 5.0 Vdc)		h_{FE}	400 100	15,000 —	—
Collector–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 100 mA) (I_C = 15 Adc, I_B = 150 mA)		$V_{CE(sat)}$	— —	2.5 4.0	Vdc
Base–Emitter On Voltage (I_C = 10 A, V_{CE} = 5.0 Vdc)		$V_{BE(on)}$	—	2.8	Vdc
Base–Emitter Saturation Voltage (I_C = 15 Adc, I_B = 150 mA)		$V_{BE(sat)}$	—	3.8	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain Bandwidth Product (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		f_T	3.0	—	—
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	MJH11018, MJH11020, MJH11022 MJH11017, MJH11019, MJH11021	C_{ob}	— —	400 600	pF
Small–Signal Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)		h_{fe}	75	—	—

SWITCHING CHARACTERISTICS

Characteristic		Symbol	Typical		Unit
			NPN	PNP	
Delay Time	(V_{CC} = 100 V, I_C = 10 A, I_B = 100 mA $V_{BE(off)}$ = 5.0 V) (See Figure 2)	t_d	150	75	ns
Rise Time		t_r	1.2	0.5	µs
Storage Time		t_s	4.4	2.7	µs
Fall Time		t_f	2.5	2.5	µs

(1) Pulse Test: Pulse Width = 300 µs, Duty Cycle ≤ 2.0%.

R_B & R_C varied to obtain desired current levels
D_1, must be fast recovery types, e.g.:
1N5825 used above $I_B \approx$ 100 mA
MSD6100 used below $I_B \approx$ 100 mA



For t_d and t_r, D_1 is disconnected and V2 = 0

t_r, $t_f \leq$ 10 ns
Duty Cycle = 1.0%

For NPN test circuit, reverse diode and voltage polarities.

Figure 2. Switching Times Test Circuit

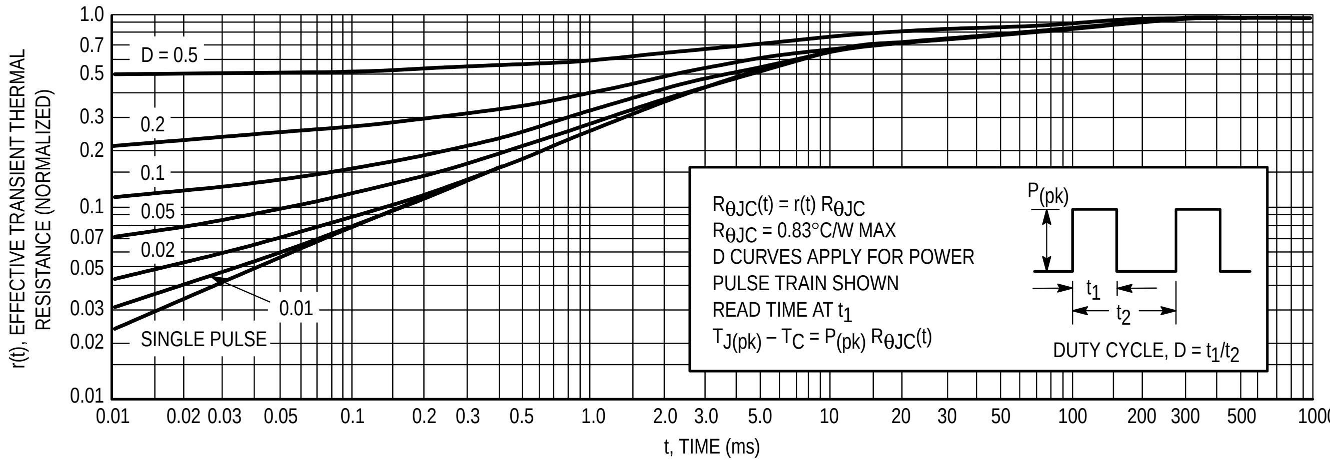


Figure 3. Thermal Response

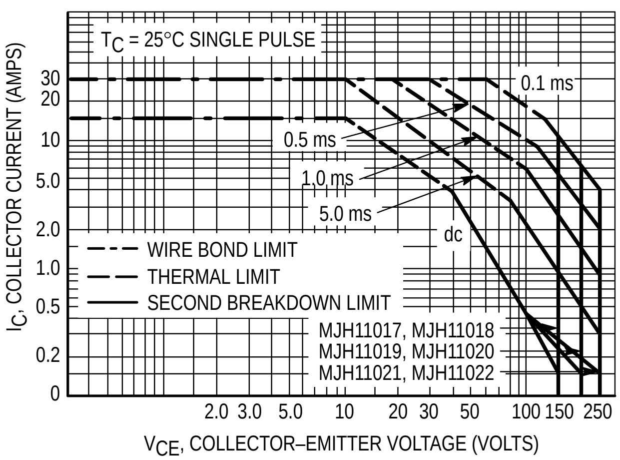


Figure 4. Maximum Rated Forward Bias Safe Operating Area (FBSOA)

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 4 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 3. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

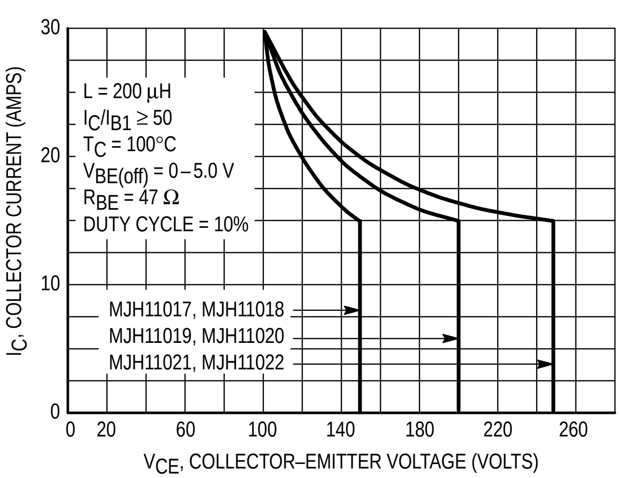


Figure 5. Maximum Rated Reverse Bias Safe Operating Area (RBSOA)

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage–current conditions during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 5 gives RBSOA characteristics.

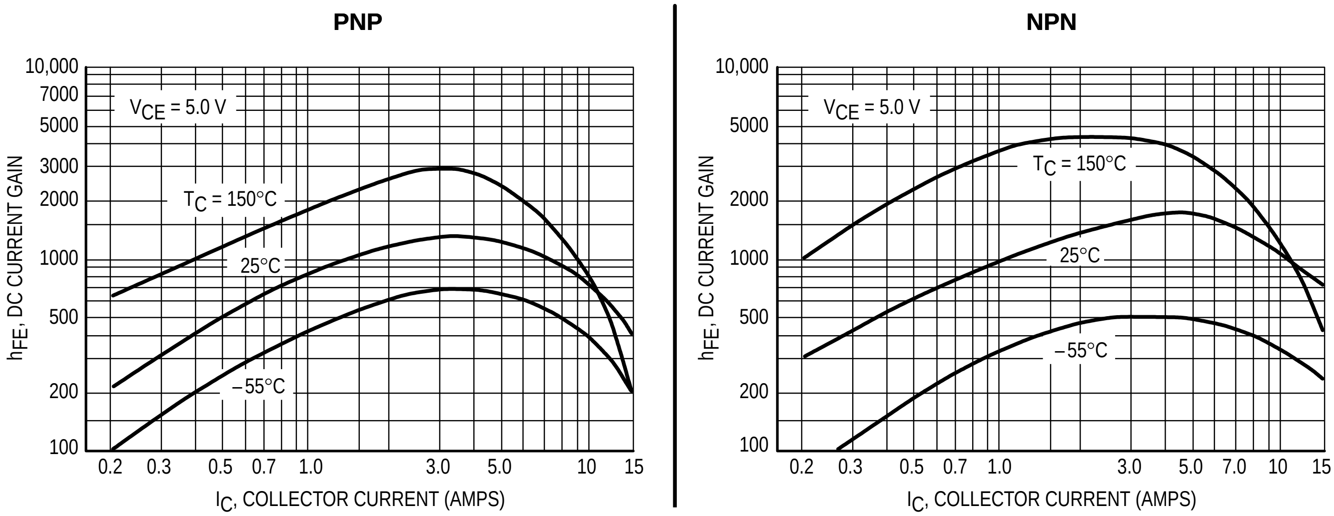


Figure 6. DC Current Gain

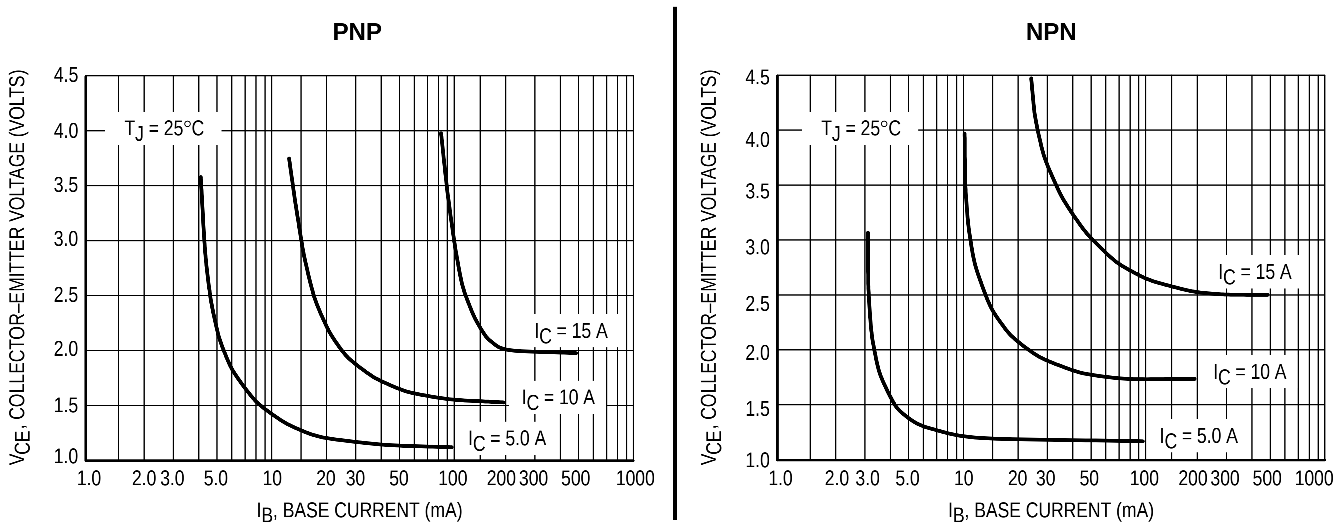


Figure 7. Collector Saturation Region

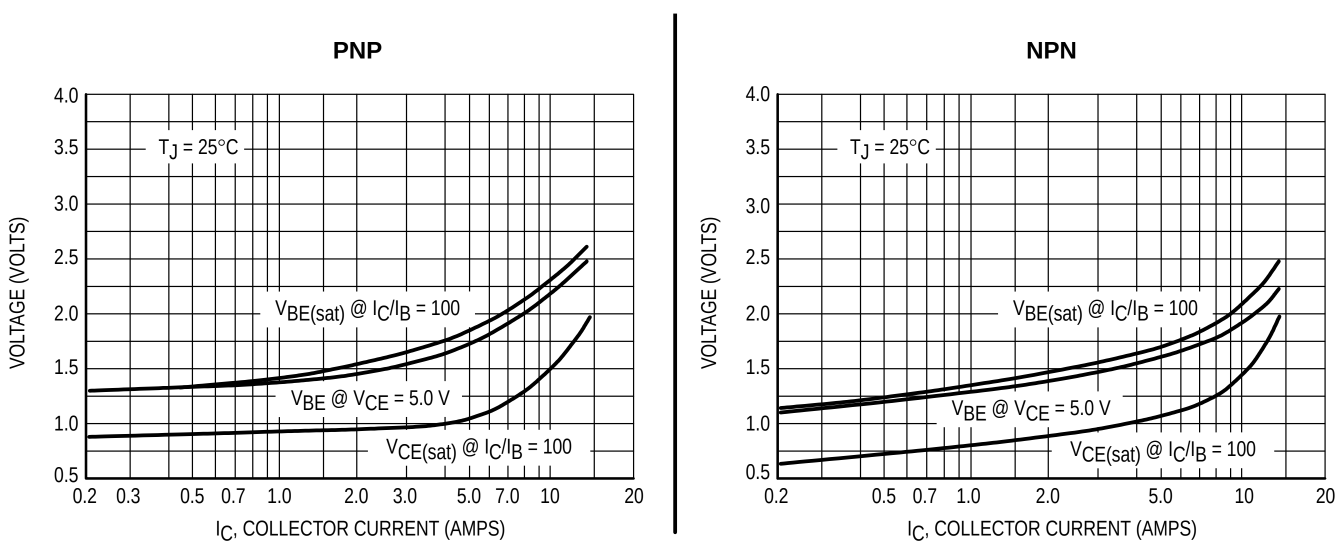


Figure 8. “On” Voltages

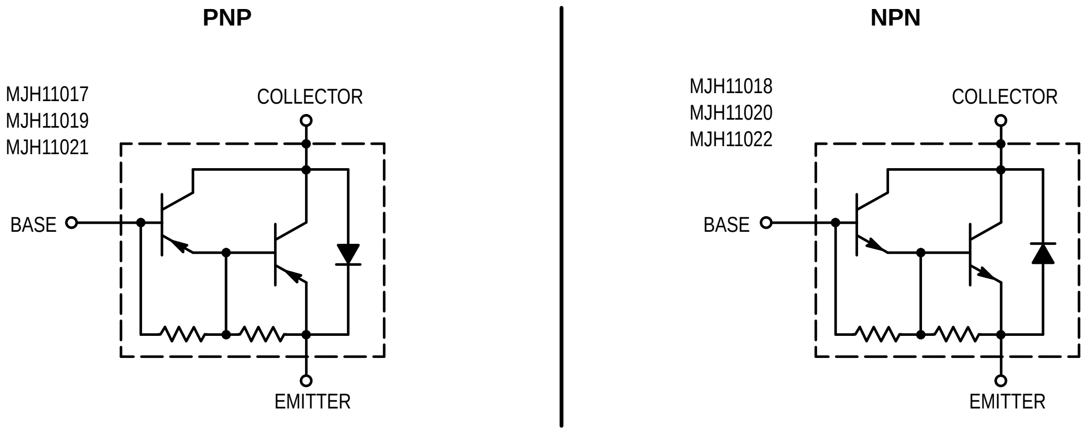
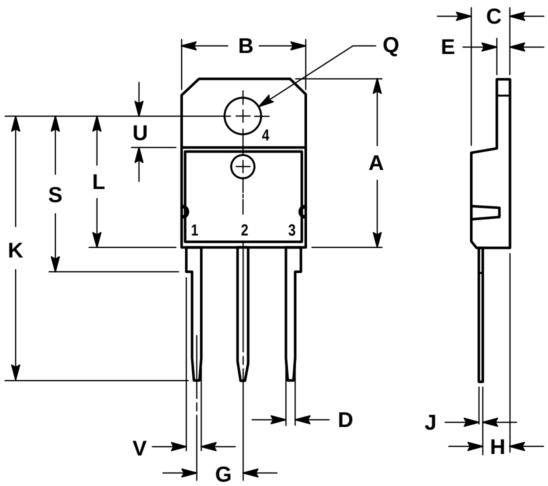


Figure 9. Darlington Schematic

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	19.00	19.60	0.749	0.771
B	14.00	14.50	0.551	0.570
C	4.20	4.70	0.165	0.185
D	1.00	1.30	0.040	0.051
E	1.45	1.65	0.058	0.064
G	5.21	5.72	0.206	0.225
H	2.60	3.00	0.103	0.118
J	0.40	0.60	0.016	0.023
K	28.50	32.00	1.123	1.259
L	14.70	15.30	0.579	0.602
Q	4.00	4.25	0.158	0.167
S	17.50	18.10	0.689	0.712
U	3.40	3.80	0.134	0.149
V	1.50	2.00	0.060	0.078

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 340D–01
SOT 93, TO–218 TYPE
ISSUE A

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