FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-16315-1E

32-bit Proprietary Microcontrollers

CMOS

FR30 Series

MB91126

■ DESCRIPTION

This model is a standard single-chip microcontroller with the 32-bit RISC CPU (FR30 family) as its core, incorporating a variety of I/O resources and bus control features for embedded control applications which require high-speed CPU processing.

With 10 KB of built-in RAM, the microcontroller is best suited for applications which require high-level CPU processing capabilities, such as navigation systems, high-performance FAX, and printer controllers.

■ FEATURES

FR-CPU

- 32-bit RISC (FR30), load/store architecture with a five-stage pipeline
- Operating frequency: Internal 25 MHz
- General purpose registers: 32 bits × 16 registers
- 16-bit fixed-length instructions (basic instructions): One instruction per cycle
- Memory-to-memory transfer, bit processing, and barrel shift instructions: Instructions suitable for embedded control applications
- Function entrance/exit instructions and register data multi-load/store instructions: Instructions applicable to high-level languages

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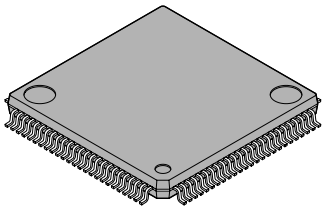
■ PACKAGE

100-pin Plastic LQFP



(FPT-100P-M05)

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- Register interlock functions: Facilitating coding in assemblers
- Branch instructions with delay slot: Reducing the overhead in branching
- Internal multiplier/supported at the instruction level
  Signed 32-bit multiplication: 5 cycles
  Signed 16-bit multiplication: 3 cycles
- Interrupt (saving PC and PS): 6 cycles, 16 priority levels

Bus interface

- Internal 25 MHz
- 25-bit address bus (32 MB space)
- 16-bit address output, 8-/16-bit data input/output
- Basic bus cycle : 2-clock cycle
- Chip select output that can be set to a minimum 64-Kbyte units : 6
- Interface support for various memories
  DRAM interface (Area 4 and 5)
- Automatic wait cycle insertion: Flexible setting, from 0 to 7 cycles per area
- Unused data/address pins can be configured as input/output ports.
- Little endian mode supported (One area selected from among area 1 to 5)

DRAM Interface

- Independent control of two banks (area 4 and 5)
- Double CAS DRAM (normal DRAM I/F)/Single CAS DRAM/Hyper DRAM
- Basic bus cycles: Normally 5 cycles. 2-cycle enabled in Fast Page mode.
- Programmable waveform: Capable of automatic insertion of one wait cycle to RAS and CAS
- DRAM refresh
  CBR refresh (Arbitrary interval setting using a 6-bit timer)
  Self-refresh mode
- 8/9/10/12-bit column addresses supported
- 2CAS/1WE or 2WE/1CAS selectable

DMAC (DMA controller)

- 8 channels
- Transfer incident: External pin/internal resource interrupt requests
- Transfer sequence: Step transfer/block transfer/burst transfer/continuous transfer
- Transfer data length: 8, 16, or 32 bits selectable
- Capable of pausing with an NMI/interrupt request

UART

- 3 channels
- Full duplex double buffer
- Data length 7 bits to 9 bits (without parity) , 6 bits to 8 bits (with parity)
- Asynchronous (start-stop system) or CLK-synchronized communication selectable
- Multi processor mode
- Internal 16-bit timer (U-Timer) as a baud rate generator: Generates any given baud rate.
- Capable of using an external clock as the transfer clock
- Error detection: Parity, frame, and overrun

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Reload Timer
- 16-bit timer : 3 channels
- Internal clock : 2-clock resolution, 2, 8 or 32 divide and external clock can be selected.

Other interval timer
- 16-bit timer : 3 channels (U-Timer)
- Watchdog timer: 1 channel

Built-in RAM 10 KB
- D-bus RAM 8 KB, C-bus RAM 2KB

Bit Search Module
- Searching the MSB in one word for the first 1/0 change bit position

Interrupt Controler
- External interrupt input : NMI, normal interrupt × 6 (INT0 to INT5)
- Internal interrupt sources : UART, DMAC, reload timer, UTIMER, delay interrupt
- Priority levels are programmable except for NMI (16 levels) .

Reset Source
- Power-on reset/watchdog timer/softwere reset/external reset

Low Power Consumption Mode
- Sleep/stop mode

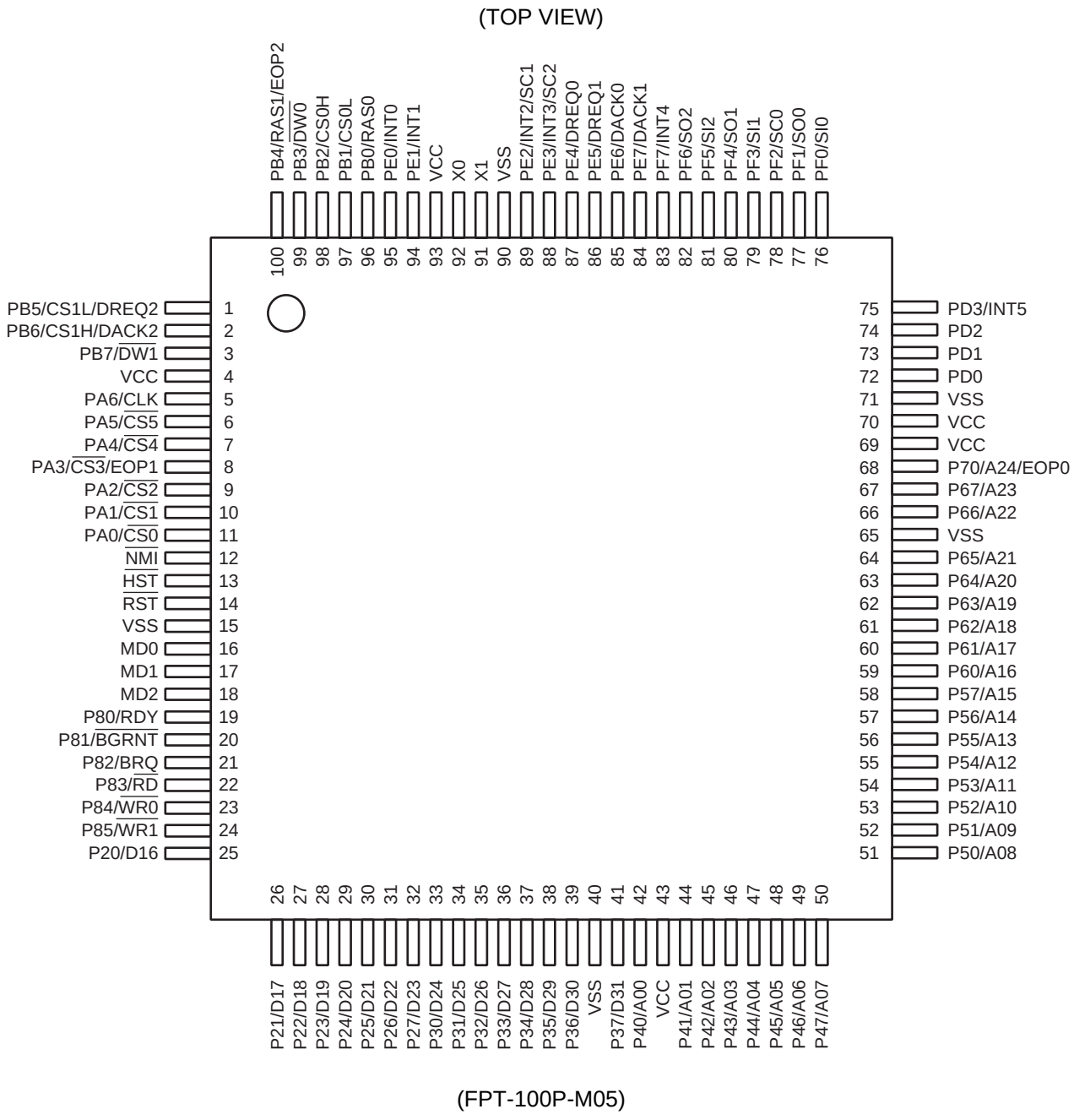
Clock control
- Built-in PLL circuit: PLL multiplication factor selectable from among 1, 1.5, and 2
- Gear function: Capable of freely setting different operating clock frequencies for the CPU and peripherals
  Gear clock selectable from among 1/1, 1/2, 1/4, and 1/8 (or among 1/2, 1/4, 1/8, and 1/16).
  Note, however, that peripherals operate at a maximum of 25 MHz.

Others
- Package : LQFP-100
- CMOS technology : 0.35 µm
- Power supply voltage : 3.3 V ± 0.3 V

■ PRODUCT LINEUP

Part number	MB91126	MB91FV129
Description	For mass production	For evaluation
FLASH Memory	—	510 KB
D-bus RAM	8 KB	16 KB
C-bus RAM	2 KB	2 KB

■ PIN ASSIGNMENT



■ PIN DESCRIPTIONS

Note that the numbers in the table are not pin numbers on a package.

NO.	Pin name	I/O circuit type	Function
1 2 3 4 5 6 7 8	D16/P20 D17/P21 D18/P22 D19/P23 D20/P24 D21/P25 D22/P26 D23/P27	D	These pins use bit 16 to bit 23 of the external data bus. They can be used as ports (P20 to P27) if the external bus width is 8 bits or in single chip mode.
9 10 11 12 13 14 15 16	D24/P30 D25/P31 D26/P32 D27/P33 D28/P34 D29/P35 D30/P36 D31/P37	D	These pins use bit 24 to bit 31 of the external data bus. They can serve as general purpose I/O pins (P30 to P37) when unassigned.
17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32	A00/P40 A01/P41 A02/P42 A03/P43 A04/P44 A05/P45 A06/P46 A07/P47 A08/P50 A09/P51 A10/P52 A11/P53 A12/P54 A13/P55 A14/P56 A15/P57	D	These pins use bit 00 to bit 15 of the external address bus. They can be used as general purpose I/O ports (P40 to P47, P50 to P57) when not used as address bus.
33 34 35 36 37 38 39 40	A16/P60 A17/P61 A18/P62 A19/P63 A20/P64 A21/P65 A22/P66 A23/P67	D	These pins use bits 16 to 23 of the external data bus. They can be used as general purpose I/O ports (P60 to P67) when not used as address bus.

(Continued)

<table>
<tr><th>NO.</th><th>Pin name</th><th>I/O circuit type</th><th>Function</th></tr>
<tr><td>41</td><td>A24/P70/EOP0</td><td>D</td><td>Bit 24 of the external address bus.
Enabled when the DMAC EOP output is enabled.
[P70] A24 can be used as a general purpose I/O port when EOP0 is not used.
[EOP0] DMAC EOP0 output (ch0)</td></tr>
<tr><td>42</td><td>RDY/P80</td><td>D</td><td>External ready input. This pin inputs 0 when the bus cycle being executed is not completed. It can serve as a general purpose I/O port when unassigned.</td></tr>
<tr><td>43</td><td>$\overline{\text{BGRNT}}$/P81</td><td>D</td><td>External bus release acknowledge output. This pin outputs the "L" level when the external bus is released. It can serve as a general purpose I/O port when unassigned.</td></tr>
<tr><td>44</td><td>BRQ/P82</td><td>D</td><td>External bus release request input. This pin inputs 1 when the external bus is required to be released. It can serve as a general purpose I/O port when unassigned.</td></tr>
<tr><td>45</td><td>$\overline{\text{RD}}$/P83</td><td>D</td><td>External bus read strobe.
It can serve as a general purpose I/O port when unassigned.</td></tr>
<tr><td>46</td><td>$\overline{\text{WR0}}$/P84</td><td>D</td><td rowspan="2">External bus write strobe.
Control signals and data bus byte positions have the following relationships:
<table><tr><th></th><th>16-bit bus width</th><th>8-bit bus width</th><th>Single chip mode</th></tr><tr><td>D31 to D24</td><td>$\overline{\text{WR0}}$</td><td>$\overline{\text{WR0}}$</td><td>(port enabled)</td></tr><tr><td>D23 to D16</td><td>$\overline{\text{WR1}}$</td><td>(port enabled)</td><td>(port enabled)</td></tr></table>
Notes :
$\overline{\text{WR1}}$ remains in High-Z state during a reset.
For use at a 16-bit bus width, add an external pull-up resistor.
[P84 or P85] $\overline{\text{WR0}}$ can be used as a general purpose I/O port when $\overline{\text{WR1}}$ is not used.</td></tr>
<tr><td>47</td><td>$\overline{\text{WR1}}$/P85</td><td>D</td></tr>
<tr><td>48
49
50</td><td>$\overline{\text{CS0}}$/PA0
$\overline{\text{CS1}}$/PA1
$\overline{\text{CS2}}$/PA2</td><td>D</td><td>Chip select 0 output (Low active)
Chip select 1 output (Low active)
Chip select 2 output (Low active)
[PA0, 1, 2] They can serve as general purpose I/O ports when unassigned.</td></tr>
<tr><td>51</td><td>$\overline{\text{CS3}}$/PA3/
EOP1</td><td>D</td><td>Chip select 3 output (Low active)
[EOP1] DMAC EOP output (ch1)
This funcyion is valid when DMAC and EOP output are enabled.
[PA3] It can serve as a general purpose I/O port when $\overline{\text{CS3}}$ and EOP1 are unassigned.</td></tr>
<tr><td>52
53</td><td>$\overline{\text{CS4}}$/PA4
$\overline{\text{CS5}}$/PA5</td><td>D</td><td>Chip select 4 output (Low active)
Chip select 5 output (Low active)
[PA4, 5] They can serve as general purpose I/O ports when unassigned.</td></tr>
<tr><td>54</td><td>CLK/PA6</td><td>D</td><td>System clock output
Outputs clock signal of external bus operating frequency.
[PA6] It can serve as a general purpose I/O port when unassigned.</td></tr>
</table>

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NO.	Pin name	I/O circuit type	Function
55 56 57 58 59 60 61 62	RAS0/PB0 CS0L/PB1 CS0H/PB2 $\overline{DW0}$/PB3 RAS1/PB4/EOP2 CS1L/PB5/DREQ2 CS1H/PB6/DACK2 $\overline{DW1}$/PB7	D	RAS output of DRAM bank 0 CASL output of DRAM bank 0 CASH output of DRAM bank 0 $\overline{WE}$ output of DRAM bank 0 (Low active) RAS output of DRAM bank 1 CASL output of DRAM bank 1 CASH output of DRAM bank 1 $\overline{WE}$ output of DRAM bank 1 (Low active) In detail, refer to “DRAM interface”. [EOP2] DMAC EOP output (ch2). This function is enabled when the DMAC EOP output is enabled. [DREQ2] DMA external transfer request input. Since this input is used as required when it has been selected as a DMAC transfer trigger event, the output by the other function must remain off unless used intentionally. [DACK2] DMAC external transfer request accept output (ch2). This function is enabled when the DMAC transfer request accept output is enabled. [PB0 to PB7] Available as general purpose I/O ports when unassigned.
63 64 65	MD0 MD1 MD2	B	Mode pins 0 to 2. These pins set the basic operation mode of the MCU. Connect the pins directly to V_{CC} or V_{SS}.
66 67	X0 X1	A	Clock (oscillation) input Clock (oscillation) output
68	$\overline{RST}$	C	External reset input
69	$\overline{HST}$	C	Hardwere standby input
70	$\overline{NMI}$	C	NMI (Non Maskable Interrupt) input (Low Active)
71 72	INT0/PE0 INT1/PE1	D	[INT0, 1] These are external interrupt request inputs. This input is always used while the corresponding external interrupt is permitted, so output using other functions should be stopped except when carried out intentionally. [PE0,PE1]General purpose I/O ports
73	INT2/PE2/SC1		[INT2] These are external interrupt request inputs. This input is always used while the corresponding external interruption is permitted, so output using other functions should be stopped except when carried out intentionally. [PE2] General purpose I/O port This function is effective if clock output specification of UART1 is pohibited. [SC1] UART1 clock input/output Clock output is effective if clock output specification of UART1 is permitted.

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NO.	Pin name	I/O circuit type	Function
74	INT3/PE3/SC2	D	[INT3] These are external interrupt request inputs. This input is always used while the corresponding external interrupt is permitted, so output using other functions should be stopped except when carried out intentionally. [SC2] UART2 clock input/output Clock output is effective if clock output specification of UART2 is permitted. [PE3]General purpose I/O port This function is effective if clock output specification of UART2 is pohibited.
			[PE4,PE5]General purpose I/O ports
75 76	DREQ0/PE4 DREQ1/PE5	D	[DREQ0, 1] These are DMA external interrupt transfer request inputs. This input is always used if selected as the transfer factor for DMAC, so outputs from other functions should be stopped except when carried out intentionally. [PE4,PE5]General purpose I/O ports
77	DACK0/PE6		[DACK0] This is the DMAC external transfer request accept output (ch 0) . This function is effective if the transfer request accept output specification of DMAC is prohibited. [PE6]General purpose I/O port This function is effective if the transfer request accept output specification of DMAC or DACK0 is prohibited.
78	DACK1/PE7	D	[DACK1] This is the DMAC external transfer request accept output (ch 1) . This function is effective if the transfer request accept output specification of DMAC is prohibited. [PE7]General purpose I/O port This function is effective if the transfer request accept output specification of DMAC or DACK1 is prohibited.
79	SI0/PF0		[SI0] UART0 data input This input is always used while UART inputs, so outputs from other functions should be stopped except when carried out intentionally. [PF0]General purpose I/O port
80	SO0/PF1	D	[SO0] UART0 data input This function is effective if the UART0 data output specification is permitted. [PF1]General purpose I/O port This function is effective if data output specification of UART0 is pohibited.
81	SC0/PF2	D	[SC0] UART0 clock output Clock output is effective if the UART0 clock output specification is permit-ted. [PF2]General purpose I/O port This function is effective if clock output specification of UART0 is prohibited.
82	SI1/PF3	D	[SI1] UART1 data input This function is always used if selected as the initiation factor for A/D, so output by other functions should be stopped except when it is carried out intentionally. [PF3]General purpose I/O port

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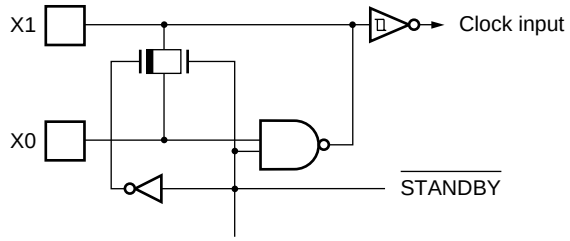
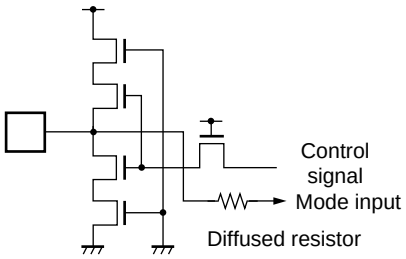
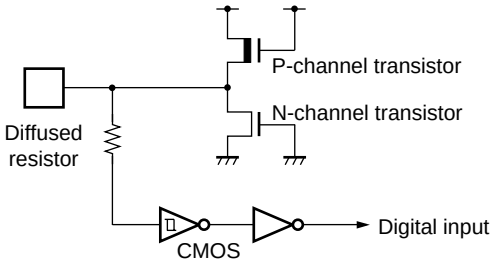
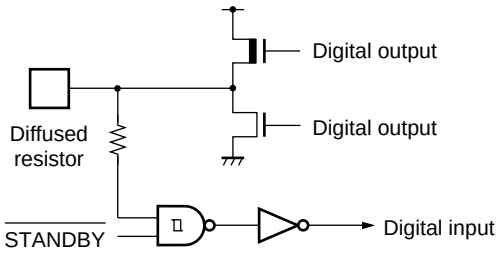
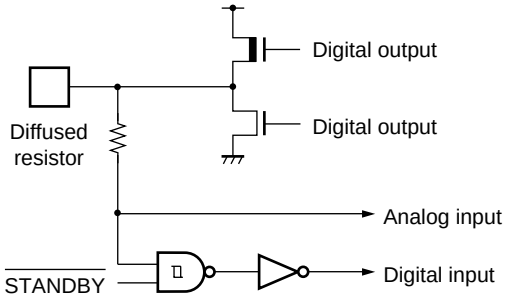
NO.	Pin name	I/O circuit type	Function
83	SO1/PF4	D	[SO1] UART1 data output This function is effective if data output specification of UART1 is permitted. [PF4]General purpose I/O port This function is effective if data output specification of UART1 is prohibited.
84	SI2/PF5	D	[SI2] UART2 data input This function is always used if selected as the initiation factor for A/D, so output by other functions should be stopped except when it is carried out intentionally. [PF5]General purpose I/O port
85	SO2/PF6	D	[SO2] UART2 data input This function is effective if data output specification of UART1 is permitted. [PF6] General purpose I/O port This function is effective if data output specification of UART1 is prohibited.
86	INT4/PF7	D	[INT4] External interrupt request input This function is always used if selected as the initiation factor for A/D, so output by other functions should be stopped except when it is carried out intentionally. [PF7] General purpose I/O port
87 to 89	PD0 PD1 PD2	E	[PD0 to PD2] General purpose I/O ports
90	PD3/INT5	E	[PD3]General purpose I/O port [INT5] External interrupt request input This function is always used if selected as the initiation factor for A/D, so output by other functions should be stopped except when it is carried out intentionally.
91 to 95	VCC	—	This provides power for the circuit system. Always power supply pin (VCC) must be connected to the power supply.
96 to 100	VSS	—	This is the earth level for digital circuits.

Note : The I/O port and resource input/outputs for most of the above pins are multiplexed, i.e. Pxx/xxxx. In the event of both the port and resource outputs were to use the same pins, the resource is given priority.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		For 25 MHz Oscillation feedback resistor : approx. 1 MΩ Standby control OFF
B		• CMOS level input. • With high voltage control for FLASH test
C		• CMOS level, hysteresis input. • Standby control OFF
D		• CMOS level output • CMOS level, hysteresis input. • Standby control ON
E		• Standby control ON • CMOS level output • CMOS level, hysteresis input. • Analog input

■ HANDLING DEVICES

1. Preventing Latch-up

The latch-up phenomenon may be generated if a voltage in excess of V_{CC} or lower than V_{SS} is applied to the input/output pins, or if the voltage exceeds the rating between V_{CC} and V_{SS}.

If latch-up is generated, the electrical current increases significantly and may destroy certain components due to the excessive heat, so great care must be taken to ensure that the maximum rating is not exceeded during use.

Also, care must be taken to ensure that the analog pin does not exceed the digital power supply.

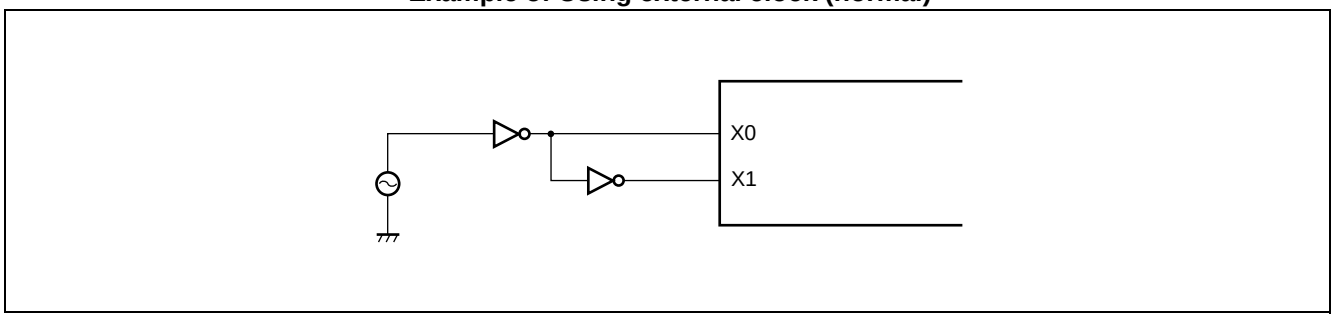
2. Treatment of Pins

- **Handling Unused Input Pins**
  Input pins that are not used should be pulled up or down as they may cause erroneous operations if they are left open.
- **Crystal Oscillator Circuit**
  Noise around the X0 or X1 pins may cause erroneous operation. Make sure to provide bypass capacitors via shortest distances from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure that lines of oscillation circuits not cross the lines of other circuit.
  A printed circuit board artwork surrounding the X0 and X1 pins with ground area for stabilizing the operation is highly recommended .
- **N.C. Pins**
  N.C. pin must be opened for use.
- **Mode Pins (MD0 to MD2)**
  Those pins must be directly connected to V_{CC} or V_{SS} for use.
  Pattern length between V_{CC} or V_{SS} and each mode pin on the printed-circuit board should be arranged to be as short as possible to prevent the test mode being erroneously turned on due to noise, they should also be connected with low impedance.

3. Precautions

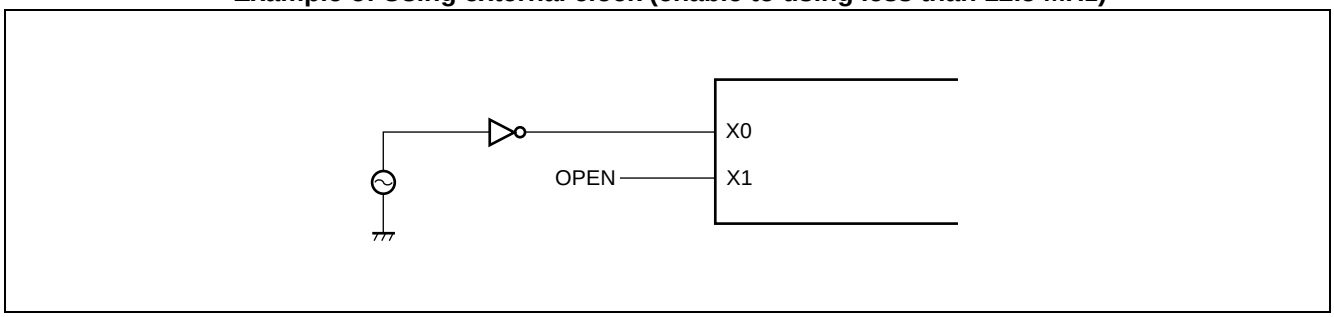
- **External Reset Input**
  “L” level should be input to the $\overline{RST}$ pin, which is required for at least five machine cycles to ensure the internal status is reset.
- **Notes on Using External Clock**
  If external clock is used, X0 pin should be provided, and X1 pin should be provided with reverse phase to X0 pin. However, in this case, do not use the STOP mode (oscillation stop mode) . (At STOP, the X1 pin is stopped with the “H”).
  Under a 12.5 MHz frequency, the device operates with a clock supplied to X0 terminal only.
  Examples of the external clock usage methods is shown below.

Example of Using external clock (normal)



Note : It cannot use in the STOP mode (oscillation stop mode) .

Example of Using external clock (enable to using less than 12.5 MHz)



- **Power Supply Pins (V_{CC}, V_{SS})**
  In products with multiple Vcc or Vss pins, the pins of the same potential are internally connected in the device to avoid abnormal operations including latch-up. However you must connect the pins to an external power and a ground line to lower the electro-magnetic emission level to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total current rating.
  Make sure to connect Vcc and Vss pins via the lowest impedance to power lines.

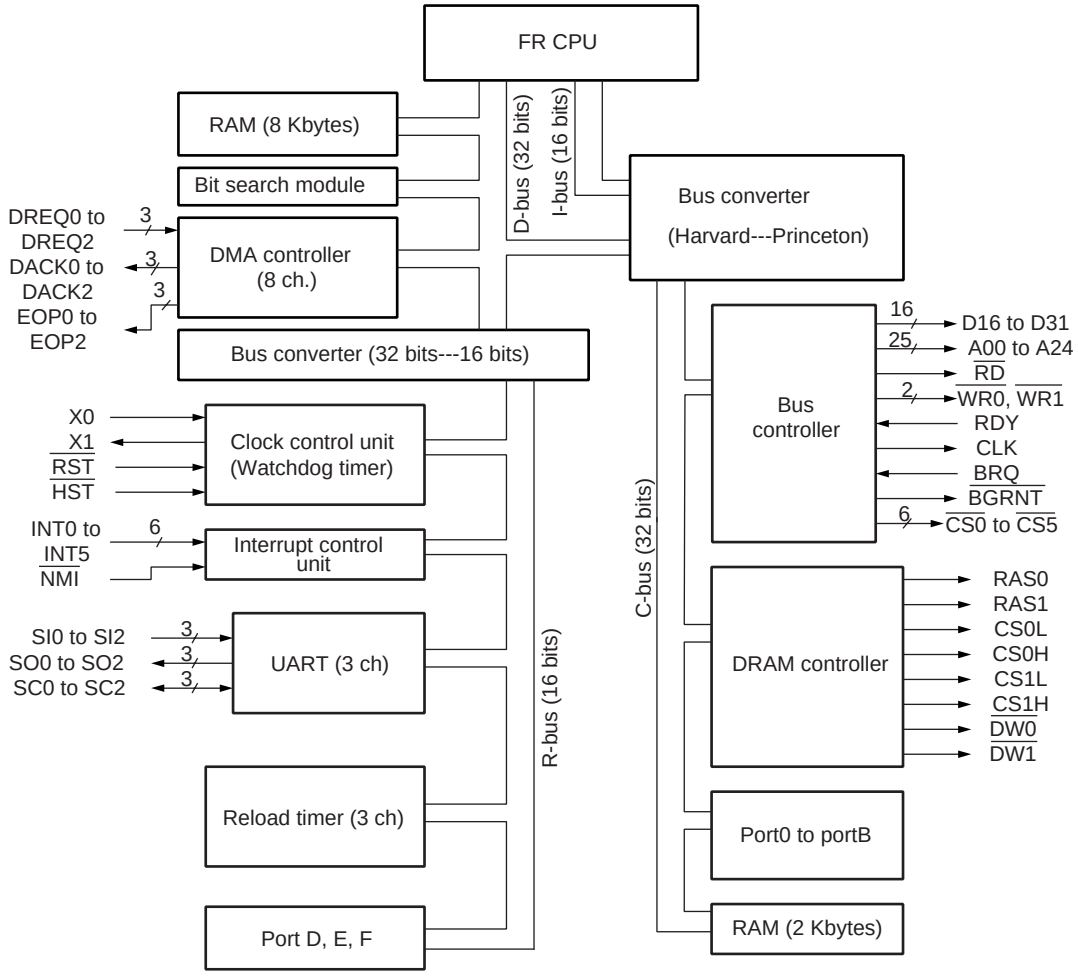
4. Care During Power Up

- **Power-on**
  The $\overline{RST}$ pin must be started from “L” level when the power is turned on, and when the power is adjusted to the VCC level it should be changed to the “H” level after being left for at least five cycles of the internal operation clock.
- **Pin condition at the power-on**
  The pin condition at turning on the power supply is unstable. The circuit starts being initialized after turning on the power supply and then starting oscillation.
- **Original Oscillation Input in the Event that Power Is Turned on**
  The clock must be input until the waiting status for oscillation stability is reset in the event that power is turned on.
- **Initialization of power-on reset**
  In the device, there are internal registers which is initialized only by a power-on reset. To initialize these resistors, run power-on reset by returning on the power supply.
- **Recovery for sleep/stop**
  For recovering from sleep/stop status initiated by a program in C-Bus RAM, reset the device instead of recovering by an interrupt process.

5. Notes on during operation of PLL clock mode

If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

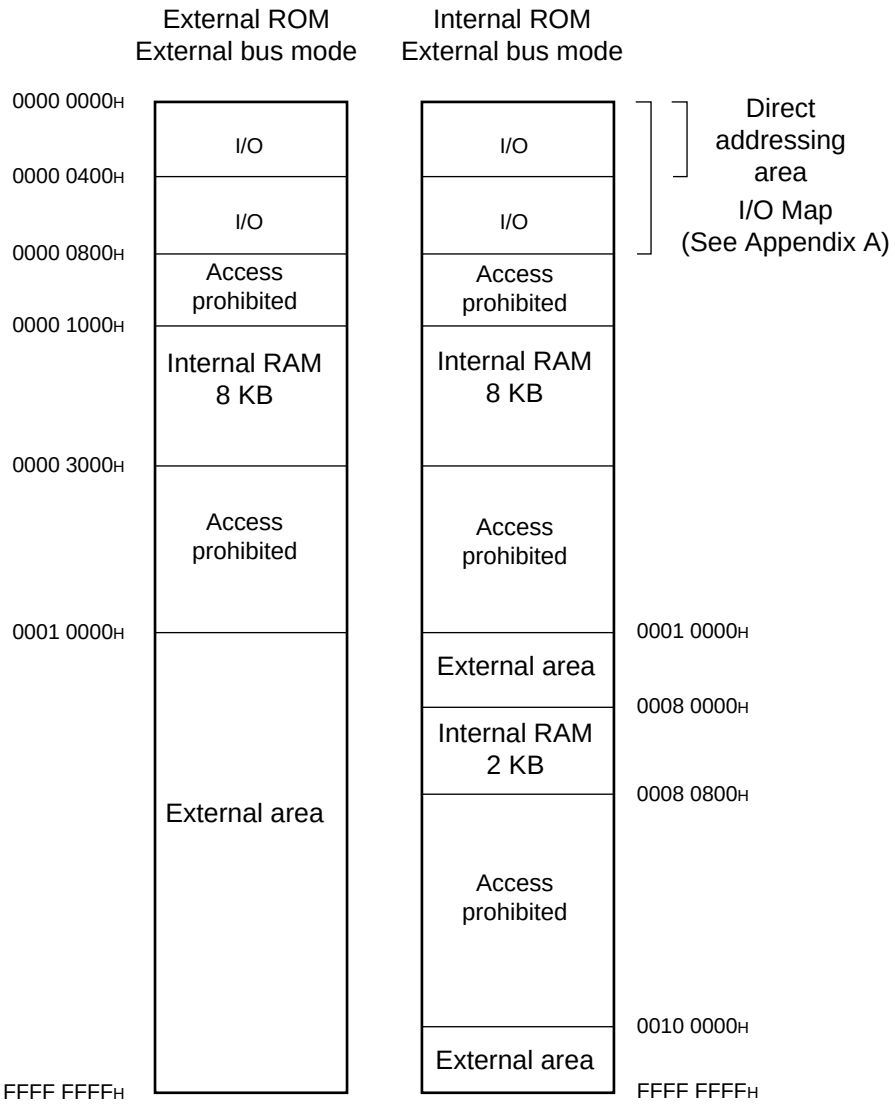
■ BLOCK DIAGRAM



Notes :
- Pins are described per function. Some of the pins are multiplexed.
- In the event that REALOS is used, an external interruption or built-in timer should be used to control the time.

■ MEMORY MAP

The memory space of MB91126 is shown.



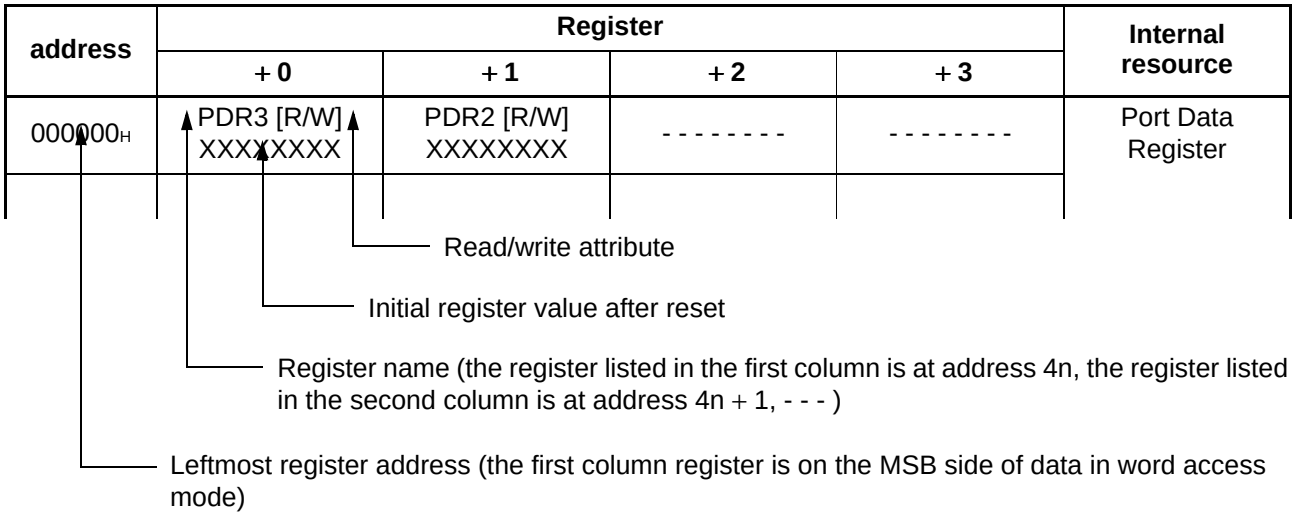
Note : External area is not accessible in single-chip mode. When accessing to external areas, select the internal ROM external bus mode in mode register.

Direct addressing area

The following areas of the address space are used for I/O. This area is called the “direct addressing area” and the address of the operand can be specified directly during instruction. The direct area differs depending on data size to be accessed.

- Byte data access : 0 to 0FF$_H$
- Half word data access : 0 to 1FF$_H$
- Word data access : 0 to 3FF$_H$

■ HOW TO READ I/O MAP



Note : Register bit value indicate initial values as shown below.

“1” : Initial value “1”

“0” : Initial value “0”

“X” : Initial value “X”

“-” : Register does not exist physically in this position.

■ I/O MAP

Address	Register				Internal resources
	+ 0	+ 1	+ 2	+ 3	
000000H	PDR3 [R/W] XXXXXXXX	PDR2 [R/W] XXXXXXXX	—	—	Port data register
000004H	PDR7 [R/W] - - - - - - - X	PDR6 [R/W] XXXXXXXX	PDR5 [R/W] XXXXXXXX	PDR4 [R/W] XXXXXXXX	
000008H	PDRB [R/W] XXXXXXXX	PDRA [R/W] XXXXXXXX	—	PDR8[R/W] - - XXXXXX	
00000CH	—				
000010H	—	PDRD [R/W] - - - - XXXX	PDRE [R/W] XXXXXXXX	PDRF [R/W] XXXXXXXX	
000014H	—	—	—	—	
000018H	—	—	—	—	Reserved
00001CH	SSR [R/W] 00001- 00	SIDR [R/W] XXXXXXXX	SCR [R/W] 00000100	SMR [R/W] 00 - - 0 - 00	UART0
000020H	SSR [R/W] 00001- 00	SIDR [R/W] XXXXXXXX	SCR [R/W] 00000100	SMR [R/W] 00 - - 0 - 00	UART1
000024H	SSR [R/W] 00001- 00	SIDR [R/W] XXXXXXXX	SCR [R/W] 00000100	SMR [R/W] 00 - - 0 - 00	UART2
000028H	TMRLR [W] XXXXXXXX XXXXXXXX		TMR [W] XXXXXXXX XXXXXXXX		Reload timer 0
00002CH	—		TMCSR [R/W] - - - - 0000 00000000		
000030H	TMRLR [W] XXXXXXXX XXXXXXXX		TMR [W] XXXXXXXX XXXXXXXX		Reload timer 1
000034H	—		TMCSR [R/W] - - - - 0000 00000000		
00003CH	TMRLR [W] XXXXXXXX XXXXXXXX		TMR [W] XXXXXXXX XXXXXXXX		Reload timer 2
000040H	—		TMCSR [R/W] - - - - 0000 00000000		
000044H	—		—		Reserved
000048H	—		—		
00004CH	—		—		
000050H	—		—		
000054H	—		—		
000058H	—		—		

(Continued)

Address	Register				Internal resources
	+ 0	+ 1	+ 2	+ 3	
00005C$_H$	—		—		Reserved
000060$_H$	—		—		
000064$_H$	—		—		
000068$_H$	—		—		
00006C$_H$	—		—		
000070$_H$	—		—		
000074$_H$	—		—		
000078$_H$	UTM/UTIMR [R/W] 00000000 00000000		—	UTIMC[R/W] 0 - - 00001	U-timer 0
00007C$_H$	UTM/UTIMR [R/W] 00000000 00000000		—	UTIMC[R/W] 0 - - 00001	U-timer 1
000080$_H$	UTM/UTIMR [R/W] 00000000 00000000		—	UTIMC[R/W] 0 - - 00001	U-timer 2
000084$_H$	—		—		Reserved
000088$_H$	—		—		
00008C$_H$	—		—		Reserved
000090$_H$	—		—		
000094$_H$	EIRR [R/W] 00000000	ENIR [R/W] 00000000	—		External interrupt /NMI
000098$_H$	EHVR [R/W] - - - - 0000	ELVR [R/W] 00000000	—		
00009C$_H$	—				Reserved
0000A0$_H$	—				
0000A4$_H$	—				
0000A8$_H$	—				
0000AC$_H$	—				
0000B0$_H$	—				
0000B4$_H$	—				
0000B8$_H$	—				
0000BC$_H$	—				
0000C0$_H$	—				
0000C4$_H$	—				
0000C8$_H$	—				
0000CC$_H$	—				
0000D0$_H$	—	DDRD [W] - - - - 0000	DDRE [W] 00000000	DDRF [W] 00000000	Port direction register

(Continued)

Address	Register				Internal resources
	+ 0	+ 1	+ 2	+ 3	
0000D8H	—	—	—	—	Reserved
0000DCH to 0000FCH	—				Reserved
000100H to 0001FCH	—				Reserved
000200H	DPDP [R/W] -0000000				DMAC
000204H	DACSR [R/W] 00000000 00000000 00000000 00000000				
000208H	DATCR [R/W] - - - - - - - - - - - XX0000 - - XX0000 - - XX0000				
00020CH	—				
000210H to 0002FCH	—				Reserved
000300H to 0003ECH	—				Reserved
0003F0H	BSD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit search module
0003F4H	BSD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003F8H	BSDC [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003FCH	BSRR [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000400H	ICR00 [R/W] - - -11111	ICR01[R/W] - - -11111	ICR02[R/W] - - -11111	ICR03[R/W] - - -11111	Interrupt controller
000404H	ICR04[R/W] - - -11111	ICR05[R/W] - - -11111	ICR06[R/W] - - -11111	ICR07[R/W] - - -11111	
000408H	ICR08 [R/W] - - -11111	ICR09[R/W] - - -11111	ICR10[R/W] - - -11111	ICR11[R/W] - - -11111	
00040CH	ICR12[R/W] - - -11111	ICR13[R/W] - - -11111	ICR14[R/W] - - -11111	ICR15[R/W] - - -11111	
000410H	ICR16[R/W] - - -11111	ICR17[R/W] - - -11111	ICR18[R/W] - - -11111	ICR19[R/W] - - -11111	

(Continued)

Address	Register				Internal resources
	+ 0	+ 1	+ 2	+ 3	
000414H	ICR20[R/W] - - -11111	ICR21[R/W] - - -11111	ICR22[R/W] - - -11111	ICR23[R/W] - - -11111	Interrupt controller
000418H	ICR24 [R/W] - - -11111	ICR25[R/W] - - -11111	ICR26[R/W] - - -11111	ICR27[R/W] - - -11111	
00041CH	ICR28[R/W] - - -11111	ICR29[R/W] - - -11111	ICR30[R/W] - - -11111	ICR31[R/W] - - -11111	
000420H	—	—	—	—	
000424H	—	—	—	—	
000428H	—	—	—	—	
00042CH	—	—	—	ICR47[R/W] - - -11111	
000430H	DICR [R/W] - - - - - - - 0	HRCL [R/W] - - -11111	—	—	Delay interruption
000434H to 00047CH	—				Reserved
000480H	RSRR/WTCR [R/W] 1XXXX- 00	STCR [R/W] 000111- -	PDDR [R/W] - - - - 0000	CTBR [W] XXXXXXXX	Clock control block
000484H	GCR [R/W] 110011 - 1	WPR [W] XXXXXXXX	—	—	
000488H	PTCR [R/W] 00 - - 0 - - -	—			PLL control block
00048CH to 0005FCH	—				Reserved
000600H	DDR3 [W] 00000000	DDR2 [W] 00000000	—	—	Data direction register
000604H	DDR7 [W] - - - - - - - 0	DDR6 [W] 00000000	DDR5 [W] 00000000	DDR4 [W] 00000000	
000608H	DDRB [W] 00000000	DDRA [W] -0000000	—	DDR8 [W] - - 000000	
00060CH	ASR1 [W] 00000000 00000001		AMR1 [W] 00000000 00000000		External bus interface
000610H	ASR2 [W] 00000000 00000010		AMR2 [W] 00000000 00000000		
000614H	ASR3 [W] 00000000 00000011		AMR3 [W] 00000000 00000000		
000618H	ASR4 [W] 00000000 00000100		AMR4 [W] 00000000 00000000		

(Continued)

(Continued)

Address	Register				Internal resources
	+ 0	+ 1	+ 2	+ 3	
00061C$_H$	ASR5 [W] 00000000 00000101		AMR5 [W] 00000000 00000000		External bus interface
000620$_H$	AMD0 [R/W] - - - XX111	AMD1 [R/W] 0 - - 00000	AMD32[R/W] 00000000	AMD4 [R/W] 0 - - 00000	
000624$_H$	AMD5[R/W] 0 - - 00000	DSCR [W] 00000000	RFCR [R/W] --XXXXXX 00 - - - 000		
000628$_H$	EPCR0 [W] - - 1 - 1100 -1111111		EPCR1 [W] - - - - - - - 1 11111111		
00062C$_H$	DMCR4 [R/W] 00000000 0000000-		DMCR5 [R/W] 00000000 0000000-		
000630$_H$ to 0007BC$_H$	—				Reserved
0007C0$_H$	—	—	—	—	Reserved
0007C4$_H$ to 0007F8$_H$	—				Reserved
0007FC$_H$	—		LER [W] - - - - - 000	MODR [W] XXXXXXXX	Little endian register mode register

Note : Do not execute RMW instructions to registers with write-only bits.

RMW instruction (RMW : Read/Modify/Write)

AND Rj, @Ri	OR Rj, @Ri	EOR Rj, @Ri
ANDH Rj, @Ri	ORH Rj, @Ri	EORH Rj, @Ri
ANDB Rj, @Ri	ORB Rj, @Ri	EORB Rj, @Ri
BANDL #u4, @Ri	BORL #u4, @Ri	BEORL #u4, @Ri
BANDH #u4, @Ri	BORH #u4, @Ri	BEORH #u4, @Ri

Data in “Reserved” or “—” is undecided.

■ INTERRUPT VECTOR

Interrupt source	IInterrupt number		Interrupt level *1	Offset	Address of TBR default*2
	Decimal	Hexadecimal			
Reset	0	00	—	$3FC_H$	$000FFFFC_H$
System reservation	1	01	—	$3F8_H$	$000FFFF8_H$
System reservation	2	02	—	$3F4_H$	$000FFFF4_H$
System reservation	3	03	—	$3F0_H$	$000FFFF0_H$
System reservation	4	04	—	$3EC_H$	$000FFFEC_H$
System reservation	5	05	—	$3E8_H$	$000FFFE8_H$
System reservation	6	06	—	$3E4_H$	$000FFFE4_H$
System reservation	7	07	—	$3E0_H$	$000FFFE0_H$
System reservation	8	08	—	$3DC_H$	$000FFFDC_H$
System reservation	9	09	—	$3D8_H$	$000FFFD8_H$
System reservation	10	0A	—	$3D4_H$	$000FFFD4_H$
System reservation	11	0B	—	$3D0_H$	$000FFFD0_H$
System reservation	12	0C	—	$3CC_H$	$000FFFCC_H$
System reservation	13	0D	—	$3C8_H$	$000FFFC8_H$
Exceptions to undefined instruction	14	0E	—	$3C4_H$	$000FFFC4_H$
NMI request	15	0F	15 (F_H) fixed	$3C0_H$	$000FFFC0_H$
External interrupt 0	16	10	ICR00	$3BC_H$	$000FFFBC_H$
External interrupt 1	17	11	ICR01	$3B8_H$	$000FFFB8_H$
External interrupt 2	18	12	ICR02	$3B4_H$	$000FFFB4_H$
External interrupt 3	19	13	ICR03	$3B0_H$	$000FFFB0_H$
UART 0 reception completed	20	14	ICR04	$3AC_H$	$000FFFAC_H$
UART1 reception completed	21	15	ICR05	$3A8_H$	$000FFFA8_H$
UART2 reception completed	22	16	ICR06	$3A4_H$	$000FFFA4_H$
UART0 transmission completed	23	17	ICR07	$3A0_H$	$000FFFA0_H$
UART1 transmission completed	24	18	ICR08	$39C_H$	$000FFF9C_H$
UART2 transmission completed	25	19	ICR09	398_H	$000FFF98_H$
DMAC 0 (end, error)	26	1A	ICR10	394_H	$000FFF94_H$
DMAC 1 (end, error)	27	1B	ICR11	390_H	$000FFF90_H$
DMAC 2 (end, error)	28	1C	ICR12	$38C_H$	$000FFF8C_H$
DMAC 3 (end, error)	29	1D	ICR13	388_H	$000FFF88_H$
DMAC 4 (end, error)	30	1E	ICR14	384_H	$000FFF84_H$
DMAC 5 (end, error)	31	1F	ICR15	380_H	$000FFF80_H$
DMAC 6 (end, error)	32	20	ICR16	$37C_H$	$000FFF7C_H$
DMAC 7 (end, error)	33	21	ICR17	378_H	$000FFF78_H$
System reservation	34	22	ICR18	374_H	$000FFF74_H$

(Continued)

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Interrupt source	IInterrupt number		Interrupt level *1	Offset	Address of TBR default*2
	Decimal	Hexadeci-mal			
Reload timer 0	35	23	ICR19	370_H	$000FFF70_H$
Reload timer 1	36	24	ICR20	$36C_H$	$000FFF6C_H$
Reload timer 2	37	25	ICR21	368_H	$000FFF68_H$
External interrupt 4	38	26	ICR22	364_H	$000FFF64_H$
External interrupt 5	39	27	ICR23	360_H	$000FFF60_H$
System reservation	40	28	ICR24	$35C_H$	$000FFF5C_H$
System reservation	41	29	ICR25	358_H	$000FFF58_H$
U-TIMER 0	42	2A	ICR26	354_H	$000FFF54_H$
U-TIMER 1	43	2B	ICR27	350_H	$000FFF50_H$
U-TIMER 2	44	2C	ICR28	$34C_H$	$000FFF4C_H$
System reservation	45	2D	ICR29	348_H	$000FFF48_H$
System reservation	46	2E	ICR30	344_H	$000FFF44_H$
System reservation	47	2F	ICR31	340_H	$000FFF40_H$
System reservation	48	30	ICR32	$33C_H$	$000FFF3C_H$
System reservation	49	31	ICR33	338_H	$000FFF38_H$
System reservation	50	32	ICR34	334_H	$000FFF34_H$
System reservation	51	33	ICR35	330_H	$000FFF30_H$
System reservation	52	34	ICR36	$32C_H$	$000FFF2C_H$
System reservation	53	35	ICR37	328_H	$000FFF28_H$
System reservation	54	36	ICR38	324_H	$000FFF24_H$
System reservation	55	37	ICR39	320_H	$000FFF20_H$
System reservation	56	38	ICR40	$31C_H$	$000FFF1C_H$
System reservation	57	39	ICR41	318_H	$000FFF18_H$
System reservation	58	3A	ICR42	314_H	$000FFF14_H$
System reservation	59	3B	ICR43	310_H	$000FFF10_H$
System reservation	60	3C	ICR44	$30C_H$	$000FFF0C_H$
System reservation	61	3D	ICR45	308_H	$000FFF08_H$
System reservation	62	3E	ICR46	304_H	$000FFF04_H$
Delay interrupt source bit	63	3F	ICR47	300_H	$000FFF00_H$
System reservation (used under REALOS) *3	64	40	—	$2FC_H$	$000FFEFC_H$
System reservation (used under REALOS) *3	65	41	—	$2F8_H$	$000FFEF8_H$
Used under INT instruction	66 to 255	42 to FF	—	$2F4_H$ to 000_H	$000FFEF4_H$ to $000FFC00_H$

*1 : ICRs are registers in the interrupt controller that set the interrupt levels for individual interrupt requests.
An ICR is provided for each interrupt request.

*2 : The TBR is the register that holds the start address of the EIT vector table.
The address obtained by adding the offset value defined for each EIT to the TBR value is used as the vector address.

*3 : When REALOS/FR is used, 0x40 and 0x41 interrupts are used for system code.

Reference : The EIT vector area is one kilobyte long starting at the address held in the TBR. The size for each vector is four bytes. Vector numbers and vector addresses have the following relationships:

vctadr = TBR + vctofs
= TBR + (3FC H – 4 × vct)
vctadr : vector address, vctofs : vector offset, vct : vector number

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(V_{SS} = 0 V)

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	V_{SS} – 0.3	V_{SS} + 4.0	V	
Input voltage	V_I	V_{SS} – 0.3	V_{CC} + 0.3	V	
Output voltage	V_O	V_{SS} – 0.3	V_{CC} + 0.3	V	
Maximum clamp current	I_{CLAMP}	– 2.0	+ 2.0	mA	*4
Total maximum clamp current	$\Sigma \mid I_{CLAMP} \mid$	—	20	mA	*4
“L” level maximum output current	I_{OL}	—	10	mA	*1
“L” level average output current	I_{OLAV}	—	4	mA	*2
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current	ΣI_{OLAV}	—	50	mA	*3
“H” level maximum output current	I_{OH}	—	– 10	mA	*1
“H” level average output current	I_{OHAV}	—	– 4	mA	*2
“H” level total maximum output current	ΣI_{OH}	—	– 50	mA	
“H” level total average output current	ΣI_{OHAV}	—	– 20	mA	*3
Power consumption	Pd	—	500	mW	
Operating temperature	Ta	– 30	+ 70	°C	
Storage temperature	Tstg	– 55	+ 150	°C	

*1 : The maximum output current specifies the peak current for the relevant single pin.

*2 : The average output current specifies the mean value of the current flowing in the relevant single pin during a period of 100 ms.

*3 : The average total output current specifies the mean value of the currents flowing in all of the relevant pins during a period of 100 ms.

*4 : • Applicable to pins: P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70, P80 to P85, PA0 to PA6, PB0 to PB7, PD0 to PD3, PE0 to PE7, PF0 to PF7
- Use within recommended operating conditions.
- Use at DC voltage (current) .
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Note that analog system input/output pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal input.

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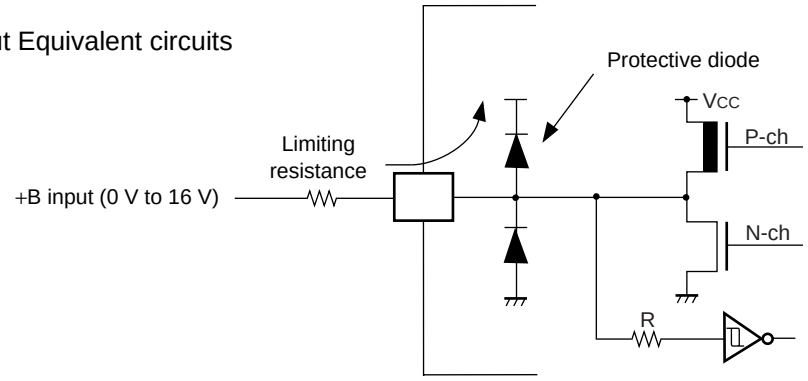
- Sample recommended circuits:

• Input/Output Equivalent circuits



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = 0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	3.0	3.6	V	At normal operating
		2.0	3.6		Keeping RAM status in the case of stopping
Operating temperature	Ta	− 30	+ 70	°C	

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

(V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V, Ta = –30 °C to +70 °C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IHS}	Hysteresis input pin	—	0.8 × V_{CC}	—	V_{CC} + 0.3	V	*
"L" level input voltage	V_{ILS}	Hysteresis input pin	—	V_{SS} – 0.3	—	0.2 × Vcc	V	*
"H" level output voltage	V_{OH}	Port2 to PortF	V_{CC} = 3.3 V I_{OH} = – 4.0 mA	V_{CC} – 0.5	—	—	V	
"L" level output voltage	V_{OL}	Port2 to PortF	V_{CC} = 3.3V I_{OL} = 4.0 mA	—	—	0.4	V	
Input leak current	I_{LI}	Port2 to PortF	V_{CC} = 3.6 V V_{SS} < VI < V_{CC}	—	—	± 5	µA	
Power supply current	I_{CC}	VCC	25 MHz V_{CC} = 3.3 V	—	75	100	mA	
	I_{CCS}		25 MHz V_{CC} = 3.3 V	—	60	85	mA	at sleep mode
	I_{CCH}		Ta = + 25 °C V_{CC} = 3.3 V	—	10	150	µA	at stop mode
Input capacitance	C_{IN}	Without VCC, VSS	—	—	10	—	pF	

* : See "■ I/O CIRCUIT TYPE"

4. AC Characteristics

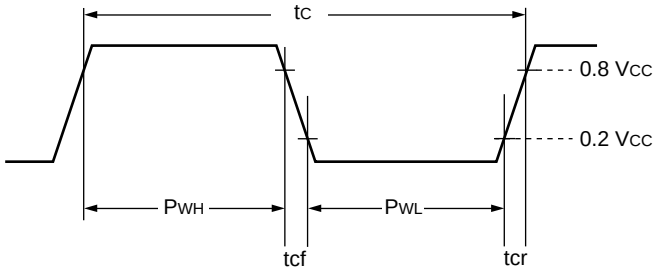
(1) Clock Timing

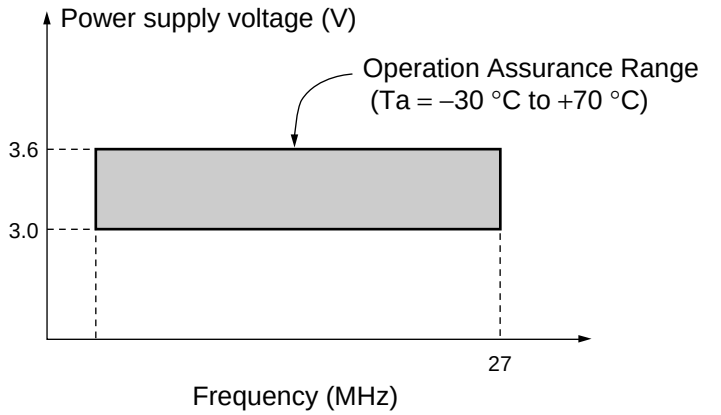
(V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V, Ta = –30 °C to +70 °C)

Parameter		Symbol	Condition	Value		Unit	Remarks
				Min	Max		
Clock frequency (High-speed • self oscillation)		f_C	—	10	25	MHz	Range in which self oscillation is allowed
Clock frequency (High-speed • PLL using)				10	25	MHz	Range in which self oscillation and external clock input is allowed*1
Clock frequency (High-speed • 1/2 cycle input)				10	25	MHz	Range in which external clock input is allowed
Clock cycle time		t_C		40	100	ns	
Input clock pulse width		P_{WH}, P_{WL}	—	9.5	—	ns	
Input clock Rise/fall time		t_{CR} t_{CF}	—	—	8	ns	(t_{CR} + t_{CF})
Internal operating clock frequency	CPU system	f_{CP}	—	0.625*2	25	MHz	
	Peripheral	f_{CPP}		0.625*2	25	MHz	
Internal operating clock cycle time	CPU system	t_{CP}		40	1600*2	ns	
	Peripheral	t_{LCPP}		40	1600*2	ns	

*1 : A multiplication factor of 1 or 2 can be selected for the PLL. It is however restricted depending on the operating oscillation frequency.
Do not set the PLL multiplication factor to 2 when the oscillation frequency exceeds 12.5 MHz.

*2 : This value is obtained when an oscillation circuit divide ratio of 2 and a gear cycle of 1/8 are used with a minimum clock frequency of 10 MHz input to X0.




Power supply voltage (V)
Operation Assurance Range
(Ta = –30 °C to +70 °C)
3.6
3.0
27
Frequency (MHz)

(2) Clock Output Timing

(V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V, Ta = –30 °C to +70 °C)

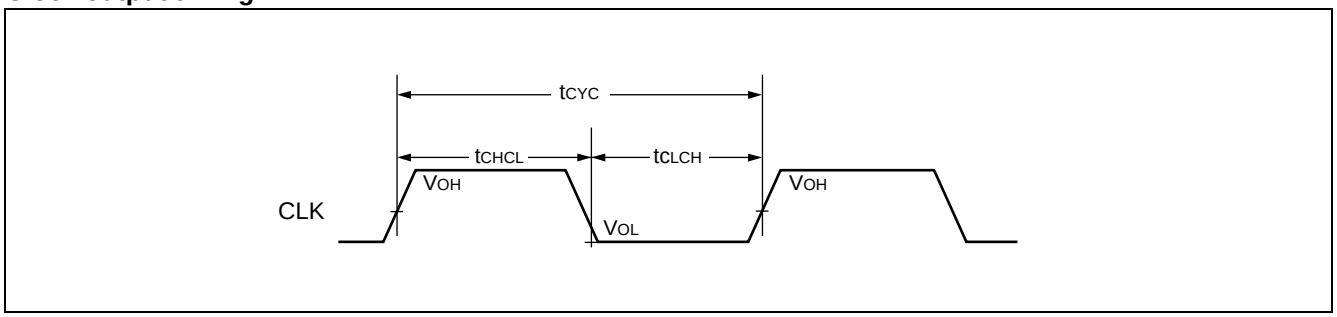
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	CLK	—	t_{CP}	—	ns	*1
CLK ↑ → CLK ↓	t_{CHCL}	CLK		1 / 2 × t_{CYC} – 10	1 / 2 × t_{CYC} + 10	ns	*2
CLK ↓ → CLK ↑	t_{CLCH}	CLK		1 / 2 × t_{CYC} – 10	1 / 2 × t_{CYC} + 10	ns	*3

*1 : t_{CYC} is frequency of 1 clock cycle including the gear cycle.

*2 : The values assume a gear cycle of × 1.
When a gear cycle of 1/2, 1/4, or 1/8 is specified, substitute “n” in the following equations with 1/2, 1/4, 1/8, respectively.
Min : (1 – n / 2) × t_{CYC} – 10
Max : (1 – n / 2) × t_{CYC} + 10

*3 : The values assume a gear cycle of × 1.
When a gear cycle of 1/2, 1/4, or 1/8 is specified, substitute “n” in the following equations with 1/2, 1/4, 1/8, respectively
Min : n / 2 × t_{CYC} – 10
Max : n / 2 × t_{CYC} + 10

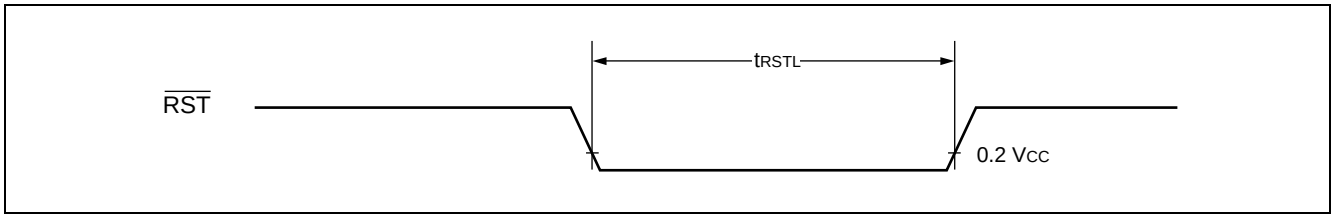
Clock output timing



(3) Reset Input

(V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V, Ta = –30 °C to +70 °C)

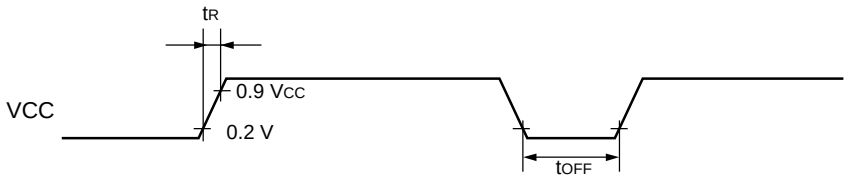
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	—	$t_{CP} \times 5$	—	ns	



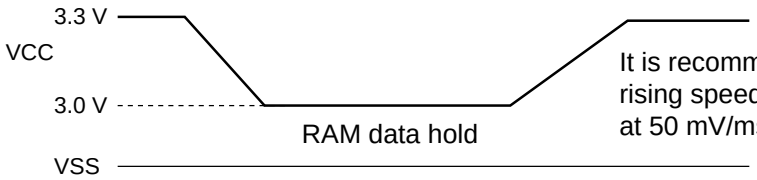
(4) Power-on reset

(V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V, Ta = –30 °C to +70 °C)

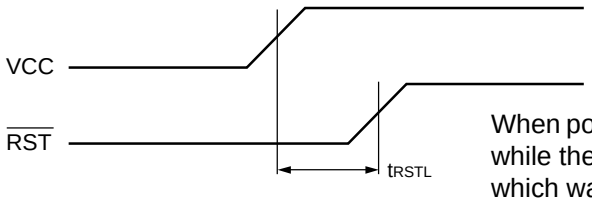
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Power rising time	t_R	VCC	V_{CC} = 3.3 V	—	20	ms	V_{CC} is less than 0.2 V before power is turned on.
Power supply cutoff time	t_{OFF}	VCC	—	2	—	ms	



Sudden change of power supply voltage may activate the power-on reset function.
To change the power supply voltage while the device is in operation, it is recommended to rise the voltage smoothly to suppress fluctuations as shown below.



It is recommended to keep the rising speed of the supply voltage at 50 mV/ms or slower.



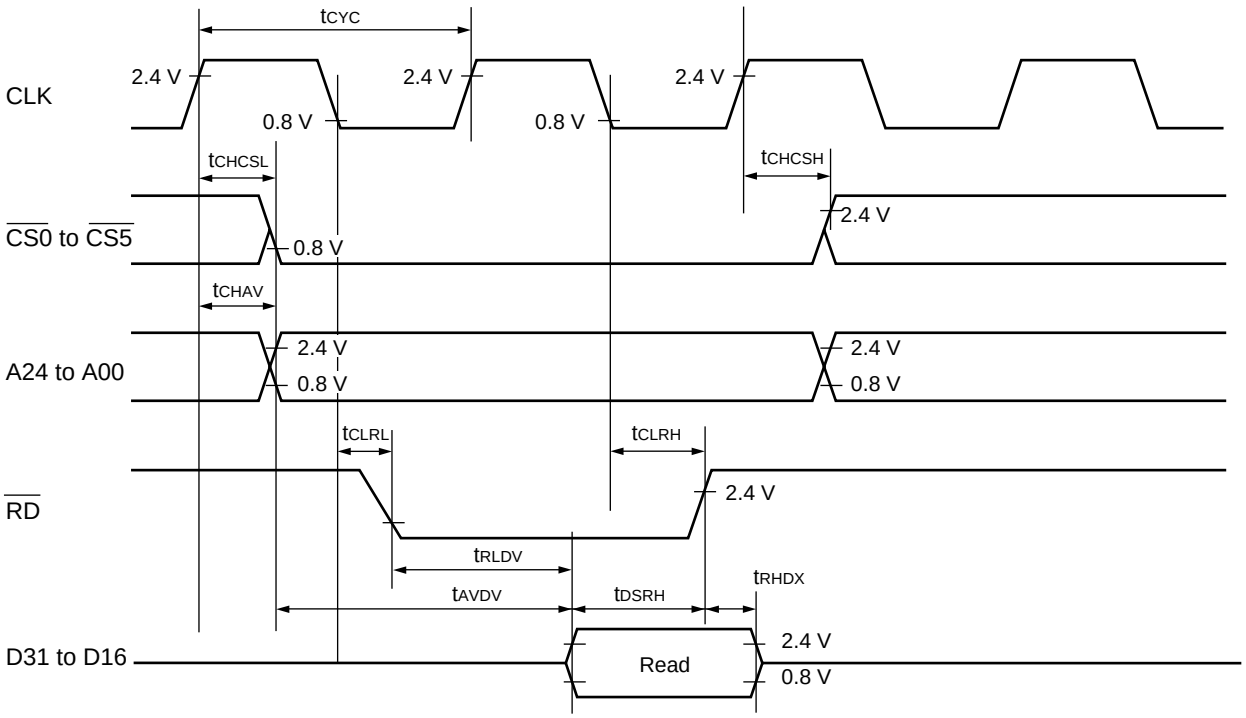
When power is turned on, it must be started while the $\overline{RST}$ pin is set to “L” level, after which wait for t_{RSTL} and change the level to “H” once the Vcc power level is reached.

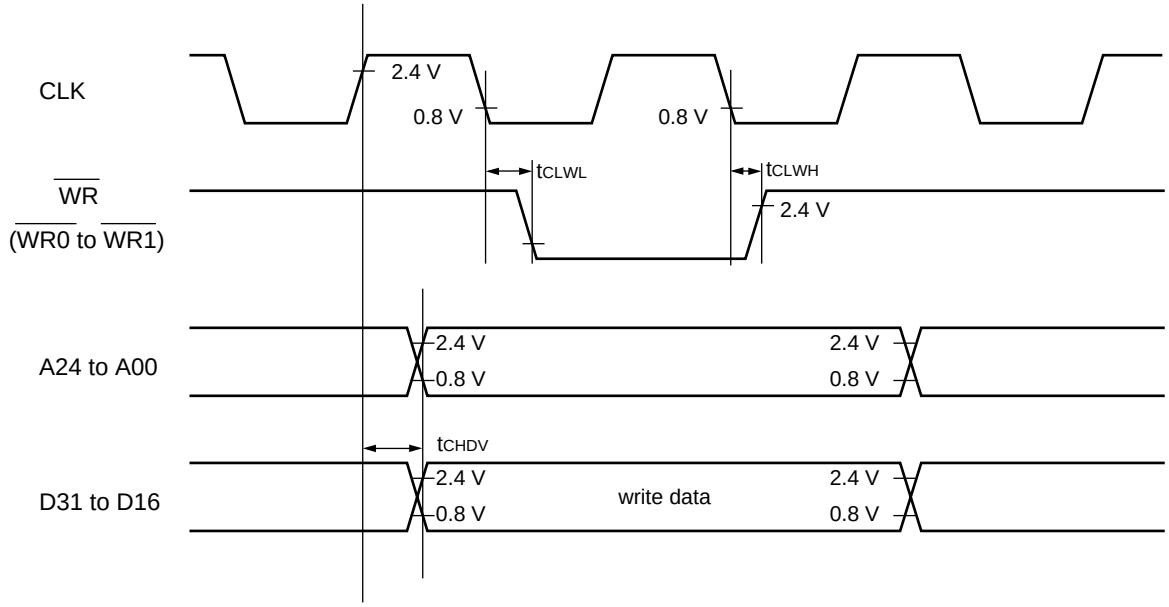
(5) Normal Bus Access Read/Write Operation

(V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V, Ta = –30 °C to +70 °C)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
CS0 to CS5 delay time	t_{CHCSL}	CLK, $\overline{CS0}$ to $\overline{CS5}$	—	—	15	ns	
	t_{CHCSH}			—	15	ns	
Address delay time	t_{CHAV}	CLK, A24 to A00		—	15	ns	
Data delay time	t_{CHDV}	CLK, D31 to D16		—	15	ns	
$\overline{RD}$ delay time	t_{CLRL}	CLK, $\overline{RD}$		—	15	ns	
	t_{CLRH}			—	15	ns	
$\overline{WR0}$, $\overline{WR1}$ delay time	t_{CLWL}	CLK, $\overline{WR0}$, $\overline{WR1}$		—	15	ns	
	t_{CLWH}			—	15	ns	
Valid address → valid data input time	t_{AVDV}	A24 to A00, D31 to D16		—	$3 / 2 \times t_{CYC} - 25$	ns	*
$\overline{RD}$ ↓ → valid data input time	t_{RLDV}	$\overline{RD}$, D31 to D16		—	$t_{CYC} - 25$	ns	*
Data set up → $\overline{RD}$ ↑ time	t_{DSRH}			25	—	ns	
$\overline{RD}$ ↑ → Data hold time	t_{RHDX}			0	—	ns	

* : When the bus timing is delayed by automatic wait insertion or RDY input, add the time (tcyc × the number of cycles added for the delay) to this rating.


tCYC
CLK
2.4 V
0.8 V
tCHCSL
tCHCSH
CS0 to CS5
tCHAV
A24 to A00
tCLRL
tCLRH
RD
tRLDV
tAVDV
tDSRH
tRHDX
D31 to D16
Read

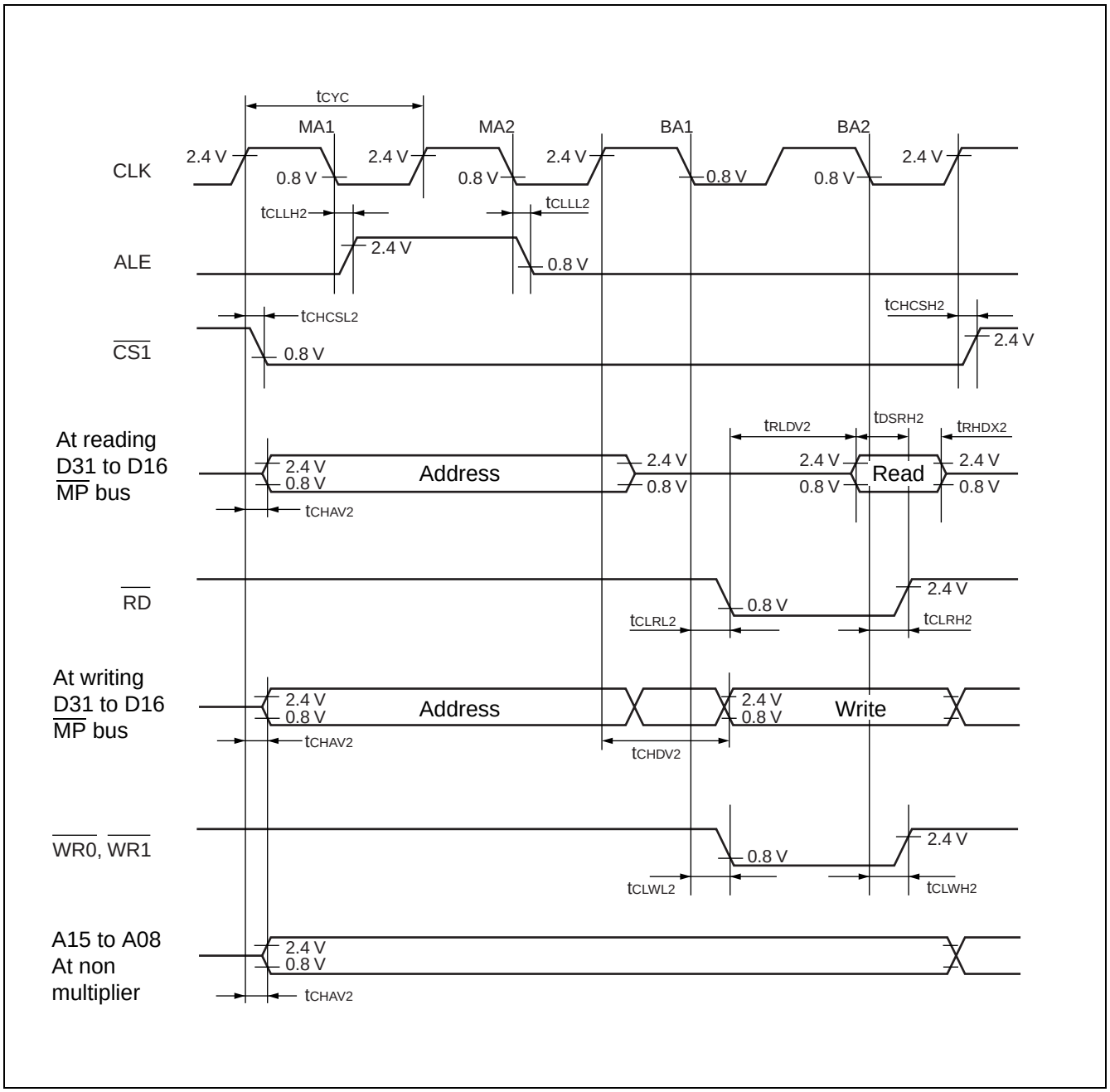

CLK
2.4 V
0.8 V
tCLWL
tCLWH
WR
(WR0 to WR1)
A24 to A00
tCHDV
D31 to D16
write data

(6) Timeshared Bus Access Read/Write Operations

(V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V, Ta = –30 °C to +70 °C)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ALE delay time	t_{CLLH2}	CLK, ALE	—	—	10	—	
	t_{CLLL2}			—	10	—	
$\overline{CS1}$ delay time	t_{CHCSL2}	CLK, $\overline{CS1}$		—	15	—	
	t_{CHCSH2}			—	15	ns	
Address delay time	t_{CHAV2}	CLK, D31 to D16		—	15	ns	
Data delay time	t_{CHDV2}			—	15	ns	
$\overline{RD}$ delay time	t_{CLRL2}	CLK, $\overline{RD}$		—	10	ns	
	t_{CLRH2}			—	10	ns	
$\overline{WR0}$, $\overline{WR1}$ delay time	t_{CLWL2}	CLK, $\overline{WR0}$, $\overline{WR1}$		—	10	ns	
$\overline{WR0}$, $\overline{WR1}$ pulse width	t_{CLWH2}			—	10	ns	
$\overline{RD}$ ↓ → valid data input time	t_{RLDV2}	$\overline{RD}$, D31 to D16		—	t_{CYC} – 25	—	*
Data set up → $\overline{RD}$ ↑ time	t_{DSRH2}			25	—	ns	
$\overline{RD}$ ↑ → Data hold time	t_{RHDX2}			0	—	ns	

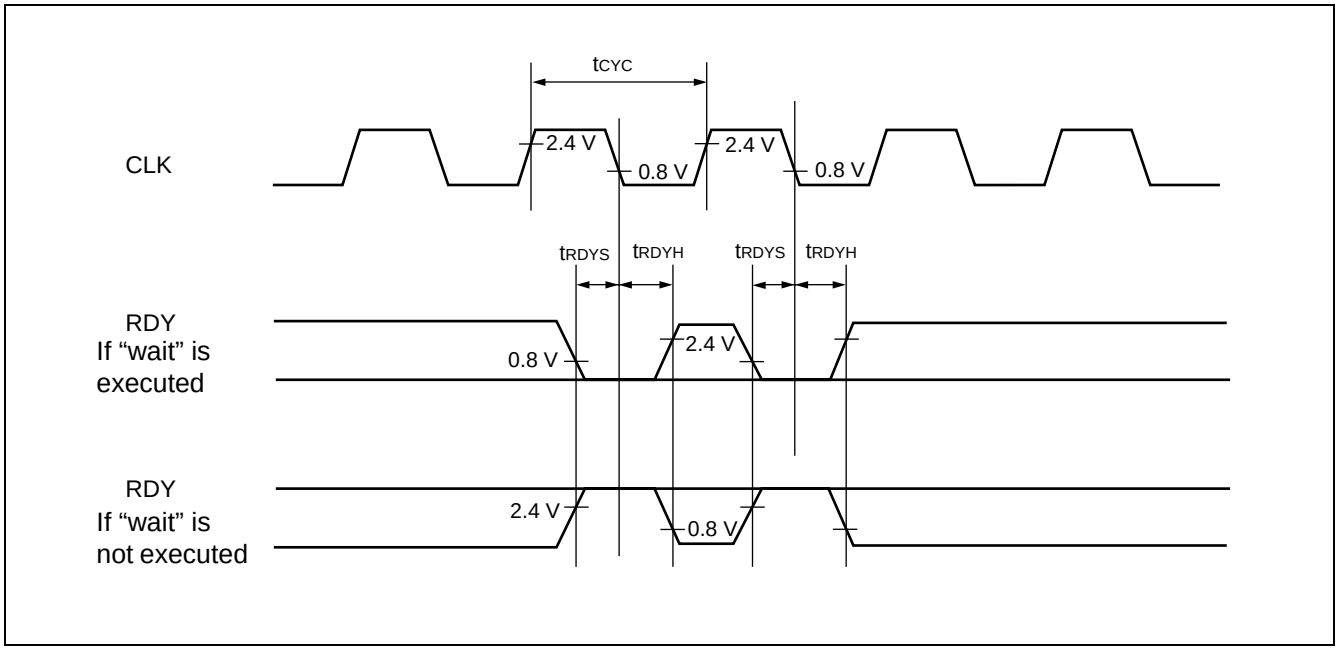
* : When the bus timing is delayed by automatic wait insertion or RDY input, add the time (tcyc × the number of cycles added for the delay) to this rating.


tCYC
MA1
MA2
BA1
BA2
CLK
2.4 V
0.8 V
tCLLH2
tCLLL2
ALE
tCHCSL2
tCHCSH2
CS1
At reading
D31 to D16
MP bus
tRLDV2
tDSRH2
tRHDX2
Address
Read
tCHAV2
RD
tCLRL2
tCLRH2
At writing
D31 to D16
MP bus
Write
tCHDV2
WR0, WR1
tCLWL2
tCLWH2
A15 to A08
At non
multiplier

(7) Ready Input Timing

(V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V, Ta = –30 °C to +70 °C)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
RDY setup time → CLK ↓	t_{RDYS}	CLK, RDY	—	15	—	ns	
CLK ↓ → RDY hold time	t_{RDYH}	CLK, RDY		0	—	ns	

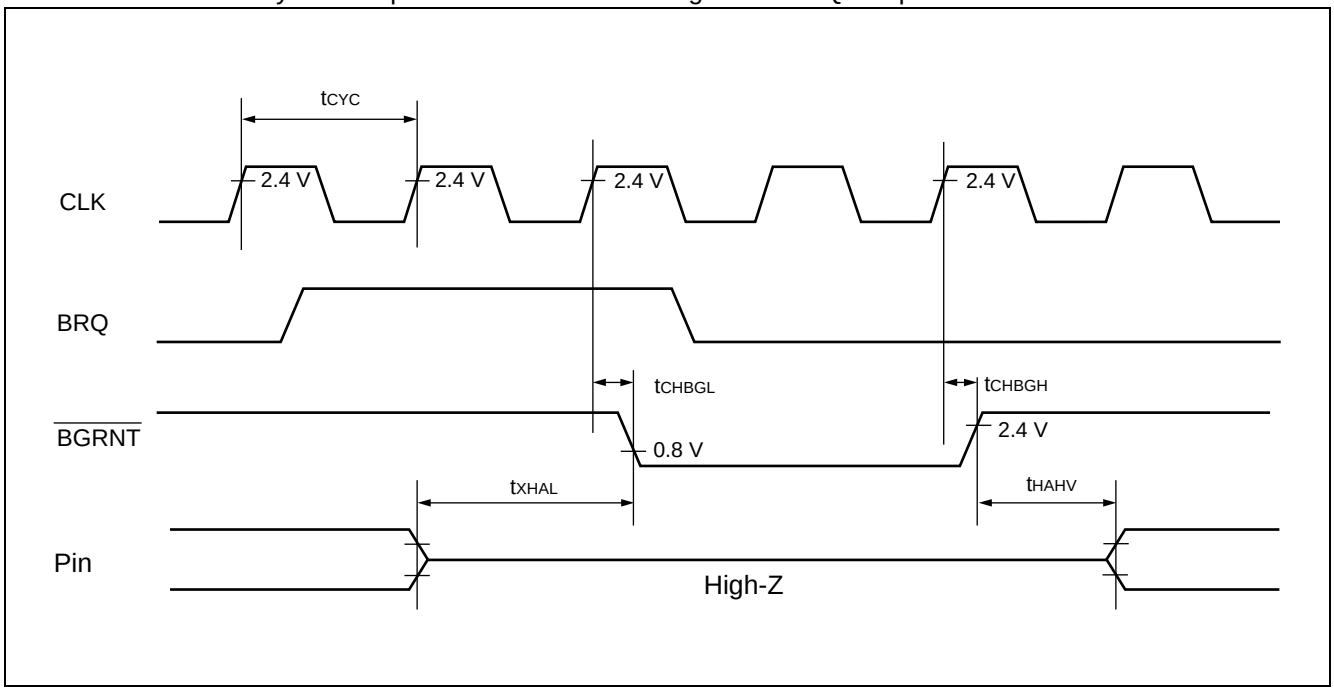


(8) Holding Timing

(V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V, Ta = –30 °C to +70 °C)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
$\overline{BGRNT}$ delay time	t_{CHBGL}	CLK, $\overline{BGRNT}$	—	—	10	ns	
	t_{CHBGH}			—	10	ns	
Pin floating → $\overline{BGRNT}$ ↓ time	t_{XHAL}	$\overline{BGRNT}$		t_{CYC} – 10	t_{CYC} + 10	ns	
$\overline{BGRNT}$ ↑ → Pin valid time	t_{HAHV}			t_{CYC} – 10	t_{CYC} + 10	ns	

Note : More than one cycle is required for $\overline{BGRNT}$ to change after BRQ is input.



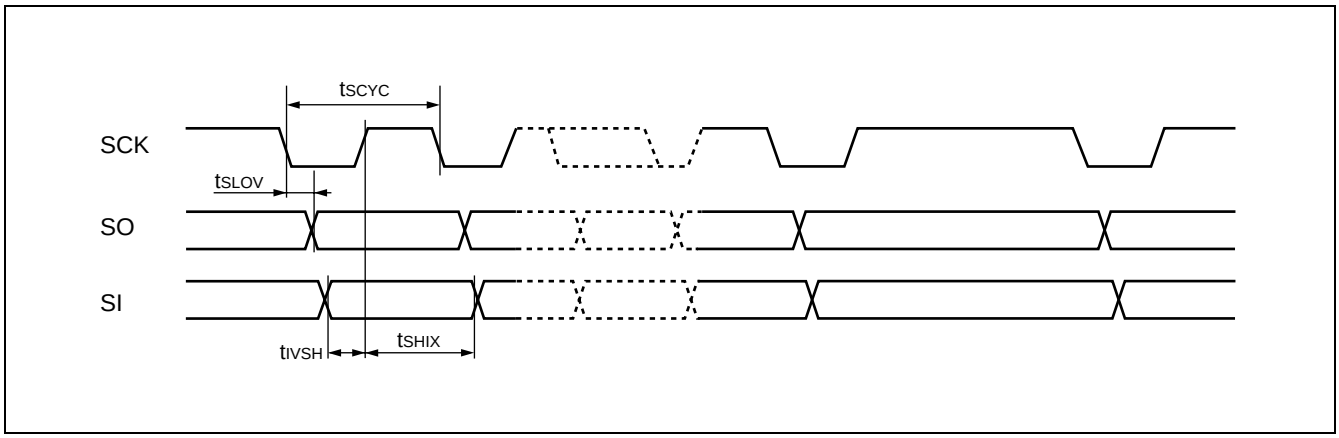
(9) UART Timing

(V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V, Ta = –30 °C to +70 °C)

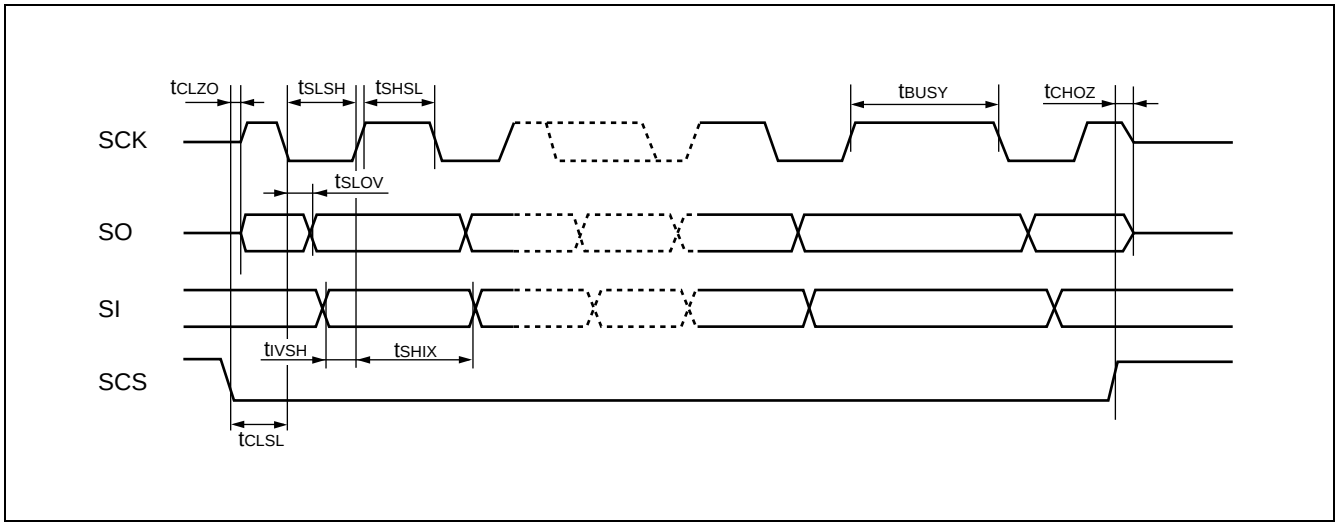
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	—	Internal shift clock mode	8 t_{CYCP}*	—	ns	
SCK ↓ → SO delay time	t_{SLOV}	—		– 10	+ 50	ns	
Valid SI → SCK ↑	t_{IVSH}	—		50	—	ns	
SCK ↑ → valid SI hold time	t_{SHIX}	—		50	—	ns	
Serial clock “H” pulse width	t_{SHSL}	—	External shift clock mode	4 t_{CYCP}* – 10	—	ns	
Serial clock “L” pulse width	t_{SLSH}	—		4 t_{CYCP}* – 10	—	ns	
SCK ↓ → SO delay time	t_{SLOV}	—		0	50	ns	
Valid SI → SCK ↑	t_{IVSH}	—		50	—	ns	
SCK ↑ → valid SI hold time	t_{SHIX}	—		50	—	ns	
Serial busy time	t_{BUSY}	—		—	6 t_{CYCP}*	ns	
SCS ↓ → SCK, SO delay time	t_{CLZO}	—		—	50	ns	
SCS ↓ → SCK input mask time	t_{CLSL}	—		—	3 t_{CYCP}*	ns	
SCS ↑ → SCK, SO High-Z time	t_{CHOZ}	—	—	50	—	ns	

* : t_{CYCP} : Peripheral clock cycle time

Internal shift clock mode



External shift clock mode

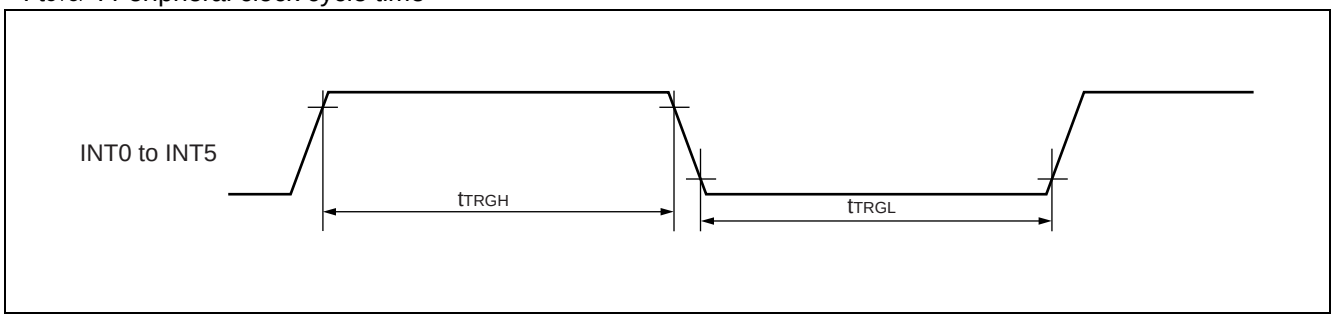


(10) Trigger Input Timing

(V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V, Ta = –30 °C to +70 °C)

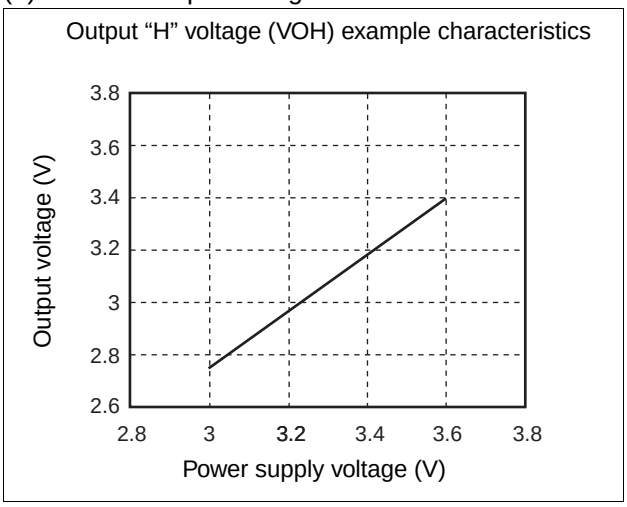
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH} t_{TRGL}	INT0 to INT5	—	5 t_{CYCP}*	—	ns	

* : t_{CYCP} : Peripheral clock cycle time

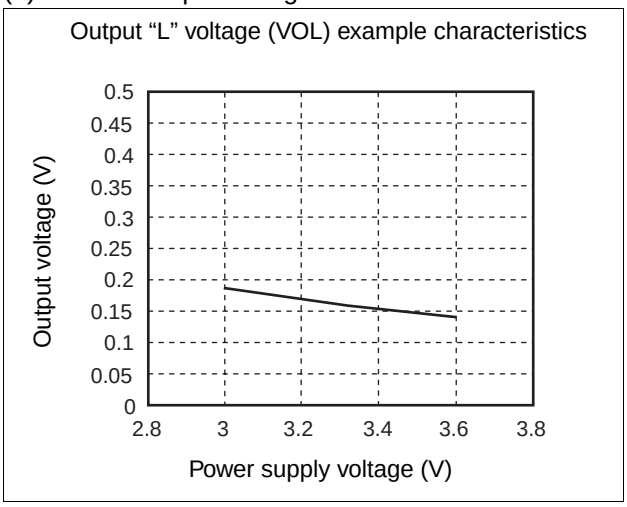


■ EXAMPLE CHARACTERISTICS

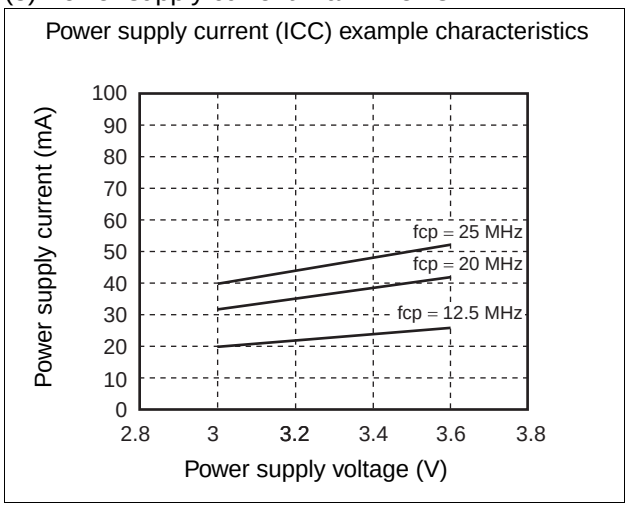
(1) “H” level output voltage Ta = +25 °C



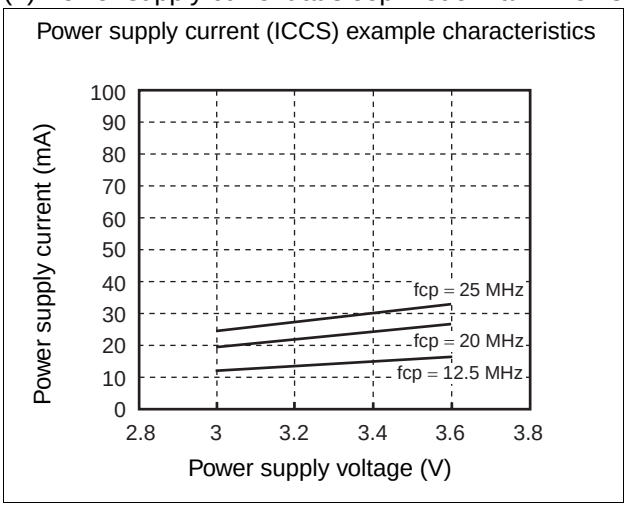
(2) “L” level output voltage Ta = +25 °C



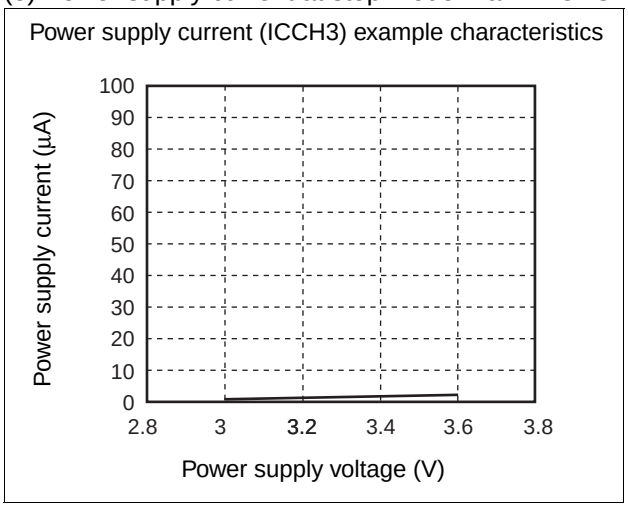
(3) Power supply current Ta = +25 °C



(4) Power supply current at sleep mode Ta = +25 °C



(5) Power supply current at stop mode Ta = +25 °C



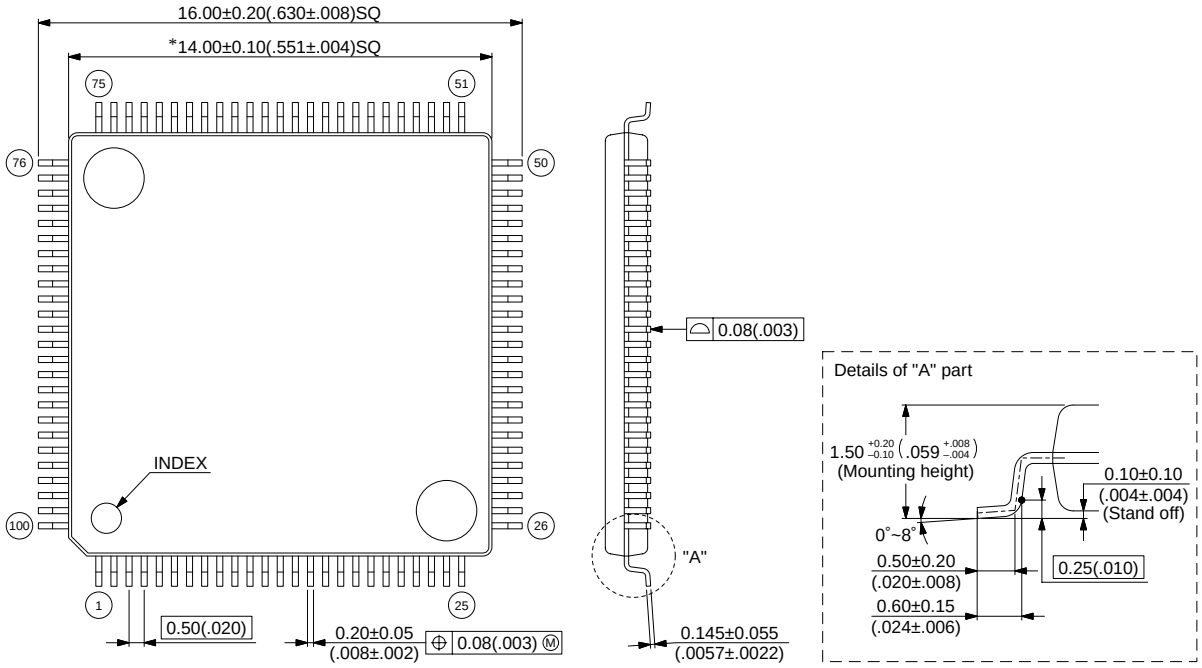
■ ORDERING INFORMATION

Part number	Package	Remarks
MB91126	100-pin Plastic LQFP (FPT-100P-M05)	

■ PACKAGE DIMENSION

100-pin Plastic LQFP
(FPT-100P-M05)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches)
Note : The values in parentheses are reference values.

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