Advance Information

DSP56364

24-Bit Audio Digital Signal Processor

The DSP56364 supports digital audio applications requiring sound field processing, acoustic equalization, and other digital audio algorithms. The DSP56364 uses the high performance, single-clock-per-cycle DSP56300 core family of programmable CMOS digital signal processors (DSPs) combined with the audio signal processing capability of the Motorola Symphony™ DSP family, as shown in **Figure 1**. This design provides a two-fold performance increase over Motorola's popular Symphony family of DSPs while retaining code compatibility. Significant architectural enhancements include a barrel shifter, 24-bit addressing, instruction cache, and direct memory access (DMA). The DSP56364 offers 100 million instructions per second (MIPS) using an internal 100 MHz clock at 3.3 V.

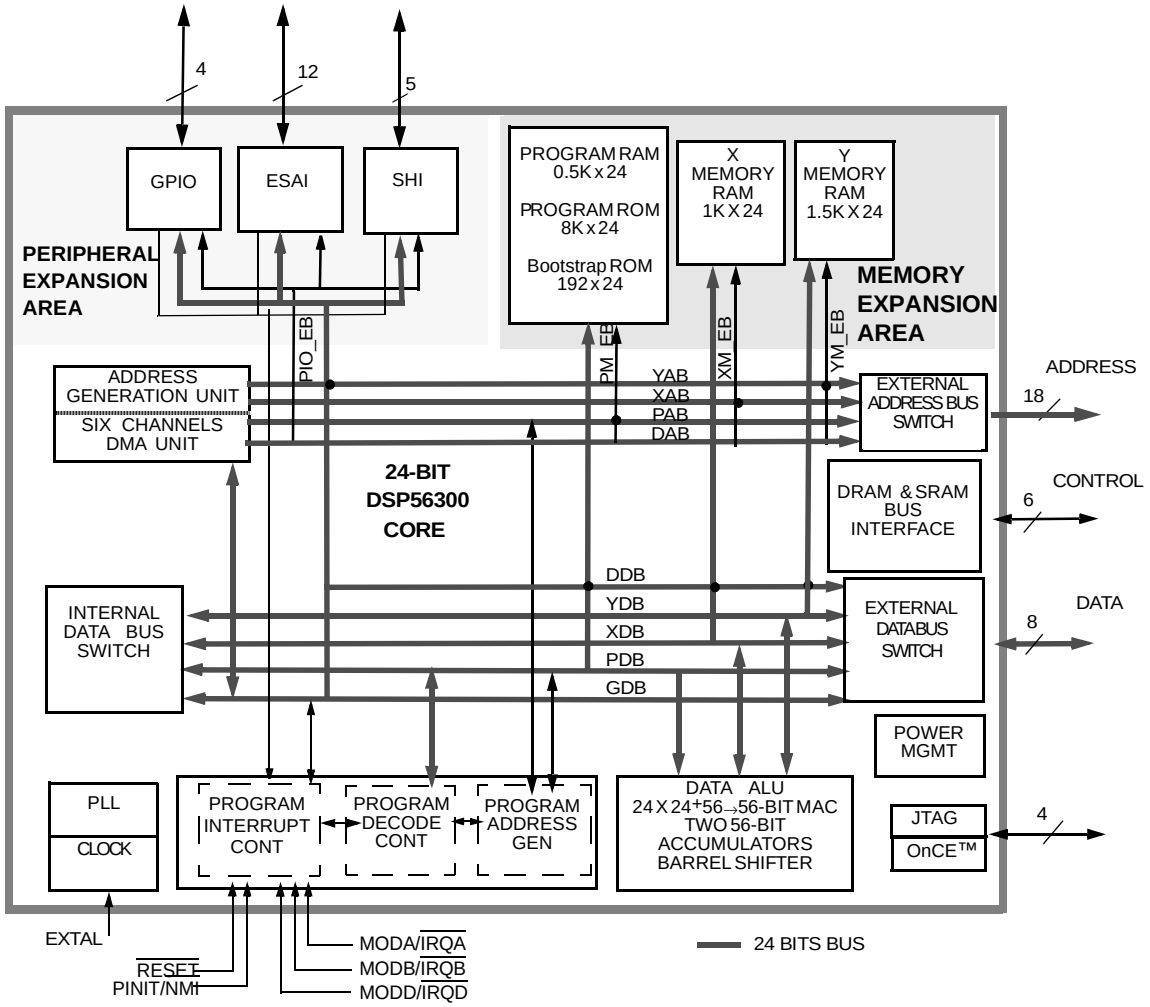


Figure 1 DSP56364 Block Diagram

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Advance Information

FOR TECHNICAL ASSISTANCE:

Telephone: 1-800-521-6274

Email: dsphelp@dsp.sps.mot.com

Internet: http://www.motorola-dsp.com

Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	Used to indicate a signal that is active when pulled low (For example, the $\overline{\text{RESET}}$ pin is active when low.)
"asserted"	Means that a high true (active high) signal is high or that a low true (active low) signal is low
"deasserted"	Means that a high true (active high) signal is low or that a low true (active low) signal is high

Examples:

Signal/Symbol	Logic State	Signal State	Voltage*
$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
PIN	True	Asserted	V_{IH}/V_{OH}
PIN	False	Deasserted	V_{IL}/V_{OL}

Note: *Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

FEATURES

Digital Signal Processing Core

- 100 Million Instructions Per Second (MIPS) with an 100 MHz clock at 3.3V.
- Object Code Compatible with the 56000 core.
- Data ALU with a 24 x 24 bit multiplier-accumulator and a 56-bit barrel shifter. 16-bit arithmetic support.
- Program Control with position independent code support and instruction cache support.
- Six-channel DMA controller.
- PLL based clocking with a wide range of frequency multiplications (1 to 4096), predivider factors (1 to 16) and power saving clock divider (2^i: i=0 to 7). Reduces clock noise.
- Internal address tracing support and OnCE™ for Hardware/Software debugging.
- JTAG port.
- Very low-power CMOS design, fully static design with operating frequencies down to DC.
- STOP and WAIT low-power standby modes.

On-chip Memory Configuration

- 1.5Kx24 Bit Y-Data RAM.
- 1Kx24 Bit X-Data RAM.
- 8Kx24 Bit Program ROM.
- 0.5Kx24 Bit Program RAM and 192x24 Bit Bootstrap ROM.
- 0.75Kx24 Bit from Y Data RAM can be switched to Program RAM resulting in up to 1.25Kx24 Bit of Program RAM.

Off-chip memory expansion

- External Memory Expansion Port with 8-bit data bus.
- Off-chip expansion up to 2 x 16M x 8-bit word of Data/Program memory when using DRAM.

- Off-chip expansion up to 2 x 256k x 8-bit word of Data/Program memory when using SRAM.
- Simultaneous glueless interface to SRAM and DRAM.

Peripheral modules

- Enhanced Serial Audio Interface (ESAI): 6 serial lines, 4 selectable as receive or transmitt and 2 transmitt only, master or slave. I^2S, Sony, AC97, network and other programmable protocols. Unused pins of ESAI may be used as GPIO lines.
- Serial Host Interface (SHI): SPI and I^2C protocols, 10-word receive FIFO, support for 8, 16 and 24-bit words.
- Four dedicated GPIO lines.

Packaging

- 100-pin plastic TQFP package.

DOCUMENTATION

Table 1 lists the documents that provide a complete description of the DSP56364 and are required to design properly with the part. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, a Motorola Literature Distribution Center, or through the Motorola DSP home page on the Internet (the source for the latest information).

Table 1 DSP56364 Documentation

Document Name	Description	Order Number
DSP56300 Family Manual	Detailed description of the 56000-family architecture and the 24-bit core processor and instruction set	DSP56300FM/AD
DSP56364 User's Manual	Detailed description of memory, peripherals, and interfaces	DSP56364UM/AD
DSP56364 Technical Data Sheet	Electrical and timing specifications; pin and package descriptions	DSP56364/D
There is also a product brief for this chip.		
DSP56364 Product Brief	Brief description of the chip	DSP56364P/D

SECTION 1

SIGNAL/CONNECTION DESCRIPTIONS

SIGNAL GROUPINGS

The input and output signals of the DSP56364 are organized into functional groups, which are listed in **Table 0-1.** and illustrated in **Figure 0-1.**.

The DSP56364 is operated from a 3.3 V supply; however, some of the inputs can tolerate 5 V. A special notice for this feature is added to the signal descriptions of those inputs.

Table 1-1. DSP56364 Functional Signal Groupings

Functional Group		Number of Signals	Detailed Description
Power (V_{CC})		18	**Table 0-2.**
Ground (GND)		14	**Table 0-3.**
Clock and PLL		3	**Table 0-4.**
Address bus	Port A[1]	18	**Table 0-5.**
Data bus		8	**Table 0-6.**
Bus control		6	**Table 0-7.**
Interrupt and mode control		4	**Table 0-8.**
General Purpose I/O	Port B2	4	Table 0-12
SHI		5	**Table 0-9.**
ESAI	Port C3	12	**Table 0-10.**
JTAG/OnCE Port		4	**Table 0-11.**

Notes:
1. Port A is the external memory interface port, including the external address bus, data bus, and control signals.
2. Port B signals are the GPIO signals.
3. Port C signals are the ESAI port signals multiplexed with the GPIO signals.

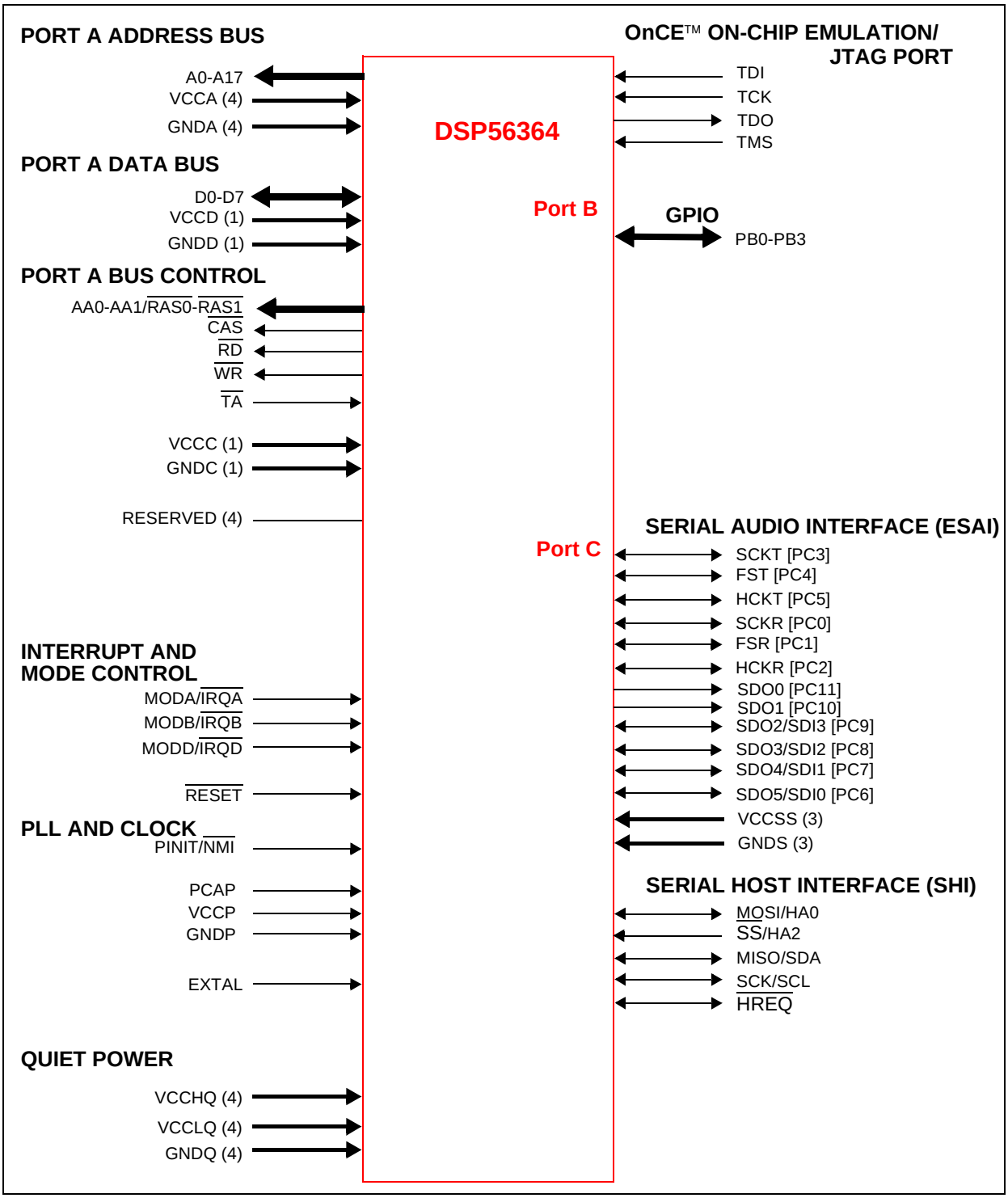


Figure 1-1. Signals Identified by Functional Group

POWER

Table 1-2. Power Inputs

Power Name	Description
V_{CCP}	**PLL Power**—V_{CCP} is V_{CC} dedicated for PLL use. The voltage should be well-regulated and the input should be provided with an extremely low impedance path to the V_{CC} power rail. There is one V_{CCP} input.
V_{CCQL} (4)	**Quiet Core (Low) Power—**V_{CCQL} is an isolated power for the internal processing logic. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There are four V_{CCQL} inputs.
V_{CCQH} (4)	**Quiet External (High) Power**—V_{CCQH} is a quiet power source for I/O lines. This input must be tied externally to all other chip power inputs. The user must provide adequate decoupling capacitors. There are four V_{CCQH} inputs.
V_{CCA} (4)	**Address Bus Power**—V_{CCA} is an isolated power for sections of the address bus I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There are four V_{CCA} inputs.
V_{CCD} (1)	**Data Bus Power**—V_{CCD} is an isolated power for sections of the data bus I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There is one V_{CCD} inputs.
V_{CCC} (1)	**Bus Control Power**—V_{CCC} is an isolated power for the bus control I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There is one V_{CCC} inputs.
V_{CCS} (3)	**SHI and ESAI** —V_{CCS} is an isolated power for the SHI and ESAI. This input must be tied externally to all other chip power inputs$_L$. The user must provide adequate external decoupling capacitors. There are three V_{CCS} inputs.

GROUND

Table 1-3. Grounds

Ground Name	Description
GND_P	**PLL Ground**—GND_P is ground-dedicated for PLL use. The connection should be provided with an extremely low-impedance path to ground. V_{CCP} should be bypassed to GND_P by a 0.47 µF capacitor located as close as possible to the chip package. There is one GND_P connection.
GND_Q (4)	**Quiet Ground**—GND_Q is an isolated ground for the internal processing logic. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are four GND_Q connections.
GND_A (4)	**Address Bus Ground**—GND_A is an isolated ground for sections of the address bus I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are four GND_A connections.
GND_D (1)	**Data Bus Ground**—GND_D is an isolated ground for sections of the data bus I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There is one GND_D connections.
GND_C (1)	**Bus Control Ground**—GND_C is an isolated ground for the bus control I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There is one GND_C connections.
GND_S (3)	**SHI and ESAI** —GND_S is an isolated ground for the SHI and ESAI. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are three GND_S connections.

CLOCK AND PLL

Table 1-4. Clock and PLL Signals

Signal Name	Type	State during Reset	Signal Description
EXTAL	Input	Input	**External Clock Input**—An external clock source must be connected to EXTAL in order to supply the clock to the internal clock generator and PLL.
PCAP	Input	Input	**PLL Capacitor**—PCAP is an input connecting an off-chip capacitor to the PLL filter. Connect one capacitor terminal to PCAP and the other terminal to V_{CCP}. If the PLL is not used, PCAP may be tied to V_{CC}, GND, or left floating.
PINIT/NMI	Input	Input	**PLL Initial/Nonmaskable Interrupt**—During assertion of RESET, the value of PINIT/NMI is written into the PLL Enable (PEN) bit of the PLL control register, determining whether the PLL is enabled or disabled. After RESET de assertion and during normal instruction processing, the PINIT/NMI Schmitt-trigger input is a negative-edge-triggered nonmaskable interrupt (NMI) request internally synchronized to internal system clock. *This input is 5 V tolerant.*

EXTERNAL MEMORY EXPANSION PORT (PORT A)

When the DSP56364 enters a low-power standby mode (stop or wait), it tri-states the relevant port A signals: D0–D7, AA0, AA1, RD, WR, CAS.

External Address Bus

Table 1-5. External Address Bus Signals

Signal Name	Type	State during Reset	Signal Description
A0–A17	Output	Keeper active	**Address Bus**—A0–A17 are active-high outputs that specify the address for external program and data memory accesses. Otherwise, the signals are kept to their previous values by internal weak keepers. To minimize power dissipation, A0–A17 do not change state when external memory spaces are not being accessed.

External Data Bus

Table 1-6. External Data Bus Signals

Signal Name	Type	State during Reset	Signal Description
D0–D7	Input/ Output	Tri-stated	**Data Bus**—D0–D7 are active-high, bidirectional input/ outputs that provide the bidirectional data bus for external program and data memory accesses. D0–D7 are tri-stated during hardware reset and when the DSP is in the stop or wait low-power standby mode.

External Bus Control

Table 1-7. External Bus Control Signals

Signal Name	Type	State during Reset	Signal Description
AA0–AA1/RAS0–RAS1	Output	Tri-stated	**Address Attribute or Row Address Strobe**—When defined as AA, these signals can be used as chip selects or additional address lines. When defined as RAS, these signals can be used as RAS for DRAM interface. These signals are tri-statable outputs with programmable polarity. These signals are tri-stated during hardware reset and when the DSP is in the stop or wait low-power standby mode.
CAS	Output	Tri-stated	**Column Address Strobe**— CAS is an active-low output used by DRAM to strobe the column address. This signal is tri-stated during hardware reset and when the DSP is in the stop or wait low-power standby mode.
RD	Output	Tri-stated	**Read Enable**—RD is an active-low output that is asserted to read external memory on the data bus. This signal is tri-stated during hardware reset and when the DSP is in the stop or wait low-power standby mode.
WR	Output	Tri-stated	**Write Enable**— WR is an active-low output that is asserted to write external memory on the data bus. This signal is tri-stated during hardware reset and when the DSP is in the stop or wait low-power standby mode.
TA	Input	Ignored Input	**Transfer Acknowledge**—If there is no external bus activity, the TA input is ignored. The TA input is a data transfer acknowledge (DTACK) function that can extend an external bus cycle indefinitely. Any number of wait states (1, 2. . .infinity) may be added to the wait states inserted by the BCR by keeping TA deasserted. In typical operation, TA is deasserted at the start of a bus cycle, is asserted to enable completion of the bus cycle, and is deasserted before the next bus cycle. The current bus cycle completes one clock period after TA is asserted synchronous to the internal system clock. The number of wait states is determined by the TA input or by the bus control register (BCR), whichever is longer. The BCR can be used to set the minimum number of wait states in external bus cycles. In order to use the TA functionality, the BCR must be programmed to at least one wait state. A zero wait state access cannot be extended by TA deassertion, otherwise improper operation may result. TA can operate synchronously or asynchronously, depending on the setting of the TAS bit in the operating mode register (OMR). TA functionality may not be used while performing DRAM type accesses, otherwise improper operation may result.

INTERRUPT AND MODE CONTROL

The interrupt and mode control signals select the chip's operating mode as it comes out of hardware reset. After RESET is deasserted, these inputs are hardware interrupt request lines.

Table 1-8. Interrupt and Mode Control

Signal Name	Type	State during Reset	Signal Description
MODA/IRQA	Input	Input	**Mode Select A/External Interrupt Request A—**MODA/IRQA is an active-low Schmitt-trigger input, internally synchronized to the internal system clock. MODA/IRQA selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. MODA, MODB, and MODD select one of 8 initial chip operating modes, latched into the OMR when the RESET signal is deasserted. If IRQA is asserted synchronous to the internal system clock, multiple processors can be re synchronized using the WAIT instruction and asserting IRQA to exit the wait state. If the processor is in the stop standby state and IRQA is asserted, the processor will exit the stop state. *This input is 5 V tolerant*.
MODB/IRQB	Input	Input	**Mode Select B/External Interrupt Request B—**MODB/IRQB is an active-low Schmitt-trigger input, internally synchronized to the internal system clock. MODB/IRQB selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. MODA, MODB, and MODD select one of 8 initial chip operating modes, latched into OMR when the RESET signal is deasserted. If IRQB is asserted synchronous to the internal system clock, multiple processors can be re-synchronized using the WAIT instruction and asserting IRQB to exit the wait state. This input is 5 V tolerant.

Table 1-8. Interrupt and Mode Control (Continued)

Signal Name	Type	State during Reset	Signal Description
MODD/$\overline{\text{IRQD}}$	Input	Input	**Mode Select D/External Interrupt Request D**—MODD/$\overline{\text{IRQD}}$ is an active-low Schmitt-trigger input, internally synchronized to the internal system clock. MODD/$\overline{\text{IRQD}}$ selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. MODA, MODB, and MODD select one of 8 initial chip operating modes, latched into OMR when the $\overline{\text{RESET}}$ signal is deasserted. If $\overline{\text{IRQD}}$ is asserted synchronous to the internal system clock, multiple processors can be re synchronized using the WAIT instruction and asserting $\overline{\text{IRQD}}$ to exit the wait state. This input is 5 V tolerant.
$\overline{\text{RESET}}$	Input	Input	**Reset—**$\overline{\text{RESET}}$ is an active-low, Schmitt-trigger input. When asserted, the chip is placed in the reset state and the internal phase generator is reset. The Schmitt-trigger input allows a slowly rising input (such as a capacitor charging) to reset the chip reliably. When the $\overline{\text{RESET}}$ signal is deasserted, the initial chip operating mode is latched from the MODA, MODB, and MODD inputs. The $\overline{\text{RESET}}$ signal must be asserted during power up. A stable EXTAL signal must be supplied before deassertionof $\overline{\text{RESET}}$. *This input is 5 V tolerant*.

SERIAL HOST INTERFACE

The SHI has five I/O signals that can be configured to allow the SHI to operate in either SPI or I^2C mode.

Table 1-9. Serial Host Interface Signals

Signal Name	Signal Type	State during Reset	Signal Description
SCK	Input or output	Tri-stated	**SPI Serial Clock**—The SCK signal is an output when the SPI is configured as a master and a Schmitt-trigger input when the SPI is configured as a slave. When the SPI is configured as a master, the SCK signal is derived from the internal SHI clock generator. When the SPI is configured as a slave, the SCK signal is an input, and the clock signal from the external master synchronizes the data transfer. The SCK signal is ignored by the SPI if it is defined as a slave and the slave select (SS) signal is not asserted. In both the master and slave SPI devices, data is shifted on one edge of the SCK signal and is sampled on the opposite edge where data is stable. Edge polarity is determined by the SPI transfer protocol. **I^2C Serial Clock**—SCL carries the clock for I^2C bus transactions in the I^2C mode. SCL is a Schmitt-trigger input when configured as a slave and an open-drain output when configured as a master. SCL should be connected to V_{CC} through a pull-up resistor. This signal is tri-stated during hardware, software, and individual reset. Thus, there is no need for an external pull-up in this state. This input is 5 V tolerant.
SCL	Input or output		

Table 1-9. Serial Host Interface Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
MISO	Input or output	Tri-stated	**SPI Master-In-Slave-Out**—When the SPI is configured as a master, MISO is the master data input line. The MISO signal is used in conjunction with the MOSI signal for transmitting and receiving serial data. This signal is a Schmitt-trigger input when configured for the SPI Master mode, an output when configured for the SPI Slave mode, and tri-stated if configured for the SPI Slave mode when $\overline{SS}$ is deasserted. An external pull-up resistor is not required for SPI operation. **I^{2}C Data and Acknowledge**—In I^{2}C mode, SDA is a Schmitt-trigger input when receiving and an open-drain output when transmitting. SDA should be connected to V_{CC} through a pull-up resistor. SDA carries the data for I^{2}C transactions. The data in SDA must be stable during the high period of SCL. The data in SDA is only allowed to change when SCL is low. When the bus is free, SDA is high. The SDA line is only allowed to change during the time SCL is high in the case of start and stop events. A high-to-low transition of the SDA line while SCL is high is a unique situation, and is defined as the start event. A low-to-high transition of SDA while SCL is high is a unique situation defined as the stop event. This signal is tri-stated during hardware, software, and individual reset. Thus, there is no need for an external pull-up in this state. This input is 5 V tolerant.
SDA	Input or open-drain output		
MOSI	Input or output	Tri-stated	**SPI Master-Out-Slave-In**—When the SPI is configured as a master, MOSI is the master data output line. The MOSI signal is used in conjunction with the MISO signal for transmitting and receiving serial data. MOSI is the slave data input line when the SPI is configured as a slave. This signal is a Schmitt-trigger input when configured for the SPI Slave mode. **I^{2}C Slave Address 0**—This signal uses a Schmitt-trigger input when configured for the I^{2}C mode. When configured for I^{2}C slave mode, the HA0 signal is used to form the slave device address. HA0 is ignored when configured for the I^{2}C master mode. This signal is tri-stated during hardware, software, and individual reset. Thus, there is no need for an external pull-up in this state. This input is 5 V tolerant.
HA0	Input		

Table 1-9. Serial Host Interface Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
$\overline{SS}$ **HA2**	Input	Input	**SPI Slave Select**—This signal is an active low Schmitt-trigger input when configured for the SPI mode. When configured for the SPI Slave mode, this signal is used to enable the SPI slave for transfer. When configured for the SPI master mode, this signal should be kept deasserted (pulled high). If it is asserted while configured as SPI master, a bus error condition is flagged. If $\overline{SS}$ is deasserted, the SHI ignores SCK clocks and keeps the MISO output signal in the high-impedance state. **I^2C Slave Address 2**—This signal uses a Schmitt-trigger input when configured for the I^2C mode. When configured for the I^2C Slave mode, the HA2 signal is used to form the slave device address. HA2 is ignored in the I^2C master mode. This signal is tri-stated during hardware, software, and individual reset. Thus, there is no need for an external pull-up in this state. *This input is 5 V tolerant.*
$\overline{HREQ}$	Input or Output	Tri-stated	**Host Request**—This signal is an active low Schmitt-trigger input when configured for the master mode but an active low output when configured for the slave mode. When configured for the slave mode, $\overline{HREQ}$ is asserted to indicate that the SHI is ready for the next data word transfer and deasserted at the first clock pulse of the new data word transfer. When configured for the master mode, $\overline{HREQ}$ is an input. When asserted by the external slave device, it will trigger the start of the data word transfer by the master. After finishing the data word transfer, the master will await the next assertion of $\overline{HREQ}$ to proceed to the next transfer. This signal is tri-stated during hardware, software, personal reset, or when the HREQ1–HREQ0 bits in the HCSR are cleared. There is no need for external pull-up in this state. *This input is 5 V toler*ant.

ENHANCED SERIAL AUDIO INTERFACE

Table 1-10. Enhanced Serial Audio Interface Signals

Signal Name	Signal Type	State during Reset	Signal Description
HCKR PC2	Input or output Input, output, or disconnected	GPIO disconnected	**High Frequency Clock for Receiver**—When programmed as an input, this signal provides a high frequency clock source for the ESAI receiver as an alternate to the DSP core clock. When programmed as an output, this signal can serve as a high-frequency sample clock (e.g., for external digital to analog converters [DACs]) or as an additional system clock. **Port C 2**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. *This input is 5 V tolerant.*
HCKT PC5	Input or output Input, output, or disconnected	GPIO disconnected	**High Frequency Clock for Transmitter**—When programmed as an input, this signal provides a high frequency clock source for the ESAI transmitter as an alternate to the DSP core clock. When programmed as an output, this signal can serve as a high frequency sample clock (e.g., for external DACs) or as an additional system clock. **Port C 5**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.

Table 1-10. Enhanced Serial Audio Interface Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
FSR PC1	Input or output Input, output, or disconnected	GPIO disconnected	**Frame Sync for Receiver**—This is the receiver frame sync input/output signal. In the asynchronous mode (SYN=0), the FSR pin operates as the frame sync input or output used by all the enabled receivers. In the synchronous mode (SYN=1), it operates as either the serial flag 1 pin (TEBE=0), or as the transmitter external buffer enable control (TEBE=1, RFSD=1). When this pin is configured as serial flag pin, its direction is determined by the RFSD bit in the RCCR register. When configured as the output flag OF1, this pin will reflect the value of the OF1 bit in the SAICR register, and the data in the OF1 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF1, the data value at the pin will be stored in the IF1 bit in the SAISR register, synchronized by the frame sync in normal mode or the slot in network mode. **Port C 1**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.
FST PC4	Input or output Input, output, or disconnected	GPIO disconnected	**Frame Sync for Transmitter**—This is the transmitter frame sync input/output signal. For synchronous mode, this signal is the frame sync for both transmitters and receivers. For asynchronous mode, FST is the frame sync for the transmitters only. The direction is determined by the transmitter frame sync direction (TFSD) bit in the ESAI transmit clock control register (TCCR). **Port C 4**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.

Table 1-10. Enhanced Serial Audio Interface Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
SCKR	Input or output	GPIO disconnected	**Receiver Serial Clock**—SCKR provides the receiver serial bit clock for the ESAI. The SCKR operates as a clock input or output used by all the enabled receivers in the asynchronous mode (SYN=0), or as serial flag 0 pin in the synchronous mode (SYN=1). When this pin is configured as serial flag pin, its direction is determined by the RCKD bit in the RCCR register. When configured as the output flag OF0, this pin will reflect the value of the OF0 bit in the SAICR register, and the data in the OF0 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF0, the data value at the pin will be stored in the IF0 bit in the SAISR register, synchronized by the frame sync in normal mode or the slot in network mode.
PC0	Input, output, or disconnected		**Port C 0**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.
SCKT	Input or output	GPIO disconnected	**Transmitter Serial Clock**—This signal provides the serial bit rate clock for the ESAI. SCKT is a clock input or output used by all enabled transmitters and receivers in synchronous mode, or by all enabled transmitters in asynchronous mode.
PC3	Input, output, or disconnected		**Port C 3**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.

Table 1-10. Enhanced Serial Audio Interface Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
SDO5	Output	GPIO disconnected	**Serial Data Output 5**—When programmed as a transmitter, SDO5 is used to transmit data from the TX5 serial transmit shift register.
SDI0	Input		**Serial Data Input 0**—When programmed as a receiver, SDI0 is used to receive serial data into the RX0 serial receive shift register.
PC6	Input, output, or disconnected		**Port C 6**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.
SDO4	Output	GPIO disconnected	**Serial Data Output 4**—When programmed as a transmitter, SDO4 is used to transmit data from the TX4 serial transmit shift register.
SDI1	Input		**Serial Data Input 1**—When programmed as a receiver, SDI1 is used to receive serial data into the RX1 serial receive shift register.
PC7	Input, output, or disconnected		**Port C 7**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.

Table 1-10. Enhanced Serial Audio Interface Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
SDO3 SDI2 PC8	Output Input Input, output, or disconnected	GPIO disconnected	**Serial Data Output 3**—When programmed as a transmitter, SDO3 is used to transmit data from the TX3 serial transmit shift register. **Serial Data Input 2**—When programmed as a receiver, SDI2 is used to receive serial data into the RX2 serial receive shift register. **Port C 8**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.
SDO2 SDI3 PC9	Output Input Input, output, or disconnected	GPIO disconnected	**Serial Data Output 2**—When programmed as a transmitter, SDO2 is used to transmit data from the TX2 serial transmit shift register **Serial Data Input 3**—When programmed as a receiver, SDI3 is used to receive serial data into the RX3 serial receive shift register. **Port C 9**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.
SDO1 PC10	Output Input, output, or disconnected	GPIO disconnected	**Serial Data Output 1**—SDO1 is used to transmit data from the TX1 serial transmit shift register. **Port C 10**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.

Table 1-10. Enhanced Serial Audio Interface Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
SDO0 PC11	Output Input, output, or disconnected	GPIO disconnected	**Serial Data Output 0**—SDO0 is used to transmit data from the TX0 serial transmit shift register. **Port C 11**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.

JTAG/OnCE INTERFACE

Table 1-11. JTAG/OnCE Interface

Signal Name	Signal Type	State during Reset	Signal Description
TCK	Input	Input	**Test Clock**—TCK is a test clock input signal used to synchronize the JTAG test logic. It has an internal pull-up resistor. *This input is 5 V tolerant.*
TDI	Input	Input	**Test Data Input**—TDI is a test data serial input signal used for test instructions and data. TDI is sampled on the rising edge of TCK and has an internal pull-up resistor. This input is 5 V tolerant.
TDO	Output	Tri-stated	**Test Data Output**—TDO is a test data serial output signal used for test instructions and data. TDO is tri-statable and is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCK.
TMS	Input	Input	**Test Mode Select**—TMS is an input signal used to sequence the test controller's state machine. TMS is sampled on the rising edge of TCK and has an internal pull-up resistor. This input is 5 V tolerant.

Table 1-12. GPIO Signals

Signal Name	Signal Type	State during Reset	Signal Description
GPIO0-GPIO3	Input, output or disconnected	disconnected	GPIO0-3- The General Purpose I/O pins are used for control and handshake functions between the DSP and external circuitry. Each Port B GPIO pin may be individually programmed as an input, output or disconnected

SECTION 2

SPECIFICATIONS

INTRODUCTION

The DSP56364 is a high density CMOS device with Transistor-Transistor Logic (TTL) compatible inputs and outputs. The DSP56364 specifications are preliminary and are from design simulations, and may not be fully tested or guaranteed. Finalized specifications will be published after full characterization and device qualifications are complete.

MAXIMUM RATINGS

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields. However, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability of operation is enhanced if unused inputs are pulled to an appropriate logic voltage level (e.g., either GND or V_{CC}). The suggested value for a pullup or pulldown resistor is 10 kΩ.

Note: In the calculation of timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a “maximum” value for a specification will never occur in the same device that has a “minimum” value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2-1. Maximum Ratings

Rating[1]	Symbol	Value[1, 2]	Unit
Supply Voltage	V_{CC}	–0.3 to +4.0	V
All input voltages excluding “5 V tolerant” inputs[3]	V_{IN}	GND -0.3 to V_{CC} + 0.3	V
All “5 V tolerant” input voltages[3]	V_{IN5}	GND – 0.3 to V_{CC} + 3.95	V
Current drain per pin excluding V_{CC} and GND	I	10	mA
Operating temperature range	T_J	-40 to +105	°C
Storage temperature	T_{STG}	–55 to +125	°C

Notes:
1. GND = 0 V, V_{CC} = 3.3 V ± 0.16 V, T_J = –0°C to +105°C, CL = 50 pF
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the maximum rating may affect device reliability or cause permanent damage to the device.
3. **CAUTION**: All “5 V Tolerant” input voltages must not be more than 3.95 V greater than the supply voltage; this restriction applies to “power on”, as well as during normal operation. In any case, the input voltages cannot be more than 5.75 V. “5 V Tolerant” inputs are inputs that tolerate 5 V.

THERMAL CHARACTERISTICS

Table 2-2. Thermal Characteristics

Characteristic	Symbol	TQFP Value	Unit
Junction-to-ambient thermal resistance[1]	$R_{\theta JA}$ or θ_{JA}	49.87	°C/W
Junction-to-case thermal resistance[2]	$R_{\theta JC}$ or θ_{JC}	9.26	°C/W
Thermal characterization parameter	Ψ_{JT}	2.0	°C/W

Notes:
1. Junction-to-ambient thermal resistance is based on measurements on a horizontal single-sided printed circuit board per SEMI G38-87 in natural convection.(SEMI is Semiconductor Equipment and Materials International, 805 East Middlefield Rd., Mountain View, CA 94043, (415) 964-5111.) Measurements were done with parts mounted on thermal test boards conforming to specification EIA/JESD51-3.
2. Junction-to-case thermal resistance is based on measurements using a cold plate per SEMI G30-88, with the exception that the cold plate temperature is used for the case temperature.

DC ELECTRICAL CHARACTERISTICS

Table 2-3. DC Electrical Characteristics[6]

Characteristics	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	3.14	3.3	3.46	V
Input high voltage • D(0:7), $\overline{TA}$	V_{IH}	2.0	—	V_{CC}	V
• MOD[1]/$\overline{IRQ}$[1], $\overline{RESET}$, PINIT/$\overline{NMI}$ and all JTAG/ESAI/GPIO/SHI (SPI mode)pins	V_{IHP}	2.0	—	V_{CC} + 3.95	
• SHI (I2C mode) pins	V_{IHP}	1.5	—	V_{CC} + 3.95	
• EXTAL[8]	V_{IHX}	$0.8 \times V_{CC}$	—	V_{CC}	
Input low voltage • D(0:7), $\overline{TA}$, MOD[1]/$\overline{IRQ}$[1], $\overline{RESET}$, PINIT	V_{IL}	–0.3	—	0.8	V
• JTAG/ESAI/GPIO/SHI (SPI mode)pins	V_{ILP}	–0.3	—	0.8	
• SHI (I2C mode) pins	V_{ILP}	-0.3	—	$0.3xV_{CC}$	
• EXTAL[8]	V_{ILX}	–0.3	—	$0.2 \times V_{CC}$	
Input leakage current	I_{IN}	–10	—	10	µA
High impedance (off-state) input current (@ 2.4 V / 0.4 V)	I_{TSI}	–10	—	10	µA
Output high voltage • TTL (I_{OH} = –0.4 mA)[5,7]	V_{OH}	2.4	—	—	V
• CMOS (I_{OH} = –10 µA)[5]		V_{CC} – 0.01	—	—	V
Output low voltage • TTL (I_{OL} = 3.0 mA, open-drain pins I_{OL} = 6.7 mA)[5,7]	V_{OL}	—	—	0.4	V
• CMOS (I_{OL} = 10 µA)[5]		—	—	0.01	
Internal supply current[2] at internal clock of 100Mhz • In Normal mode	I_{CCI}	—	127	181	mA
• In Wait mode[3]	I_{CCW}	—	7. 5	11	mA
• In Stop mode[4]	I_{CCS}	—	100	150	µA

Table 2-3. DC Electrical Characteristics[6] (Continued)

Characteristics	Symbol	Min	Typ	Max	Unit
PLL supply current		—	1	2.5	mA
Input capacitance[5]	C_{IN}	—	—	10	pF

Notes:
1. Refers to MODA/$\overline{\text{IRQA}}$, MODB/$\overline{\text{IRQB}}$, and MODD/$\overline{\text{IRQD}}$ pins
2. **Power Consumption Considerations** on page 4-4 provides a formula to compute the estimated current requirements in Normal mode. In order to obtain these results, all inputs must be terminated (i.e., not allowed to float). Measurements are based on synthetic intensive DSP benchmarks. The power consumption numbers in this specification are 90% of the measured results of this benchmark. This reflects typical DSP applications. Typical internal supply current is measured with V_{CC} = 3.3 V at T_J = 105°C. Maximum internal supply current is measured with V_{CC} = 3.46 V at T_J = 105°C.
3. In order to obtain these results, all inputs must be terminated (i.e., not allowed to float). PLL signal is disabled during Stop state.
4. In order to obtain these results, all inputs, which are not disconnected at Stop mode, must be terminated (i.e., not allowed to float).
5. Periodically sampled and not 100% tested
6. V_{CC} = 3.3 V ± .16 V; T_J = 0°C to +105°C, C_L = 50 pF
7. This characteristic does not apply to PCAP.
8. Driving EXTAL to the low V_{IHX} or the high V_{ILX} value may cause additional power consumption (DC current). To minimize power consumption, the minimum V_{IHX} should be no lower than $0.9 \times V_{CC}$ and the maximum V_{ILX} should be no higher than $0.1 \times V_{CC}$.

AC ELECTRICAL CHARACTERISTICS

The timing waveforms shown in the AC electrical characteristics section are tested with a V_{IL} maximum of 0.3 V and a V_{IH} minimum of 2.4 V for all pins except EXTAL, which is tested using the input levels shown in **Note 8** of the previous table. AC timing specifications, which are referenced to a device input signal, are measured in production with respect to the 50% point of the respective input signal's transition. DSP56364 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.4 V and 2.4 V, respectively.

Note: Although the minimum value for the frequency of EXTAL is 0 MHz, the device AC test conditions are 15 MHz and rated speed.

INTERNAL CLOCKS

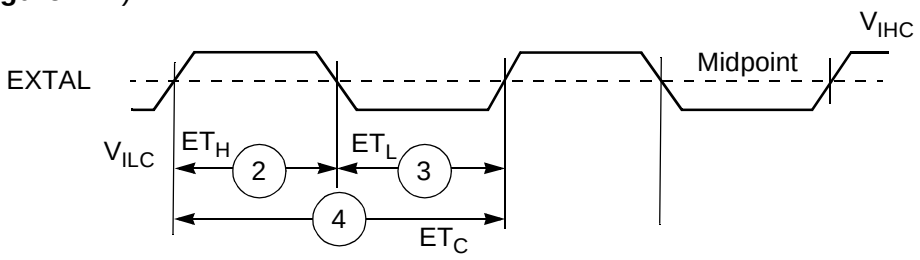
Table 2-4. Internal Clocks

Characteristics	Symbol	Expression[1, 2]		
		Min	Typ	Max
Internal operation frequency with PLL enabled	f	—	(Ef × MF)/ (PDF × DF)	—
Internal operation frequency with PLL disabled	f	—	Ef/2	—
Internal clock high period • With PLL disabled • With PLL enabled and MF ≤ 4 • With PLL enabled and MF > 4	T_H	— 0.49 × ET_C × PDF × DF/MF 0.47 × ET_C × PDF × DF/MF	ET_C — —	— 0.51 × ET_C × PDF × DF/MF 0.53 × ET_C × PDF × DF/MF
Internal clock low period • With PLL disabled • With PLL enabled and MF ≤ 4 • With PLL enabled and MF > 4	T_L	— 0.49 × ET_C × PDF × DF/MF 0.47 × ET_C × PDF × DF/MF	ET_C — —	— 0.51 × ET_C × PDF × DF/MF 0.53 × ET_C × PDF × DF/MF
Internal clock cycle time with PLL enabled	T_C	—	ET_C × PDF × DF/MF	—
Internal clock cycle time with PLL disabled	T_C	—	2 × ET_C	—
Instruction cycle time	I_{CYC}	—	T_C	—

Notes: 1. DF = Division Factor
Ef = External frequency
ET_C = External clock cycle
MF = Multiplication Factor
PDF = Predivision Factor
T_C = internal clock cycle
2. See the **PLL and Clock Generation** section in the *DSP56300 Family Manual* for a detailed discussion of the PLL.

EXTERNAL CLOCK OPERATION

The DSP56364 system clock is an externally supplied square wave voltage source connected to EXTAL(**Figure 2-1.**).



Note: The midpoint is 0.5 (V_{IHC} + V_{ILC}).

Figure 2-1. External Clock Timing

Table 2-5. Clock Operation

No.	Characteristics	Symbol	Min	Max
1	Frequency of EXTAL (EXTAL Pin Frequency) The rise and fall time of this external clock should be 3 ns maximum.	Ef	0	100.0
2	EXTAL input high[1, 2] • With PLL disabled (46.7%–53.3% duty cycle[6]) • With PLL enabled (42.5%–57.5% duty cycle[6])	ET_H	4.67 ns 4.25 ns	∞ 157.0 µs
3	EXTAL input low[1, 2] • With PLL disabled (46.7%–53.3% duty cycle[6]) • With PLL enabled (42.5%–57.5% duty cycle[6])	ET_L	4.67 ns 4.25 ns	∞ 157.0 µs
4	EXTAL cycle time[2] • With PLL disabled • With PLL enabled	ET_C	10.00 ns 10.00 ns	∞ 273.1 µs

Notes: 1. Measured at 50% of the input transition
2. The maximum value for PLL enabled is given for minimum V_{CO} and maximum MF.

PHASE LOCK LOOP (PLL) CHARACTERISTICS

Table 2-6. PLL Characteristics

Characteristics	Min	Max	Unit
V_{CO} frequency when PLL enabled ($MF \times E_f \times 2/PDF$)	30	200	MHz
PLL external capacitor (PCAP pin to V_{CCP}) (C_{PCAP}[1)] • @ $MF \leq 4$ • @ $MF > 4$	 $(MF \times 580) - 100$ $MF \times 830$	 $(MF \times 780) - 140$ $MF \times 1470$	pF

Notes: 1. C_{PCAP} is the value of the PLL capacitor (connected between the PCAP pin and V_{CCP}). The recommended value in pF for C_{PCAP} can be computed from one of the following equations:
(MF x 680)-120, for $MF \leq 4$, or
MF x 1100, for $MF > 4$.

RESET, STOP, MODE SELECT, AND INTERRUPT TIMING

Table 2-7. Reset, Stop, Mode Select, and Interrupt Timing[6]

No.	Characteristics	Expression	Min	Max	Unit
8	Delay from $\overline{\text{RESET}}$ assertion to all pins at reset value[3]	—	—	26.0	ns
9	Required $\overline{\text{RESET}}$ duration[4]				
	• Power on, external clock generator, PLL disabled	$50 \times ET_C$	500.0	—	ns
	• Power on, external clock generator, PLL enabled	$1000 \times ET_C$	10.0	—	ns
	• Power on, internal oscillator	$75000 \times ET_C$	0.75	—	µs
	• During STOP, XTAL disabled (PCTL Bit 16 = 0)	$75000 \times ET_C$	0.75	—	ms
	• During STOP, XTAL enabled (PCTL Bit 16 = 1)	$2.5 \times T_C$	25.0	—	ms
	• During normal operation	$2.5 \times T_C$	25.0	—	ns
10	Delay from asynchronous $\overline{\text{RESET}}$ deassertion to first external address output (internal reset deassertion)[5]				
	• Minimum	$3.25 \times T_C + 2.0$	34.5	—	ns
	• Maximum	$20.25\ T_C + 7.50$	—	211.5	ns
13	Mode select setup time		30.0	—	ns
14	Mode select hold time		0.0	—	ns
15	Minimum edge-triggered interrupt request assertion width		6.6	—	ns
16	Minimum edge-triggered interrupt request deassertion width		6.6	—	ns
17	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to external memory access address out valid				
	• Caused by first interrupt instruction fetch	$4.25 \times T_C + 2.0$	44.5	—	ns
	• Caused by first interrupt instruction execution	$7.25 \times T_C + 2.0$	74.5	—	ns
18	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to general-purpose transfer output valid caused by first interrupt instruction execution	$10 \times T_C + 5.0$	105.0	—	ns

Table 2-7. Reset, Stop, Mode Select, and Interrupt Timing[6] (Continued)

No.	Characteristics	Expression	Min	Max	Unit
19	Delay from address output valid caused by first interrupt instruction execute to interrupt request deassertion for level sensitive fast interrupts[1]	$3.75 \times T_C + WS \times T_C - 10.94$	—	—	ns
20	Delay from $\overline{RD}$ assertion to interrupt request deassertion for level sensitive fast interrupts[1]	$3.25 \times T_C + WS \times T_C - 10.94$	—	—	ns
21	Delay from $\overline{WR}$ assertion to interrupt request deassertion for level sensitive fast interrupts[1]				ns
	• DRAM for all WS	$(WS + 3.5) \times T_C - 10.94$	—	—	
	• SRAM WS = 1	$(WS + 3.5) \times T_C - 10.94$	—	—	
	• SRAM WS = 2, 3	$(WS + 3) \times T_C - 10.94$	—	—	
	• SRAM WS ≥ 4	$(WS + 2.5) \times T_C - 10.94$	—	—	
24	Duration for $\overline{IRQA}$ assertion to recover from Stop state		5.9	—	
25	Delay from $\overline{IRQA}$ assertion to fetch of first instruction (when exiting Stop)[2, 3]				
	• PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is enabled (OMR Bit 6 = 0)	$PLC \times ET_C \times PDF + (128\ K - PLC/2) \times T_C$	1.3	13.6	ms
	• PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is not enabled (OMR Bit 6 = 1)	$PLC \times ET_C \times PDF + (23.75 \pm 0.5) \times T_C$	232.5 ns	12.3 ms	
	• PLL is active during Stop (PCTL Bit 17 = 1) (Implies No Stop Delay)	$(8.25 \pm 0.5) \times T_C$	77.5	87.5	ns
26	Duration of level sensitive $\overline{IRQA}$ assertion to ensure interrupt service (when exiting Stop)[2, 3]				
	• PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is enabled (OMR Bit 6 = 0)	$PLC \times ET_C \times PDF + (128K - PLC/2) \times T_C$	13.6	—	ms
	• PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is not enabled (OMR Bit 6 = 1)	$PLC \times ET_C \times PDF + (20.5 \pm 0.5) \times T_C$	12.3	—	ms
	• PLL is active during Stop (PCTL Bit 17 = 1) (implies no Stop delay)	$5.5 \times T_C$	55.0	—	ns

Table 2-7. Reset, Stop, Mode Select, and Interrupt Timing[6] (Continued)

No.	Characteristics	Expression	Min	Max	Unit
27	Interrupt Requests Rate				
	• ESAI, SCI	$12T_C$	—	120.0	ns
	• DMA	$8T_C$	—	80.0	ns
	• $\overline{\text{IRQ}}$, $\overline{\text{NMI}}$ (edge trigger)	$8T_C$	—	80.0	ns
	• $\overline{\text{IRQ}}$, $\overline{\text{NMI}}$ (level trigger)	$12T_C$	—	120.0	ns
28	DMA Requests Rate				
	• Data read from ESAI, SCI	$6T_C$	—	60.0	ns
	• Data write to ESAI, SCI	$7T_C$	—	70.0	ns
	• $\overline{\text{IRQ}}$, $\overline{\text{NMI}}$ (edge trigger)	$3T_C$	—	30.0	ns

Table 2-7. Reset, Stop, Mode Select, and Interrupt Timing[6] (Continued)

No.	Characteristics	Expression	Min	Max	Unit
29	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to external memory (DMA source) access address out valid	$4.25 \times T_C + 2.0$	44.0	—	ns

Notes:

1. When using fast interrupts and $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, and $\overline{\text{IRQD}}$ are defined as level-sensitive, timings 19 through 21 apply to prevent multiple interrupt service. To avoid these timing restrictions, the deasserted Edge-triggered mode is recommended when using fast interrupts. Long interrupts are recommended when using Level-sensitive mode.
2. This timing depends on several settings:

   For PLL disable, using internal oscillator (PLL Control Register (PCTL) Bit 16 = 0) and oscillator disabled during Stop (PCTL Bit 17 = 0), a stabilization delay is required to assure the oscillator is stable before executing programs. In that case, resetting the Stop delay (OMR Bit 6 = 0) will provide the proper delay. While it is possible to set OMR Bit 6 = 1, it is not recommended and these specifications do not guarantee timings for that case.

   For PLL disable, using internal oscillator (PCTL Bit 16 = 0) and oscillator enabled during Stop (PCTL Bit 17=1), no stabilization delay is required and recovery time will be minimal (OMR Bit 6 setting is ignored).

   For PLL disable, using external clock (PCTL Bit 16 = 1), no stabilization delay is required and recovery time will be defined by the PCTL Bit 17 and OMR Bit 6 settings.

   For PLL enable, if PCTL Bit 17 is 0, the PLL is shutdown during Stop. Recovering from Stop requires the PLL to get locked. The PLL lock procedure duration, PLL Lock Cycles (PLC), may be in the range of 0 to 1000 cycles. This procedure occurs in parallel with the stop delay counter, and stop recovery will end when the last of these two events occurs. The stop delay counter completes count or PLL lock procedure completion.

   PLC value for PLL disable is 0.

   The maximum value for ET_C is 4096 (maximum MF) divided by the desired internal frequency (i.e., for 100 MHz it is 4096/100 MHz = 40 µs). During the stabilization period, T_C, T_H, and T_L will not be constant, and their width may vary, so timing may vary as well.
3. Periodically sampled and not 100% tested
4. For an external clock generator, $\overline{\text{RESET}}$ duration is measured during the time in which $\overline{\text{RESET}}$ is asserted, V_{CC} is valid, and the EXTAL input is active and valid.

   For internal oscillator, $\overline{\text{RESET}}$ duration is measured during the time in which $\overline{\text{RESET}}$ is asserted and V_{CC} is valid. The specified timing reflects the crystal oscillator stabilization time after power-up. This number is affected both by the specifications of the crystal and other components connected to the oscillator and reflects worst case conditions.

   When the V_{CC} is valid, but the other "required $\overline{\text{RESET}}$ duration" conditions (as specified above) have not been yet met, the device circuitry will be in an uninitialized state that can result in significant power consumption and heat-up. Designs should minimize this state to the shortest possible duration.

Table 2-7. Reset, Stop, Mode Select, and Interrupt Timing[6] (Continued)

No.	Characteristics	Expression	Min	Max	Unit

5. For an external clock generator, RESET duration is measured during the time in which RESET is asserted, V_{CC} is valid, and the EXTAL input is active and valid.

   For internal oscillator, $\overline{\text{RESET}}$ duration is measured during the time in which $\overline{\text{RESET}}$ is asserted and V_{CC} is valid. The specified timing reflects the crystal oscillator stabilization time after power-up. This number is affected both by the specifications of the crystal and other components connected to the oscillator and reflects worst case conditions.

   When the V_{CC} is valid, but the other "required $\overline{\text{RESET}}$ duration" conditions (as specified above) have not been yet met, the device circuitry will be in an uninitialized state that can result in significant power consumption and heat-up. Designs should minimize this state to the shortest possible duration.
6. If PLL does not lose lock
7. V_{CC} = 3.3 V ± 0.16 V; T_J = 0°C to + 105°C, C_L = 50 pF
8. WS = number of wait states (measured in clock cycles, number of T_C)
9. Use expression to compute maximum value.

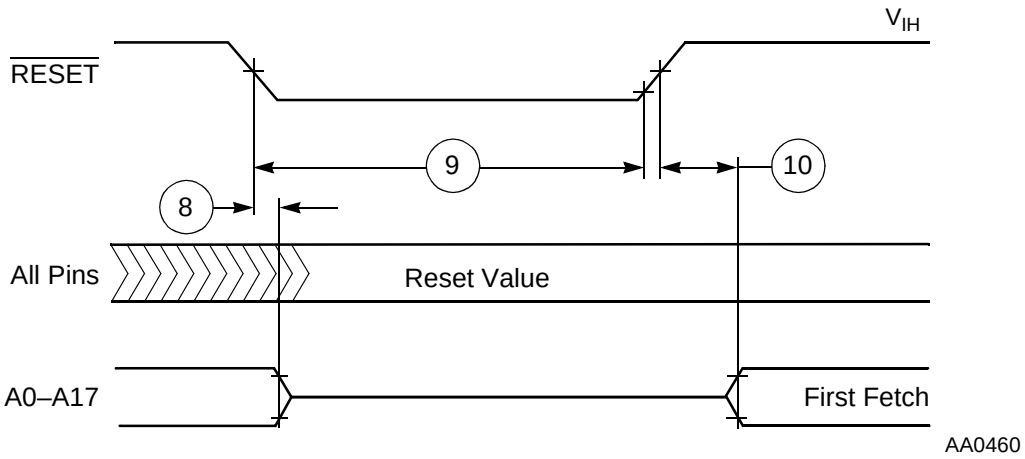


Figure 2-2. Reset Timing

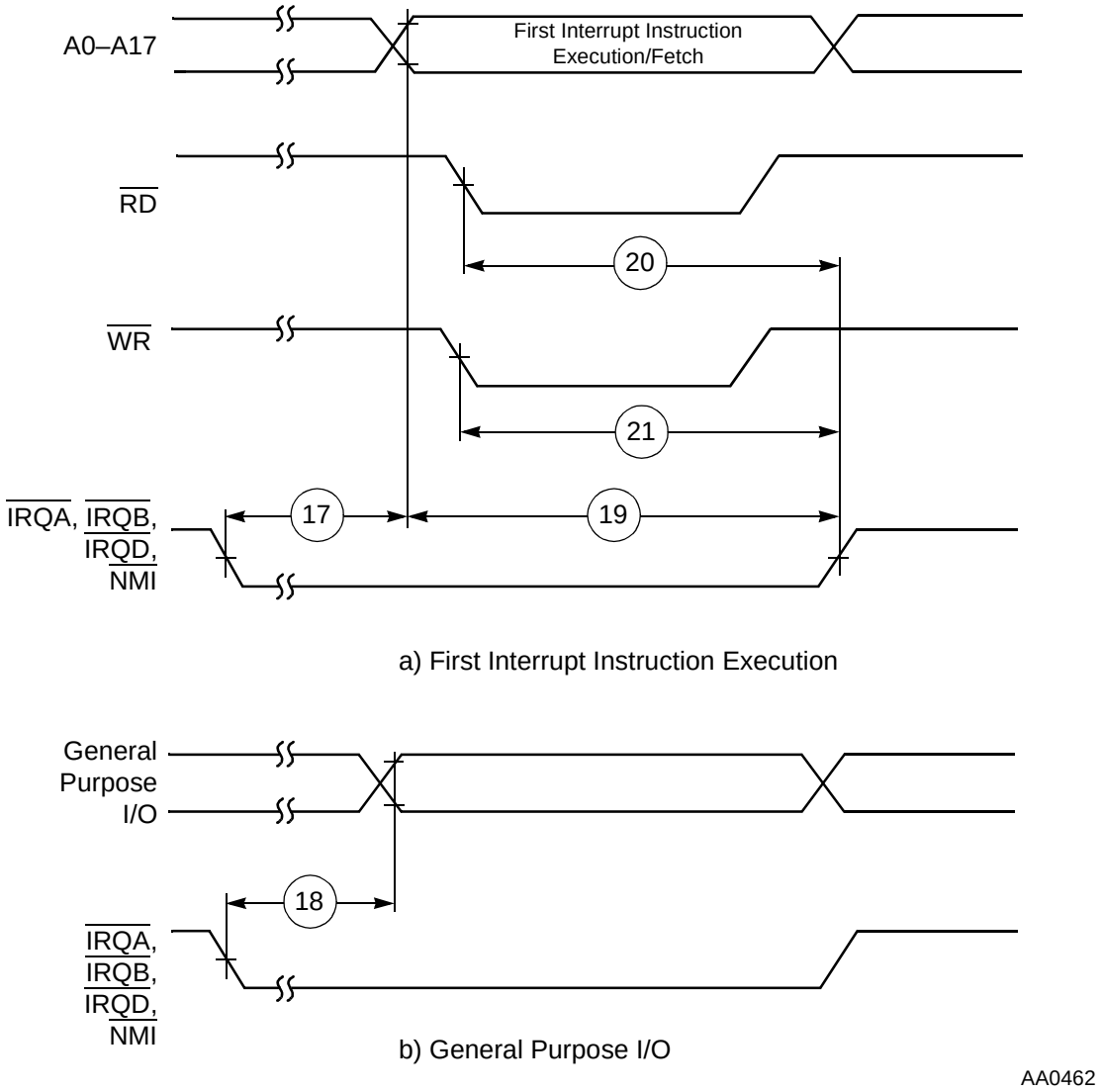


Figure 2-3. External Fast Interrupt Timing

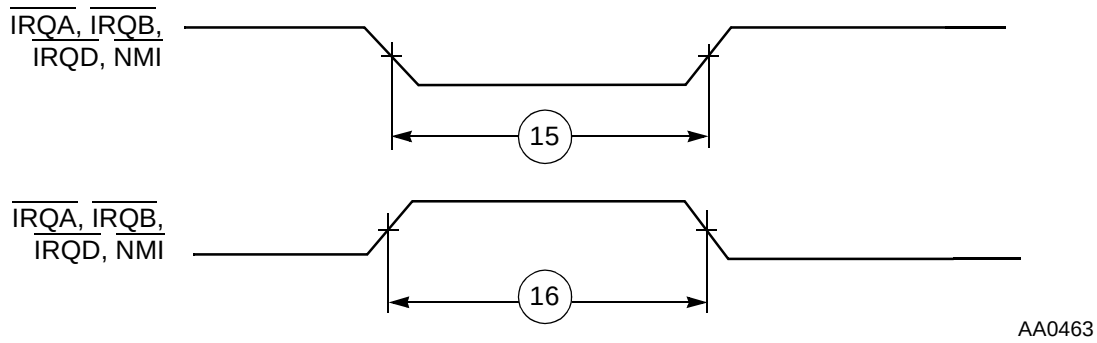


Figure 2-4. External Interrupt Timing (Negative Edge-Triggered)

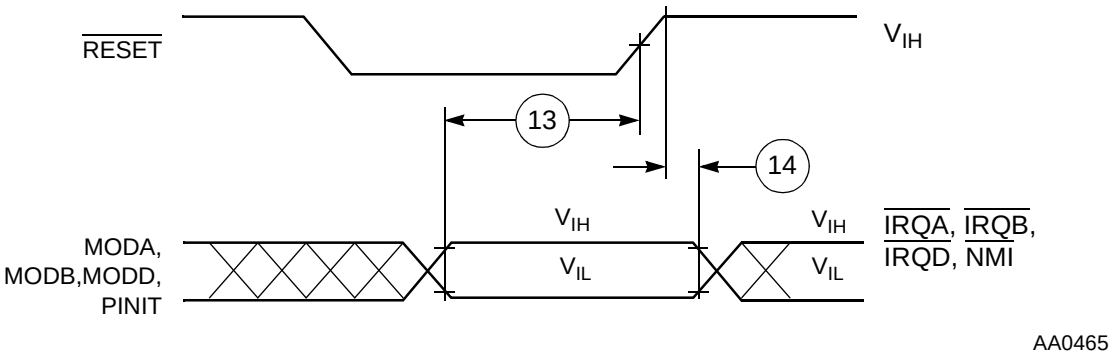


Figure 2-5. Operating Mode Select Timing

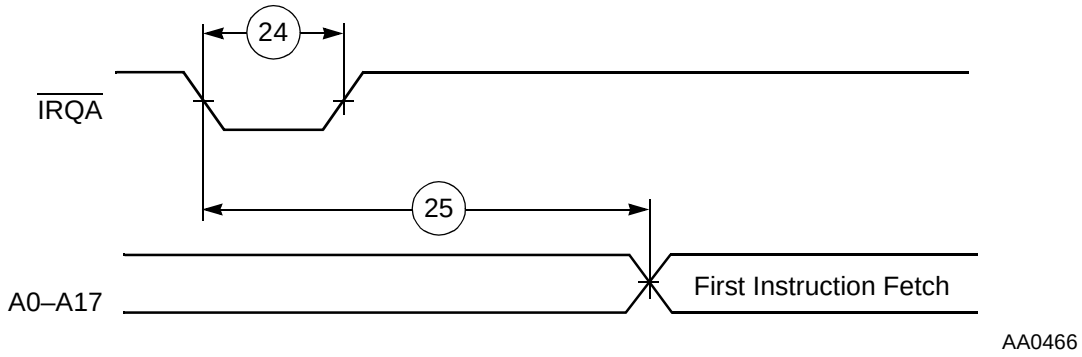


Figure 2-6. Recovery from Stop State Using IRQA

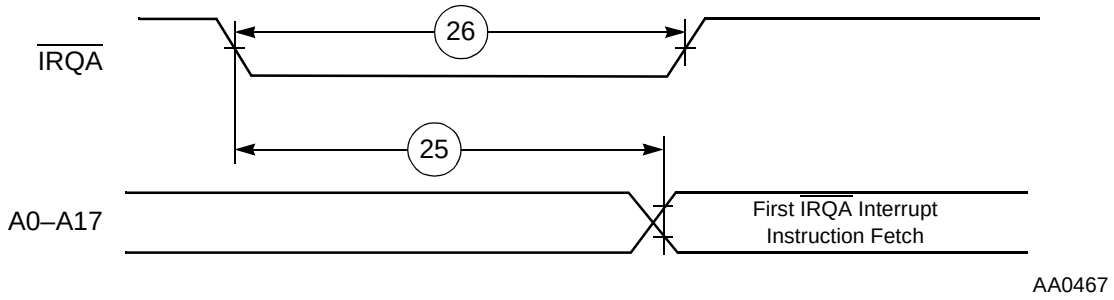


Figure 2-7. Recovery from Stop State Using IRQA Interrupt Service

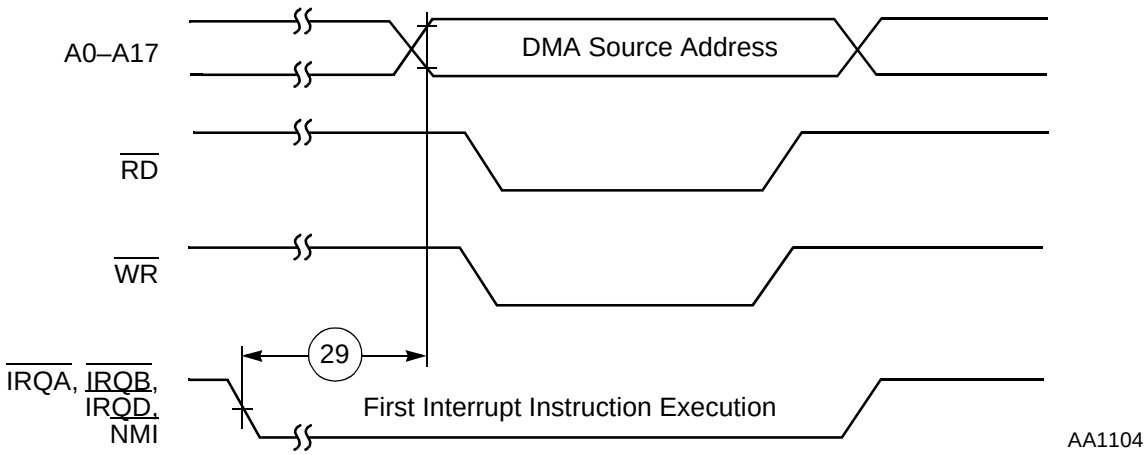


Figure 2-8. External Memory Access (DMA Source) Timing

EXTERNAL MEMORY EXPANSION PORT (PORT A)

SRAM Timing

Table 2-8. SRAM Read and Write Accesses[3]

No.	Characteristics	Symbol	Expression[1]	Min	Max	Unit
100	Address valid and AA assertion pulse width	t_{RC}, t_{WC}	$(WS + 1) \times T_C - 4.0$ [$1 \le WS \le 3$]	16.0	—	ns
			$(WS + 2) \times T_C - 4.0$ [$4 \le WS \le 7$]	56.0	—	ns
			$(WS + 3) \times T_C - 4.0$ [$WS \ge 8$]	106.0	—	ns
101	Address and AA valid to $\overline{WR}$ assertion	t_{AS}	$0.25 \times T_C - 2.0$ [$WS = 1$]	0.5	—	ns
			$0.75 \times T_C - 2.0$ [$2 \le WS \le 3$]	5.5	—	ns
			$1.25 \times T_C - 2.0$ [$WS \ge 4$]	10.5	—	ns
102	$\overline{WR}$ assertion pulse width	t_{WP}	$1.5 \times T_C - 4.0$ [$WS = 1$]	11.0	—	ns
			All frequencies: $WS \times T_C - 4.0$ [$2 \le WS \le 3$]	16.0	—	ns
			$(WS - 0.5) \times T_C - 4.0$ [$WS \ge 4$]	31.0	—	ns

Table 2-8. SRAM Read and Write Accesses[3] (Continued)

No.	Characteristics	Symbol	Expression[1]	Min	Max	Unit
103	$\overline{WR}$ deassertion to address not valid	t_{WR}	$0.25 \times T_C - 2.0$ [1 ≤ WS ≤ 3]	0.5	—	ns
			$1.25 \times T_C - 2.0$ [4 ≤ WS ≤ 7]	10.5	—	ns
			$2.25 \times T_C - 2.0$ [WS ≥ 8]	20.5	—	ns
			All frequencies: $1.25 \times T_C - 4.0$ [4 ≤ WS ≤ 7]	8.5	—	ns
			$2.25 \times T_C - 4.0$ [WS ≥ 8]	18.5	—	ns
104	Address and AA valid to input data valid	t_{AA}, t_{AC}	$(WS + 0.75) \times T_C - 7.0$ [WS ≥ 1]	—	10.5	ns
105	$\overline{RD}$ assertion to input data valid	t_{OE}	$(WS + 0.25) \times T_C - 7.0$ [WS ≥ 1]	—	5.5	ns
106	$\overline{RD}$ deassertion to data not valid (data hold time)	t_{OHZ}		0.0	—	ns
107	Address valid to $\overline{WR}$ deassertion[2]	t_{AW}	$(WS + 0.75) \times T_C - 4.0$ [WS ≥ 1]	13.5	—	ns
108	Data valid to $\overline{WR}$ deassertion (data setup time)	t_{DS} (t_{DW})	$(WS - 0.25) \times T_C - 3.0$ [WS ≥ 1]	4.5	—	ns
109	Data hold time from $\overline{WR}$ deassertion	t_{DH}	$0.25 \times T_C - 2.0$ [1 ≤ WS ≤ 3]	0.5	—	ns
			$1.25 \times T_C - 2.0$ [4 ≤ WS ≤ 7]	10.5	—	ns
			$2.25 \times T_C - 2.0$ [WS ≥ 8]	20.5	—	ns
113	$\overline{RD}$ deassertion time		$0.75 \times T_C - 4.0$ [1 ≤ WS ≤ 3]	3.5	—	ns
			$1.75 \times T_C - 4.0$ [4 ≤ WS ≤ 7]	13.5	—	ns
			$2.75 \times T_C - 4.0$ [WS ≥ 8]	23.5	—	ns

Table 2-8. SRAM Read and Write Accesses[3] (Continued)

No.	Characteristics	Symbol	Expression[1]	Min	Max	Unit
114	$\overline{WR}$ deassertion time		$0.5 \times T_C - 4.0$ [WS = 1]	1.0	—	ns
			$T_C - 2.0$ [2 ≤ WS ≤ 3]	6.0	—	ns
			$2.5 \times T_C - 4.0$ [4 ≤ WS ≤ 7]	21.0	—	ns
			$3.5 \times T_C - 4.0$ [WS ≥ 8]	31.0	—	ns
115	Address valid to $\overline{RD}$ assertion		$0.5 \times T_C - 4.0$	1.0	—	ns
116	$\overline{RD}$ assertion pulse width		$(WS + 0.25) \times T_C - 4.0$	8.5	—	ns
117	$\overline{RD}$ deassertion to address not valid		$0.25 \times T_C - 2.0$ [1 ≤ WS ≤ 3]	0.5	—	ns
			$1.25 \times T_C - 2.0$ [4 ≤ WS ≤ 7]	10.5	—	ns
			$2.25 \times T_C - 2.0$ [WS ≥ 8]	20.5	—	ns
118	$\overline{TA}$ setup before $\overline{RD}$ or $\overline{WR}$ deassertion[4]		$0.25 \times T_C + 2.0$	4.5	—	ns
119	$\overline{TA}$ hold after $\overline{RD}$ or $\overline{WR}$ deassertion			0	—	ns

Notes:
1. WS is the number of wait states specified in the BCR.
2. Timings 100, 107 are guaranteed by design, not tested.
3. All timings for 100 MHz are measured from 0.5 · Vcc to .05 · Vcc
4. In the case of $\overline{TA}$ negation: timing 118 is relative to the deassertion edge of $\overline{RD}$ or WR were $\overline{TA}$ to remain active

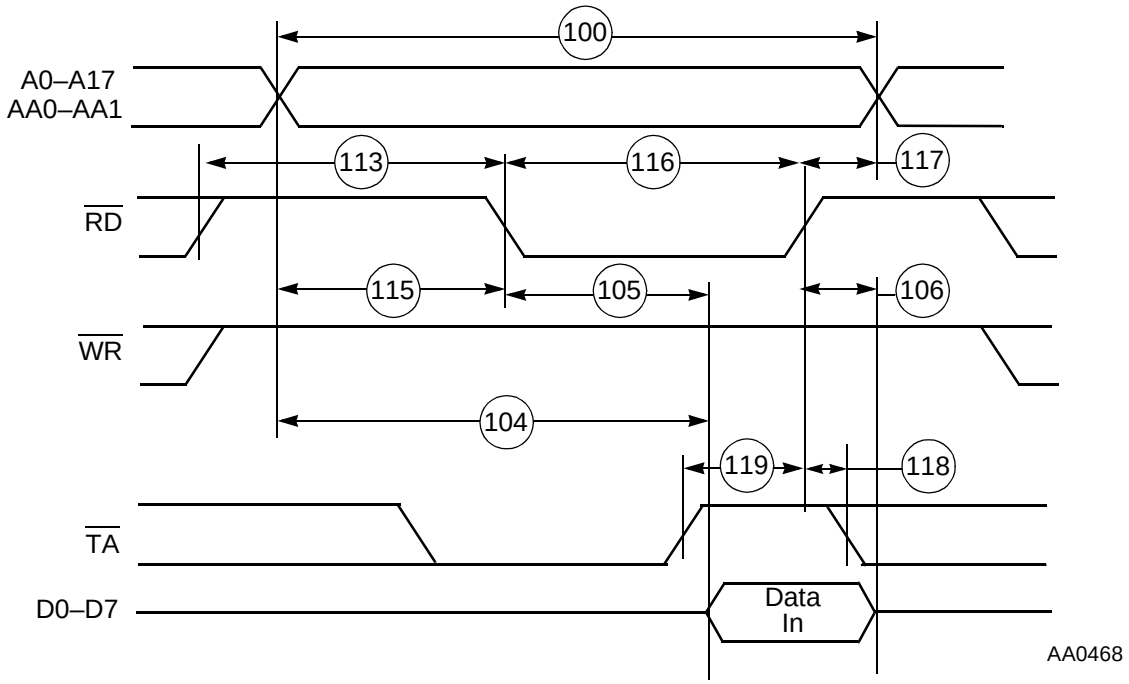


Figure 2-9. SRAM Read Access

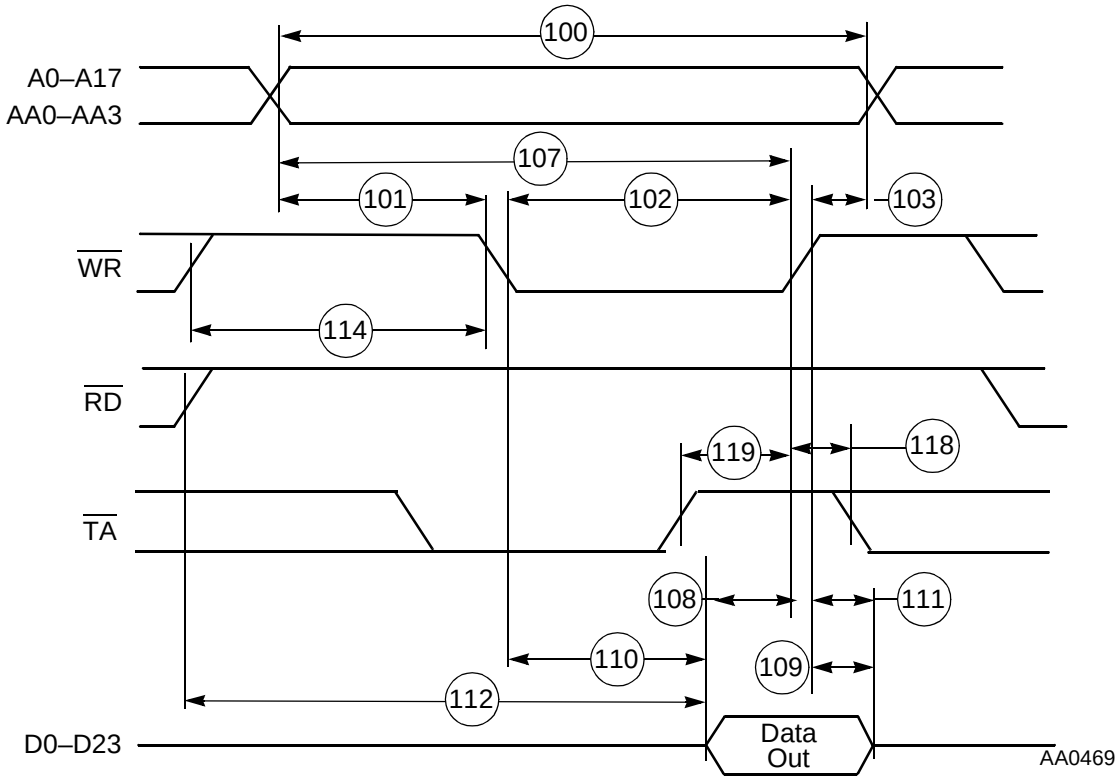


Figure 2-10. SRAM Write Access

DRAM Timing

The selection guides provided in **Figure 2-11.** and **Figure 2-14.** should be used for primary selection only. Final selection should be based on the timing provided in the following tables. As an example, the selection guide suggests that 4 wait states must be used for 100 MHz operation when using Page Mode DRAM. However, by using the information in the appropriate table, a designer may choose to evaluate whether fewer wait states might be used by determining which timing prevents operation at 100 MHz, running the chip at a slightly lower frequency (e.g., 95 MHz), using faster DRAM (if it becomes available), and control factors such as capacitive and resistive load to improve overall system performance.

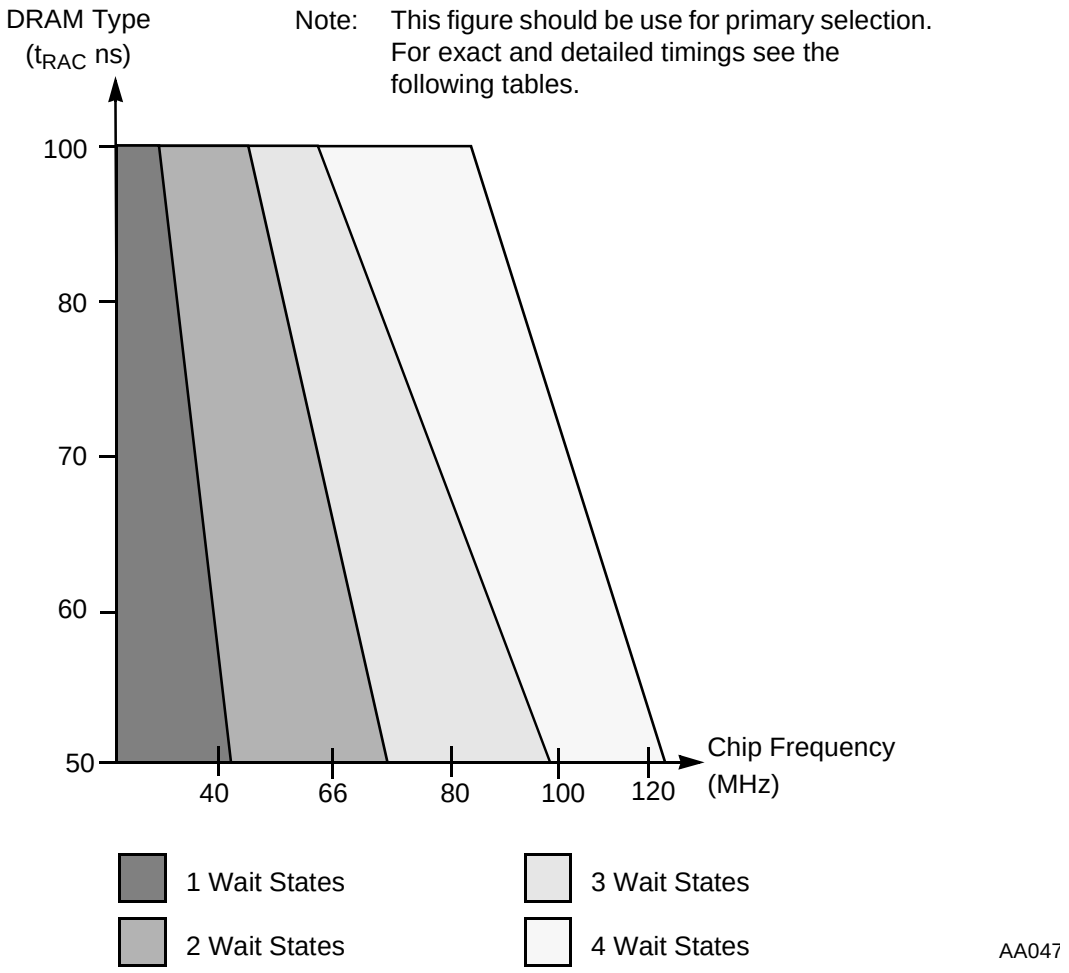


Figure 2-11. DRAM Page Mode Wait States Selection Guide

Table 2-9. DRAM Page Mode Timings, One Wait State (Low-Power Applications)[1, 2, 3]

No.	Characteristics	Symbol	Expression	20 MHz[6]		30 MHz[6]		Unit
				Min	Max	Min	Max	
131	Page mode cycle time for two consecutive accesses of the same direction	t_{PC}	$2 \times T_C$	100.0	—	66.7	—	ns
	Page mode cycle time for mixed (read and write) accesses		$1.25 \times T_C$	62.5	—	41.7	—	
132	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$T_C - 7.5$	—	42.5	—	25.8	ns
133	Column address valid to data valid (read)	t_{AA}	$1.5 \times T_C - 7.5$	—	67.5	—	42.5	ns
134	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	0.0	—	ns
135	Last $\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$0.75 \times T_C - 4.0$	33.5	—	21.0	—	ns
136	Previous $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion	t_{RHCP}	$2 \times T_C - 4.0$	96.0	—	62.7	—	ns
137	$\overline{CAS}$ assertion pulse width	t_{CAS}	$0.75 \times T_C - 4.0$	33.5	—	21.0	—	ns
138	Last $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion[4] • BRW[1:0] = 00	t_{CRP}	$1.75 \times T_C - 6.0$	81.5	—	52.3	—	ns
	• BRW[1:0] = 01		$3.25 \times T_C - 6.0$	156.5		102.2	—	ns
	• BRW[1:0] = 10		$4.25 \times T_C - 6.0$	206.5		135.5	—	ns
	• BRW[1:0] = 11		$6.25 \times T_C - 6.0$	306.5	—	202.1	—	ns
139	$\overline{CAS}$ deassertion pulse width	t_{CP}	$0.5 \times T_C - 4.0$	21.0	—	12.7	—	ns
140	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$0.5 \times T_C - 4.0$	21.0	—	12.7	—	ns
141	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$0.75 \times T_C - 4.0$	33.5	—	21.0	—	ns
142	Last column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$2 \times T_C - 4.0$	96.0	—	62.7	—	ns

Table 2-9. DRAM Page Mode Timings, One Wait State (Low-Power Applications)[1, 2, 3]

No.	Characteristics	Symbol	Expression	20 MHz[6]		30 MHz[6]		Unit
				Min	Max	Min	Max	
143	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$0.75 \times T_C - 3.8$	33.7	—	21.2	—	ns
144	$\overline{CAS}$ deassertion to $\overline{WR}$ assertion	t_{RCH}	$0.25 \times T_C - 3.7$	8.8	—	4.6	—	ns
145	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$0.5 \times T_C - 4.2$	20.8	—	12.5	—	ns
146	$\overline{WR}$ assertion pulse width	t_{WP}	$1.5 \times T_C - 4.5$	70.5	—	45.5	—	ns
147	Last $\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$1.75 \times T_C - 4.3$	83.2	—	54.0	—	ns
148	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$1.75 \times T_C - 4.3$	83.2	—	54.0	—	ns
149	Data valid to $\overline{CAS}$ assertion (Write)	t_{DS}	$0.25 \times T_C - 4.0$	8.5	—	4.3	—	ns
150	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$0.75 \times T_C - 4.0$	33.5	—	21.0	—	ns
151	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$T_C - 4.3$	45.7	—	29.0	—	ns
152	Last $\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$1.5 \times T_C - 4.0$	71.0	—	46.0	—	ns
153	$\overline{RD}$ assertion to data valid	t_{GA}	$T_C - 7.5$	—	42.5	—	25.8	ns
154	$\overline{RD}$ deassertion to data not valid [5]	t_{GZ}		0.0	—	0.0	—	ns
155	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 0.3$	37.2	—	24.7	—	ns
156	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	12.5	—	8.3	ns

Notes:
1. The number of wait states for Page mode access is specified in the DCR.
2. The refresh period is specified in the DCR.
3. All the timings are calculated for the worst case. Some of the timings are better for specific cases (e.g., t_{PC} equals $2 \times T_C$ for read-after-read or write-after-write sequences).
4. BRW[1:0] (DRAM control register bits) defines the number of wait states that should be inserted in each DRAM out-of-page access.
5. $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.
6. Reduced DSP clock speed allows use of Page Mode DRAM with one Wait state (See **Figure 2-14**.).

Table 2-10. DRAM Page Mode Timings, Two Wait States[1, 2, 3, 7]

No.	Characteristics	Symbol	Expression	66 MHz		80 MHz		Unit
				Min	Max	Min	Max	
131	Page mode cycle time for two consecutive accesses of the same direction	t_{PC}	$2 \times T_C$	45.4	—	37.5	—	ns
	Page mode cycle time for mixed (read and write) accesses		$1.25 \times T_C$	41.1	—	34.4	—	
132	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$1.5 \times T_C - 7.5$	—	15.2	—	—	ns
			$1.5 \times T_C - 6.5$	—	—	—	12.3	ns
133	Column address valid to data valid (read)	t_{AA}	$2.5 \times T_C - 7.5$	—	30.4	—	—	ns
			$2.5 \times T_C - 6.5$	—	—	—	24.8	ns
134	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	0.0	—	ns
135	Last $\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$1.75 \times T_C - 4.0$	22.5	—	17.9	—	ns
136	Previous $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion	t_{RHCP}	$3.25 \times T_C - 4.0$	45.2	—	36.6	—	ns
137	$\overline{CAS}$ assertion pulse width	t_{CAS}	$1.5 \times T_C - 4.0$	18.7	—	14.8	—	ns
138	Last $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion[5]	t_{CRP}	$2.0 \times T_C - 6.0$	24.4	—	19.0	—	ns
	• BRW[1:0] = 00							
	• BRW[1:0] = 01		$3.5 \times T_C - 6.0$	47.2	—	37.8	—	ns
	• BRW[1:0] = 10		$4.5 \times T_C - 6.0$	62.4	—	50.3	—	ns
	• BRW[1:0] = 11		$6.5 \times T_C - 6.0$	92.8	—	75.3	—	ns
139	$\overline{CAS}$ deassertion pulse width	t_{CP}	$1.25 \times T_C - 4.0$	14.9	—	11.6	—	ns
140	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$T_C - 4.0$	11.2	—	8.5	—	ns
141	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$1.75 \times T_C - 4.0$	22.5	—	17.9	—	ns

Table 2-10. DRAM Page Mode Timings, Two Wait States[1, 2, 3, 7] (Continued)

No.	Characteristics	Symbol	Expression	66 MHz		80 MHz		Unit
				Min	Max	Min	Max	
142	Last column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$3 \times T_C - 4.0$	41.5	—	33.5	—	ns
143	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$1.25 \times T_C - 3.8$	15.1	—	11.8	—	ns
144	$\overline{CAS}$ deassertion to $\overline{WR}$ assertion	t_{RCH}	$0.5 \times T_C - 3.7$	3.9	—	2.6	—	ns
145	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$1.5 \times T_C - 4.2$	18.5	—	14.6	—	ns
146	$\overline{WR}$ assertion pulse width	t_{WP}	$2.5 \times T_C - 4.5$	33.5	—	26.8	—	ns
147	Last $\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$2.75 \times T_C - 4.3$	33.4	—	26.8	—	ns
148	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$2.5 \times T_C - 4.3$	33.6	—	27.0	—	ns
149	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$0.25 \times T_C - 3.7$	0.1	—	—	—	ns
			$0.25 \times T_C - 3.0$	—	—	0.1	—	ns
150	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$1.75 \times T_C - 4.0$	22.5	—	17.9	—	ns
151	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$T_C - 4.3$	10.9	—	8.2	—	ns
152	Last $\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$2.5 \times T_C - 4.0$	33.9	—	27.3	—	ns
153	$\overline{RD}$ assertion to data valid	t_{GA}	$1.75 \times T_C - 7.5$	—	19.0	—	—	ns
			$1.75 \times T_C - 6.5$	—	—	—	15.4	ns
154	$\overline{RD}$ deassertion to data not valid[6]	t_{GZ}		0.0	—	0.0	—	ns
155	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 0.3$	11.1	—	9.1	—	ns
156	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	3.8	—	3.1	ns

Table 2-10. DRAM Page Mode Timings, Two Wait States[1, 2, 3, 7] (Continued)

No.	Characteristics	Symbol	Expression	66 MHz		80 MHz		Unit
				Min	Max	Min	Max	

Notes:
1. The number of wait states for Page mode access is specified in the DCR.
2. The refresh period is specified in the DCR.
3. The asynchronous delays specified in the expressions are valid for DSP56364.
4. All the timings are calculated for the worst case. Some of the timings are better for specific cases (e.g., t_{PC} equals $3 \times T_C$ for read-after-read or write-after-write sequences).
5. BRW[1:0] (DRAM Control Register bits) defines the number of wait states that should be inserted in each DRAM out-of-page access.
6. $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.
7. There are no DRAMs fast enough to fit to two wait states Page mode @ 100MHz (See **Figure 2-11.**)

Table 2-11. DRAM Page Mode Timings, Three Wait States[1, 2, 3]

No.	Characteristics	Symbol	Expression	Min	Max	Unit
131	Page mode cycle time for two consecutive accesses of the same direction	t_{PC}	$2 \times T_C$	40.0	—	ns
	Page mode cycle time for mixed (read and write) accesses		$1.25 \times T_C$	35.0	—	
132	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$2 \times T_C - 7.0$	—	13.0	ns
133	Column address valid to data valid (read)	t_{AA}	$3 \times T_C - 7.0$	—	23.0	ns
134	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	ns
135	Last $\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$2.5 \times T_C - 4.0$	21.0	—	ns
136	Previous $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion	t_{RHCP}	$4.5 \times T_C - 4.0$	41.0	—	ns
137	$\overline{CAS}$ assertion pulse width	t_{CAS}	$2 \times T_C - 4.0$	16.0	—	ns
138	Last $\overline{CAS}$ deassertion to $\overline{RAS}$ assertion[5] • BRW[1:0] = 00	t_{CRP}	$2.25 \times T_C - 6.0$	—	—	ns
	• BRW[1:0] = 01		$3.75 \times T_C - 6.0$	—	—	ns
	• BRW[1:0] = 10		$4.75 \times T_C - 6.0$	41.5	—	ns
	• BRW[1:0] = 11		$6.75 \times T_C - 6.0$	61.5	—	ns
139	$\overline{CAS}$ deassertion pulse width	t_{CP}	$1.5 \times T_C - 4.0$	11.0	—	ns
140	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$T_C - 4.0$	6.0	—	ns
141	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$2.5 \times T_C - 4.0$	21.0	—	ns

Table 2-11. DRAM Page Mode Timings, Three Wait States[1, 2, 3] (Continued)

No.	Characteristics	Symbol	Expression	Min	Max	Unit
142	Last column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$4 \times T_C - 4.0$	36.0	—	ns
143	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$1.25 \times T_C - 4.0$	8.5	—	ns
144	$\overline{CAS}$ deassertion to $\overline{WR}$ assertion	t_{RCH}	$0.75 \times T_C - 4.0$	3.5	—	ns
145	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$2.25 \times T_C - 4.2$	18.3	—	ns
146	$\overline{WR}$ assertion pulse width	t_{WP}	$3.5 \times T_C - 4.5$	30.5	—	ns
147	Last $\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$3.75 \times T_C - 4.3$	33.2	—	ns
148	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$3.25 \times T_C - 4.3$	28.2	—	ns
149	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$0.5 \times T_C - 4.0$	1.0	—	ns
150	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$2.5 \times T_C - 4.0$	21.0	—	ns
151	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$1.25 \times T_C - 4.3$	8.2	—	ns
152	Last $\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$3.5 \times T_C - 4.0$	31.0	—	ns
153	$\overline{RD}$ assertion to data valid	t_{GA}	$2.5 \times T_C - 7.0$	—	18.0	ns
154	$\overline{RD}$ deassertion to data not valid[6]	t_{GZ}		0.0	—	ns
155	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 0.3$	7.2	—	ns
156	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	2.5	ns

Notes:
1. The number of wait states for Page mode access is specified in the DCR.
2. The refresh period is specified in the DCR.
3. The asynchronous delays specified in the expressions are valid for DSP56364.
4. All the timings are calculated for the worst case. Some of the timings are better for specific cases (e.g., t_{PC} equals $4 \times T_C$ for read-after-read or write-after-write sequences).
5. BRW[1:0] (DRAM control register bits) defines the number of wait states that should be inserted in each DRAM out-of page-access.
6. $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.

Table 2-12. DRAM Page Mode Timings, Four Wait States[1, 2, 3]

No.	Characteristics	Symbol	Expression	Min	Max	
131	Page mode cycle time for two consecutive accesses of the same direction. Page mode cycle time for mixed (read and write) accesses	t_{PC}	$2 \times T_C$ $1.25 \times T_C$	50.0 45.0	— —	ns
132	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$2.75 \times T_C - 7.0$	—	20.5	ns
133	Column address valid to data valid (read)	t_{AA}	$3.75 \times T_C - 7.0$	—	30.5	ns
134	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	ns
135	Last $\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$3.5 \times T_C - 4.0$	31.0	—	ns
136	Previous $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion	t_{RHCP}	$6 \times T_C - 4.0$	56.0	—	ns
137	$\overline{CAS}$ assertion pulse width	t_{CAS}	$2.5 \times T_C - 4.0$	21.0	—	ns
138	Last $\overline{CAS}$ deassertion to $\overline{RAS}$ assertion[5] • BRW[1:0] = 00 • BRW[1:0] = 01 • BRW[1:0] = 10 • BRW[1:0] = 11	t_{CRP}	$2.75 \times T_C - 6.0$ $4.25 \times T_C - 6.0$ $5.25 \times T_C - 6.0$ $7.25 \times T_C - 6.0$	— — 46.5 66.5	— — — —	ns
139	$\overline{CAS}$ deassertion pulse width	t_{CP}	$2 \times T_C - 4.0$	16.0	—	ns
140	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$T_C - 4.0$	6.0	—	ns
141	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$3.5 \times T_C - 4.0$	31.0	—	ns
142	Last column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$5 \times T_C - 4.0$	46.0	—	ns
143	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$1.25 \times T_C - 4.0$	8.5	—	ns
144	$\overline{CAS}$ deassertion to $\overline{WR}$ assertion	t_{RCH}	$1.25 \times T_C - 4.0$	8.5	—	ns
145	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$3.25 \times T_C - 4.2$	28.3	—	ns
146	$\overline{WR}$ assertion pulse width	t_{WP}	$4.5 \times T_C - 4.5$	40.5	—	ns
147	Last $\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$4.75 \times T_C - 4.3$	43.2	—	ns
148	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$3.75 \times T_C - 4.3$	33.2	—	ns
149	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$0.5 \times T_C - 4.0$	1.0	—	ns
150	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$3.5 \times T_C - 4.0$	31.0	—	ns
151	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$1.25 \times T_C - 4.3$	8.2	—	ns

Table 2-12. DRAM Page Mode Timings, Four Wait States[1, 2, 3] (Continued)

No.	Characteristics	Symbol	Expression	Min	Max	
152	Last $\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$4.5 \times T_C - 4.0$	41.0	—	ns
153	$\overline{RD}$ assertion to data valid	t_{GA}	$3.25 \times T_C - 7.0$	—	25.5	ns
154	$\overline{RD}$ deassertion to data not valid[6]	t_{GZ}		0.0	—	ns
155	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 0.3$	7.2	—	ns
156	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	2.5	ns

Notes:
1. The number of wait states for Page mode access is specified in the DCR.
2. The refresh period is specified in the DCR.
3. The asynchronous delays specified in the expressions are valid for DSP56364.
4. All the timings are calculated for the worst case. Some of the timings are better for specific cases (e.g., t_{PC} equals $3 \times T_C$ for read-after-read or write-after-write sequences).
5. BRW[1:0] (DRAM control register bits) defines the number of wait states that should be inserted in each DRAM out-of-page access.
6. $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.

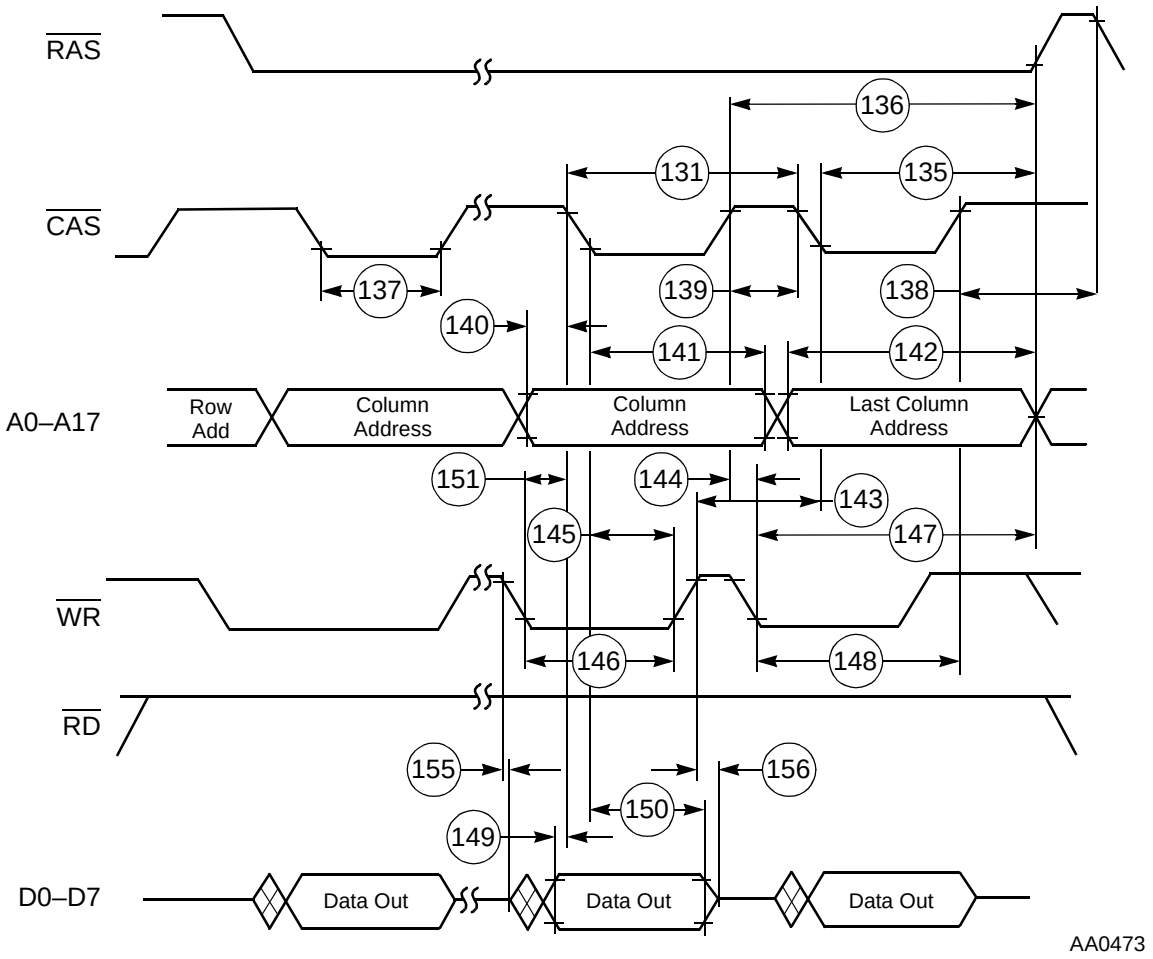


Figure 2-12. DRAM Page Mode Write Accesses

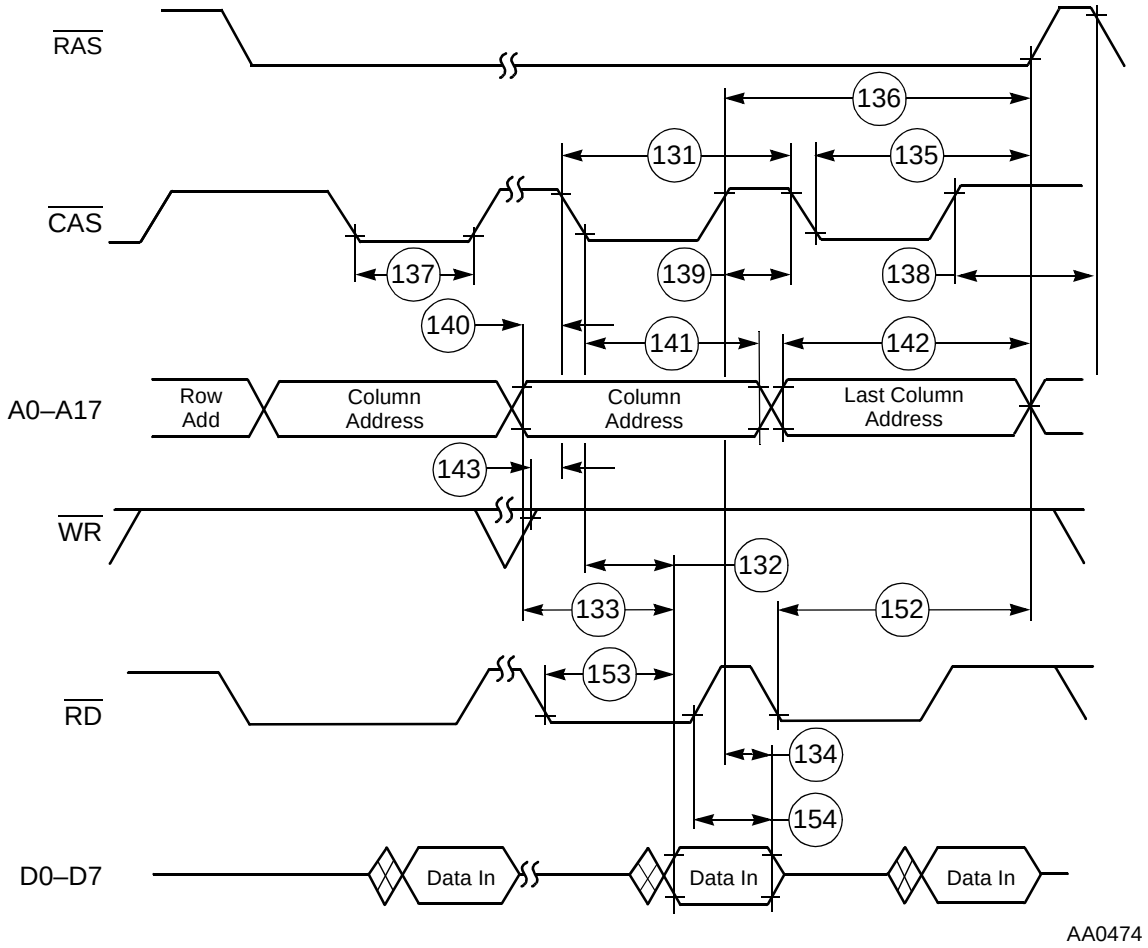


Figure 2-13. DRAM Page Mode Read Accesses

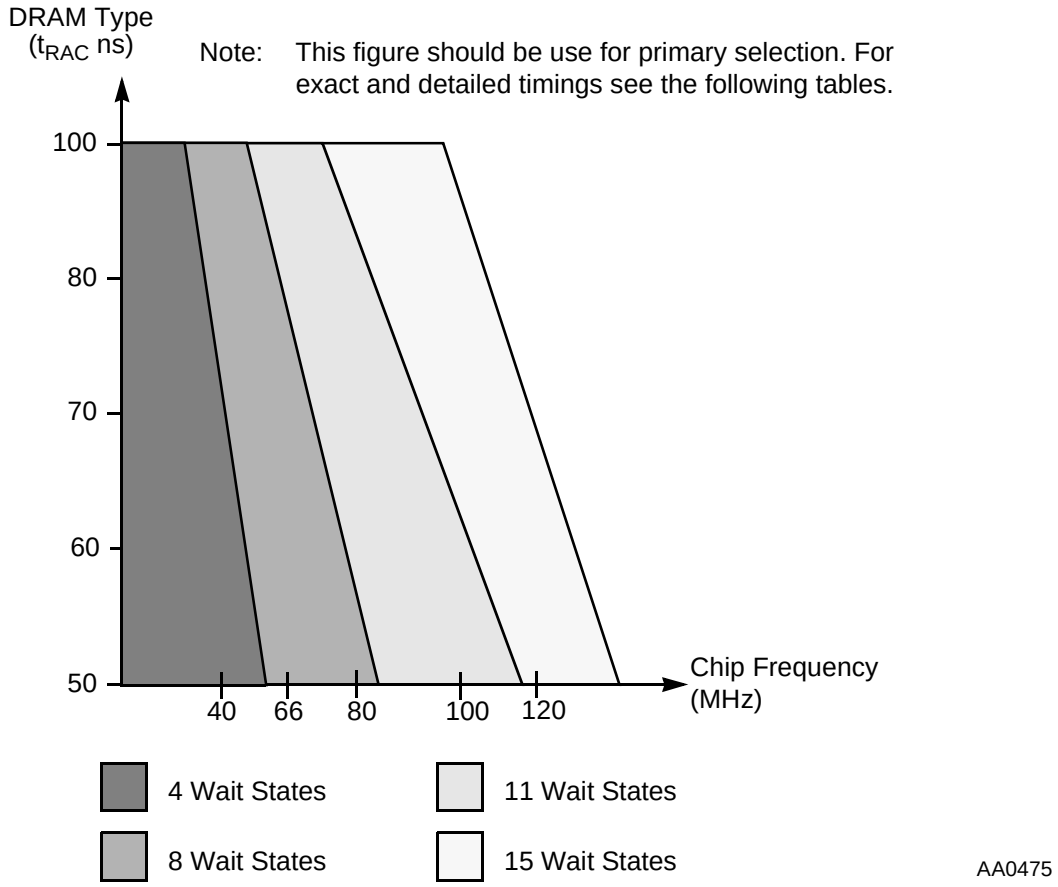


Figure 2-14. DRAM Out-of-Page Wait States Selection Guide

Table 2-13. DRAM Out-of-Page and Refresh Timings, Four Wait States[1, 2]

No.	Characteristics[3]	Symbol	Expression	20 MHz[4]		30 MHz[4]		Unit
				Min	Max	Min	Max	
157	Random read or write cycle time	t_{RC}	$5 \times T_C$	250.0	—	166.7	—	ns
158	$\overline{RAS}$ assertion to data valid (read)	t_{RAC}	$2.75 \times T_C - 7.5$	—	130.0	—	84.2	ns
159	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$1.25 \times T_C - 7.5$	—	55.0	—	34.2	ns
160	Column address valid to data valid (read)	t_{AA}	$1.5 \times T_C - 7.5$	—	67.5	—	42.5	ns

Table 2-13. DRAM Out-of-Page and Refresh Timings, Four Wait States[1, 2] (Continued)

No.	Characteristics[3]	Symbol	Expression	20 MHz[4]		30 MHz[4]		Unit
				Min	Max	Min	Max	
161	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	0.0	—	ns
162	$\overline{RAS}$ deassertion to $\overline{RAS}$ assertion	t_{RP}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
163	$\overline{RAS}$ assertion pulse width	t_{RAS}	$3.25 \times T_C - 4.0$	158.5	—	104.3	—	ns
164	$\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
165	$\overline{RAS}$ assertion to $\overline{CAS}$ deassertion	t_{CSH}	$2.75 \times T_C - 4.0$	133.5	—	87.7	—	ns
166	$\overline{CAS}$ assertion pulse width	t_{CAS}	$1.25 \times T_C - 4.0$	58.5	—	37.7	—	ns
167	$\overline{RAS}$ assertion to $\overline{CAS}$ assertion	t_{RCD}	$1.5 \times T_C \pm 2$	73.0	77.0	48.0	52.0	ns
168	$\overline{RAS}$ assertion to column address valid	t_{RAD}	$1.25 \times T_C \pm 2$	60.5	64.5	39.7	43.7	ns
169	$\overline{CAS}$ deassertion to $\overline{RAS}$ assertion	t_{CRP}	$2.25 \times T_C - 4.0$	108.5	—	71.0	—	ns
170	$\overline{CAS}$ deassertion pulse width	t_{CP}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
171	Row address valid to $\overline{RAS}$ assertion	t_{ASR}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
172	$\overline{RAS}$ assertion to row address not valid	t_{RAH}	$1.25 \times T_C - 4.0$	58.5	—	37.7	—	ns
173	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$0.25 \times T_C - 4.0$	8.5	—	4.3	—	ns
174	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
175	$\overline{RAS}$ assertion to column address not valid	t_{AR}	$3.25 \times T_C - 4.0$	158.5	—	104.3	—	ns
176	Column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$2 \times T_C - 4.0$	96.0	—	62.7	—	ns
177	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$1.5 \times T_C - 3.8$	71.2	—	46.2	—	ns
178	$\overline{CAS}$ deassertion to $\overline{WR}$ assertion	t_{RCH}	$0.75 \times T_C - 3.7$	33.8	—	21.3	—	ns

Table 2-13. DRAM Out-of-Page and Refresh Timings, Four Wait States[1, 2] (Continued)

No.	Characteristics[3]	Symbol	Expression	20 MHz[4]		30 MHz[4]		Unit
				Min	Max	Min	Max	
179	$\overline{RAS}$ deassertion to $\overline{WR}$ assertion	t_{RRH}	$0.25 \times T_C - 3.7$	8.8	—	4.6	—	ns
180	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$1.5 \times T_C - 4.2$	70.8	—	45.8	—	ns
181	$\overline{RAS}$ assertion to $\overline{WR}$ deassertion	t_{WCR}	$3 \times T_C - 4.2$	145.8	—	95.8	—	ns
182	$\overline{WR}$ assertion pulse width	t_{WP}	$4.5 \times T_C - 4.5$	220.5	—	145.5	—	ns
183	$\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$4.75 \times T_C - 4.3$	233.2	—	154.0	—	ns
184	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$4.25 \times T_C - 4.3$	208.2	—	137.4	—	ns
185	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$2.25 \times T_C - 4.0$	108.5	—	71.0	—	ns
186	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
187	$\overline{RAS}$ assertion to data not valid (write)	t_{DHR}	$3.25 \times T_C - 4.0$	158.5	—	104.3	—	ns
188	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$3 \times T_C - 4.3$	145.7	—	95.7	—	ns
189	$\overline{CAS}$ assertion to $\overline{RAS}$ assertion (refresh)	t_{CSR}	$0.5 \times T_C - 4.0$	21.0	—	12.7	—	ns
190	$\overline{RAS}$ deassertion to $\overline{CAS}$ assertion (refresh)	t_{RPC}	$1.25 \times T_C - 4.0$	58.5	—	37.7	—	ns
191	$\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$4.5 \times T_C - 4.0$	221.0	—	146.0	—	ns
192	$\overline{RD}$ assertion to data valid	t_{GA}	$4 \times T_C - 7.5$	—	192.5	—	125.8	ns
193	$\overline{RD}$ deassertion to data not valid[3]	t_{GZ}		0.0	—	0.0	—	ns
194	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 0.3$	37.2	—	24.7	—	ns
195	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	12.5	—	8.3	ns

Table 2-13. DRAM Out-of-Page and Refresh Timings, Four Wait States[1, 2] (Continued)

No.	Characteristics[3]	Symbol	Expression	20 MHz[4]		30 MHz[4]		Unit
				Min	Max	Min	Max	

Notes:
1. The number of wait states for out of page access is specified in the DCR.
2. The refresh period is specified in the DCR.
3. $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.
4. Reduced DSP clock speed allows use of DRAM out-of-page access with four Wait states (See **Figure 2-17**.).

Table 2-14. DRAM Out-of-Page and Refresh Timings, Eight Wait States[1, 2]

No.	Characteristics[4]	Symbol	Expression[3]	66 MHz		80 MHz		Unit
				Min	Max	Min	Max	
157	Random read or write cycle time	t_{RC}	$9 \times T_C$	136.4	—	112.5	—	ns
158	$\overline{RAS}$ assertion to data valid (read)	t_{RAC}	$4.75 \times T_C - 7.5$	—	64.5	—	—	ns
			$4.75 \times T_C - 6.5$	—	—	—	52.9	ns
159	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$2.25 \times T_C - 7.5$	—	26.6	—	—	ns
			$2.25 \times T_C - 6.5$	—	—	—	21.6	ns
160	Column address valid to data valid (read)	t_{AA}	$3 \times T_C - 7.5$	—	40.0	—	—	ns
			$3 \times T_C - 6.5$	—	—	—	31.0	ns
161	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	0.0	—	ns
162	$\overline{RAS}$ deassertion to $\overline{RAS}$ assertion	t_{RP}	$3.25 \times T_C - 4.0$	45.2	—	36.6	—	ns
163	$\overline{RAS}$ assertion pulse width	t_{RAS}	$5.75 \times T_C - 4.0$	83.1	—	67.9	—	ns
164	$\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$3.25 \times T_C - 4.0$	45.2	—	36.6	—	ns
165	$\overline{RAS}$ assertion to $\overline{CAS}$ deassertion	t_{CSH}	$4.75 \times T_C - 4.0$	68.0	—	55.5	—	ns
166	$\overline{CAS}$ assertion pulse width	t_{CAS}	$2.25 \times T_C - 4.0$	30.1	—	24.1	—	ns
167	$\overline{RAS}$ assertion to $\overline{CAS}$ assertion	t_{RCD}	$2.5 \times T_C \pm 2$	35.9	39.9	29.3	33.3	ns

Table 2-14. DRAM Out-of-Page and Refresh Timings, Eight Wait States[1, 2] (Continued)

No.	Characteristics[4]	Symbol	Expression[3]	66 MHz		80 MHz		Unit
				Min	Max	Min	Max	
168	$\overline{RAS}$ assertion to column address valid	t_{RAD}	$1.75 \times T_C \pm 2$	24.5	28.5	19.9	23.9	ns
169	$\overline{CAS}$ deassertion to $\overline{RAS}$ assertion	t_{CRP}	$4.25 \times T_C - 4.0$	59.8	—	49.1	—	ns
170	$\overline{CAS}$ deassertion pulse width	t_{CP}	$2.75 \times T_C - 4.0$	37.7	—	30.4	—	ns
171	Row address valid to $\overline{RAS}$ assertion	t_{ASR}	$3.25 \times T_C - 4.0$	45.2	—	36.6	—	ns
172	$\overline{RAS}$ assertion to row address not valid	t_{RAH}	$1.75 \times T_C - 4.0$	22.5	—	17.9	—	ns
173	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$0.75 \times T_C - 4.0$	7.4	—	5.4	—	ns
174	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$3.25 \times T_C - 4.0$	45.2	—	36.6	—	ns
175	$\overline{RAS}$ assertion to column address not valid	t_{AR}	$5.75 \times T_C - 4.0$	83.1	—	67.9	—	ns
176	Column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$4 \times T_C - 4.0$	56.6	—	46.0	—	ns
177	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$2 \times T_C - 3.8$	26.5	—	21.2	—	ns
178	$\overline{CAS}$ deassertion to $\overline{WR}$[5] assertion	t_{RCH}	$1.25 \times T_C - 3.7$	15.2	—	11.9	—	ns
179	$\overline{RAS}$ deassertion to $\overline{WR}$[5] assertion	t_{RRH}	$0.25 \times T_C - 3.7$ $0.25 \times T_C - 3.0$	0.1 —	— —	— 0.1	— —	ns ns
180	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$3 \times T_C - 4.2$	41.3	—	33.3	—	ns
181	$\overline{RAS}$ assertion to $\overline{WR}$ deassertion	t_{WCR}	$5.5 \times T_C - 4.2$	79.1	—	64.6	—	ns
182	$\overline{WR}$ assertion pulse width	t_{WP}	$8.5 \times T_C - 4.5$	124.3	—	101.8	—	ns
183	$\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$8.75 \times T_C - 4.3$	128.3	—	105.1	—	ns
184	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$7.75 \times T_C - 4.3$	113.1	—	92.6	—	ns

Table 2-14. DRAM Out-of-Page and Refresh Timings, Eight Wait States[1, 2] (Continued)

No.	Characteristics[4]	Symbol	Expression[3]	66 MHz		80 MHz		Unit
				Min	Max	Min	Max	
185	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$4.75 \times T_C - 4.0$	68.0	—	55.4	—	ns
186	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$3.25 \times T_C - 4.0$	45.2	—	36.6	—	ns
187	$\overline{RAS}$ assertion to data not valid (write)	t_{DHR}	$5.75 \times T_C - 4.0$	83.1	—	67.9	—	ns
188	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$5.5 \times T_C - 4.3$	79.0	—	64.5	—	ns
189	$\overline{CAS}$ assertion to $\overline{RAS}$ assertion (refresh)	t_{CSR}	$1.5 \times T_C - 4.0$	18.7	—	14.8	—	ns
190	$\overline{RAS}$ deassertion to $\overline{CAS}$ assertion (refresh)	t_{RPC}	$1.75 \times T_C - 4.0$	22.5	—	17.9	—	ns
191	$\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$8.5 \times T_C - 4.0$	124.8	—	102.3	—	ns
192	$\overline{RD}$ assertion to data valid	t_{GA}	$7.5 \times T_C - 7.5$ $7.5 \times T_C - 6.5$	— —	106.1 —	— —	— 87.3	ns ns
193	$\overline{RD}$ deassertion to data not valid[4]	t_{GZ}	0.0	0.0	—	0.0	—	ns
194	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 0.3$	11.1	—	9.1	—	ns
195	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	3.8	—	3.1	ns

Notes:
1. The number of wait states for out-of-page access is specified in the DCR.
2. The refresh period is specified in the DCR.
3. The asynchronous delays specified in the expressions are valid for DSP56364.
4. $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.
5. Either t_{RCH} or t_{RRH} must be satisfied for read cycles.

Table 2-15. DRAM Out-of-Page and Refresh Timings, Eleven Wait States[1, 2]

No.	Characteristics[4]	Symbol	Expression[3]	Min	Max	Unit
157	Random read or write cycle time	t_{RC}	$12 \times T_C$	120.0	—	ns
158	$\overline{RAS}$ assertion to data valid (read)	t_{RAC}	$6.25 \times T_C - 7.0$	—	55.5	ns
159	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$3.75 \times T_C - 7.0$	—	30.5	ns
160	Column address valid to data valid (read)	t_{AA}	$4.5 \times T_C - 7.0$	—	38.0	ns
161	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	ns
162	$\overline{RAS}$ deassertion to $\overline{RAS}$ assertion	t_{RP}	$4.25 \times T_C - 4.0$	38.5	—	ns
163	$\overline{RAS}$ assertion pulse width	t_{RAS}	$7.75 \times T_C - 4.0$	73.5	—	ns
164	$\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$5.25 \times T_C - 4.0$	48.5	—	ns
165	$\overline{RAS}$ assertion to $\overline{CAS}$ deassertion	t_{CSH}	$6.25 \times T_C - 4.0$	58.5	—	ns
166	$\overline{CAS}$ assertion pulse width	t_{CAS}	$3.75 \times T_C - 4.0$	33.5	—	ns
167	$\overline{RAS}$ assertion to $\overline{CAS}$ assertion	t_{RCD}	$2.5 \times T_C \pm 4.0$	21.0	29.0	ns
168	$\overline{RAS}$ assertion to column address valid	t_{RAD}	$1.75 \times T_C \pm 4.0$	13.5	21.5	ns
169	$\overline{CAS}$ deassertion to $\overline{RAS}$ assertion	t_{CRP}	$5.75 \times T_C - 4.0$	53.5	—	ns
170	$\overline{CAS}$ deassertion pulse width	t_{CP}	$4.25 \times T_C - 4.0$	38.5	—	ns
171	Row address valid to $\overline{RAS}$ assertion	t_{ASR}	$4.25 \times T_C - 4.0$	38.5	—	ns
172	$\overline{RAS}$ assertion to row address not valid	t_{RAH}	$1.75 \times T_C - 4.0$	13.5	—	ns
173	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$0.75 \times T_C - 4.0$	3.5	—	ns
174	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$5.25 \times T_C - 4.0$	48.5	—	ns
175	$\overline{RAS}$ assertion to column address not valid	t_{AR}	$7.75 \times T_C - 4.0$	73.5	—	ns
176	Column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$6 \times T_C - 4.0$	56.0	—	ns
177	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$3.0 \times T_C - 4.0$	26.0	—	ns
178	$\overline{CAS}$ deassertion to $\overline{WR}$[5] assertion	t_{RCH}	$1.75 \times T_C - 4.0$	13.5	—	ns
179	$\overline{RAS}$ deassertion to $\overline{WR}$[5] assertion	t_{RRH}	$0.25 \times T_C - 2.0$	0.5	—	ns
180	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$5 \times T_C - 4.2$	45.8	—	ns
181	$\overline{RAS}$ assertion to $\overline{WR}$ deassertion	t_{WCR}	$7.5 \times T_C - 4.2$	70.8	—	ns
182	$\overline{WR}$ assertion pulse width	t_{WP}	$11.5 \times T_C - 4.5$	110.5	—	ns

Table 2-15. DRAM Out-of-Page and Refresh Timings, Eleven Wait States[1, 2] (Continued)

No.	Characteristics[4]	Symbol	Expression[3]	Min	Max	Unit
183	$\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$11.75 \times T_C - 4.3$	113.2	—	ns
184	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$10.25 \times T_C - 4.3$	103.2	—	ns
185	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$5.75 \times T_C - 4.0$	53.5	—	ns
186	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$5.25 \times T_C - 4.0$	48.5	—	ns
187	$\overline{RAS}$ assertion to data not valid (write)	t_{DHR}	$7.75 \times T_C - 4.0$	73.5	—	ns
188	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$6.5 \times T_C - 4.3$	60.7	—	ns
189	$\overline{CAS}$ assertion to $\overline{RAS}$ assertion (refresh)	t_{CSR}	$1.5 \times T_C - 4.0$	11.0	—	ns
190	$\overline{RAS}$ deassertion to $\overline{CAS}$ assertion (refresh)	t_{RPC}	$2.75 \times T_C - 4.0$	23.5	—	ns
191	$\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$11.5 \times T_C - 4.0$	111.0	—	ns
192	$\overline{RD}$ assertion to data valid	t_{GA}	$10 \times T_C - 7.0$	—	93.0	ns
193	$\overline{RD}$ deassertion to data not valid[4]	t_{GZ}		0.0	—	ns
194	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 0.3$	7.2	—	ns
195	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	2.5	ns

Notes:
1. The number of wait states for out-of-page access is specified in the DCR.
2. The refresh period is specified in the DCR.
3. The asynchronous delays specified in the expressions are valid for DSP56364.
4. $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.
5. Either t_{RCH} or t_{RRH} must be satisfied for read cycles.

Table 2-16. DRAM Out-of-Page and Refresh Timings, Fifteen Wait States[1, 2]

No.	Characteristics[3]	Symbol	Expression	Min	Max	Unit
157	Random read or write cycle time	t_{RC}	$16 \times T_C$	160.0	—	ns
158	$\overline{RAS}$ assertion to data valid (read)	t_{RAC}	$8.25 \times T_C - 5.7$	—	76.8	ns
159	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$4.75 \times T_C - 5.7$	—	41.8	ns
160	Column address valid to data valid (read)	t_{AA}	$5.5 \times T_C - 5.7$	—	49.3	ns
161	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}	0.0	0.0	—	ns
162	$\overline{RAS}$ deassertion to $\overline{RAS}$ assertion	t_{RP}	$6.25 \times T_C - 4.0$	58.5	—	ns
163	$\overline{RAS}$ assertion pulse width	t_{RAS}	$9.75 \times T_C - 4.0$	93.5	—	ns
164	$\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$6.25 \times T_C - 4.0$	58.5	—	ns
165	$\overline{RAS}$ assertion to $\overline{CAS}$ deassertion	t_{CSH}	$8.25 \times T_C - 4.0$	78.5	—	ns
166	$\overline{CAS}$ assertion pulse width	t_{CAS}	$4.75 \times T_C - 4.0$	43.5	—	ns
167	$\overline{RAS}$ assertion to $\overline{CAS}$ assertion	t_{RCD}	$3.5 \times T_C \pm 2$	33.0	37.0	ns
168	$\overline{RAS}$ assertion to column address valid	t_{RAD}	$2.75 \times T_C \pm 2$	25.5	29.5	ns
169	$\overline{CAS}$ deassertion to $\overline{RAS}$ assertion	t_{CRP}	$7.75 \times T_C - 4.0$	73.5	—	ns
170	$\overline{CAS}$ deassertion pulse width	t_{CP}	$6.25 \times T_C - 4.0$	58.5	—	ns
171	Row address valid to $\overline{RAS}$ assertion	t_{ASR}	$6.25 \times T_C - 4.0$	58.5	—	ns
172	$\overline{RAS}$ assertion to row address not valid	t_{RAH}	$2.75 \times T_C - 4.0$	23.5	—	ns
173	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$0.75 \times T_C - 4.0$	3.5	—	ns
174	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$6.25 \times T_C - 4.0$	58.5	—	ns
175	$\overline{RAS}$ assertion to column address not valid	t_{AR}	$9.75 \times T_C - 4.0$	93.5	—	ns
176	Column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$7 \times T_C - 4.0$	66.0	—	ns
177	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$5 \times T_C - 3.8$	46.2	—	ns
178	$\overline{CAS}$ deassertion to $\overline{WR}$[5] assertion	t_{RCH}	$1.75 \times T_C - 3.7$	13.8	—	ns
179	$\overline{RAS}$ deassertion to $\overline{WR}$[5] assertion	t_{RRH}	$0.25 \times T_C - 2.0$	0.5	—	ns
180	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$6 \times T_C - 4.2$	55.8	—	ns
181	$\overline{RAS}$ assertion to $\overline{WR}$ deassertion	t_{WCR}	$9.5 \times T_C - 4.2$	90.8	—	ns

Table 2-16. DRAM Out-of-Page and Refresh Timings, Fifteen Wait States[1, 2] (Continued)

No.	Characteristics[3]	Symbol	Expression	Min	Max	Unit
182	$\overline{WR}$ assertion pulse width	t_{WP}	$15.5 \times T_C - 4.5$	150.5	—	ns
183	$\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$15.75 \times T_C - 4.3$	153.2	—	ns
184	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$14.25 \times T_C - 4.3$	138.2	—	ns
185	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$8.75 \times T_C - 4.0$	83.5	—	ns
186	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$6.25 \times T_C - 4.0$	58.5	—	ns
187	$\overline{RAS}$ assertion to data not valid (write)	t_{DHR}	$9.75 \times T_C - 4.0$	93.5	—	ns
188	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$9.5 \times T_C - 4.3$	90.7	—	ns
189	$\overline{CAS}$ assertion to $\overline{RAS}$ assertion (refresh)	t_{CSR}	$1.5 \times T_C - 4.0$	11.0	—	ns
190	$\overline{RAS}$ deassertion to $\overline{CAS}$ assertion (refresh)	t_{RPC}	$4.75 \times T_C - 4.0$	43.5	—	ns
191	$\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$15.5 \times T_C - 4.0$	151.0	—	ns
192	$\overline{RD}$ assertion to data valid	t_{GA}	$14 \times T_C - 5.7$	—	134.3	ns
193	$\overline{RD}$ deassertion to data not valid[3]	t_{GZ}		0.0	—	ns
194	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 0.3$	7.2	—	ns
195	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	2.5	ns

Notes:
1. The number of wait states for out-of-page access is specified in the DCR.
2. The refresh period is specified in the DCR.
3. $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.
4. Either t_{RCH} or t_{RRH} must be satisfied for read cycles.

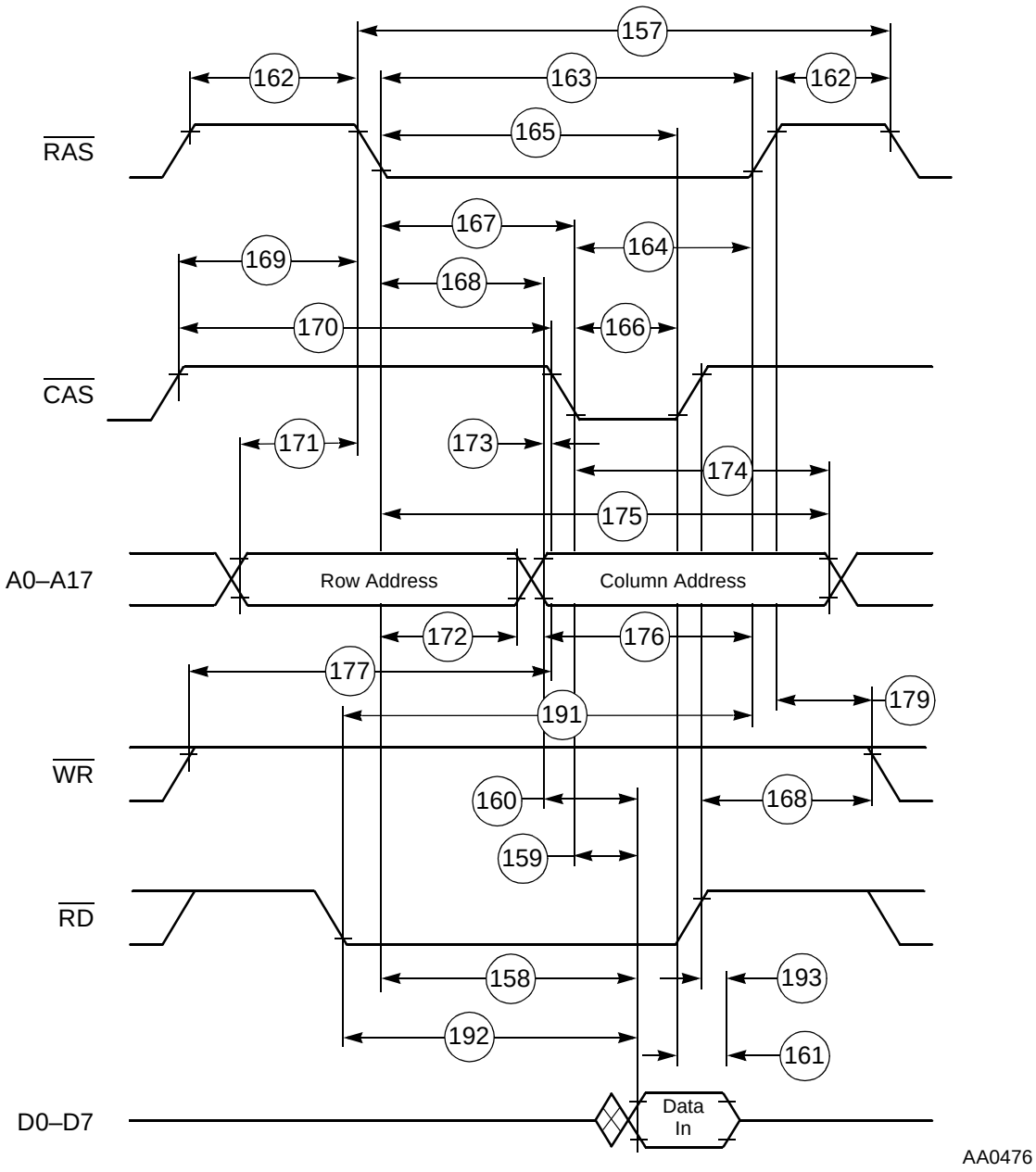


Figure 2-15. DRAM Out-of-Page Read Access

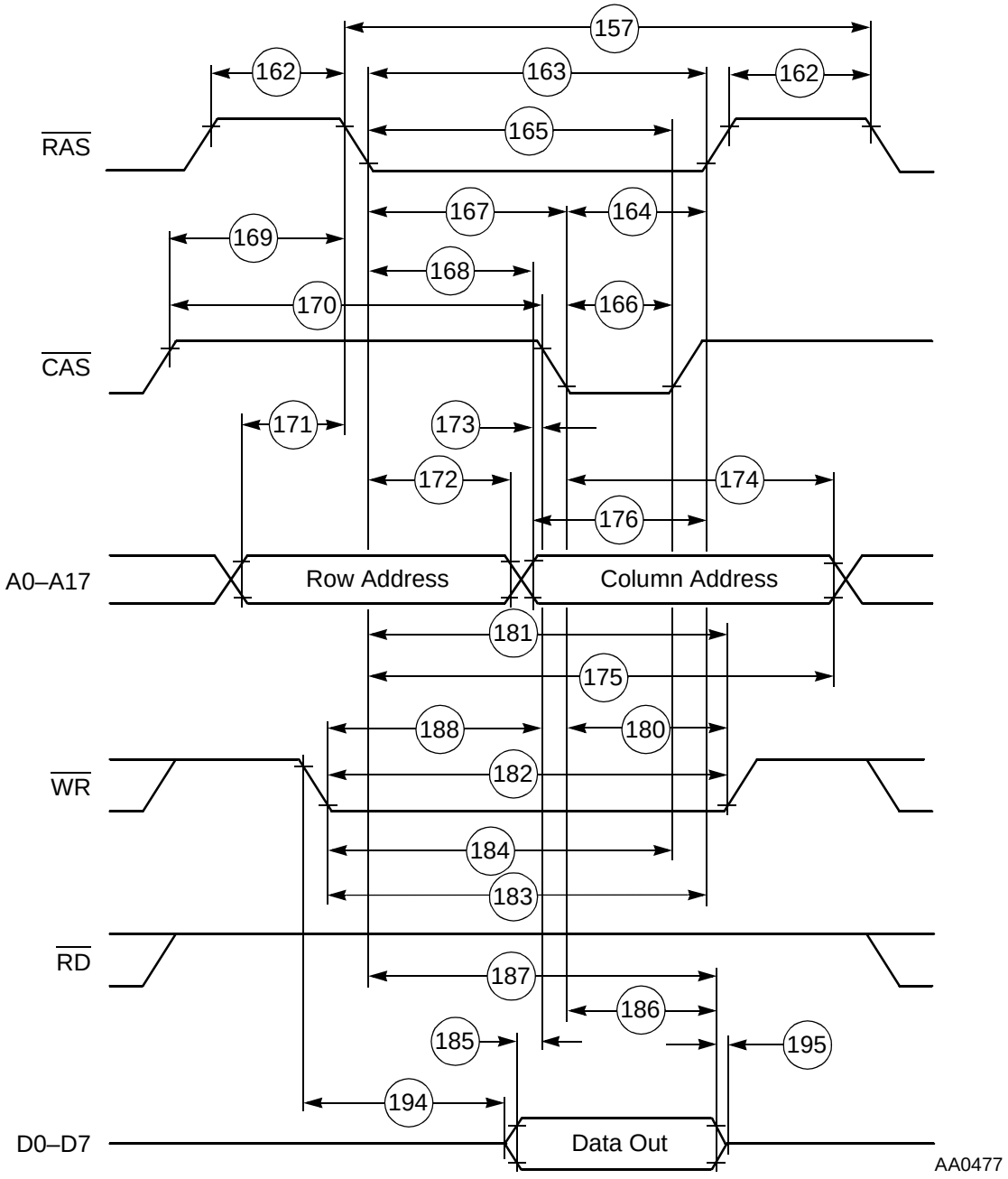


Figure 2-16. DRAM Out-of-Page Write Access

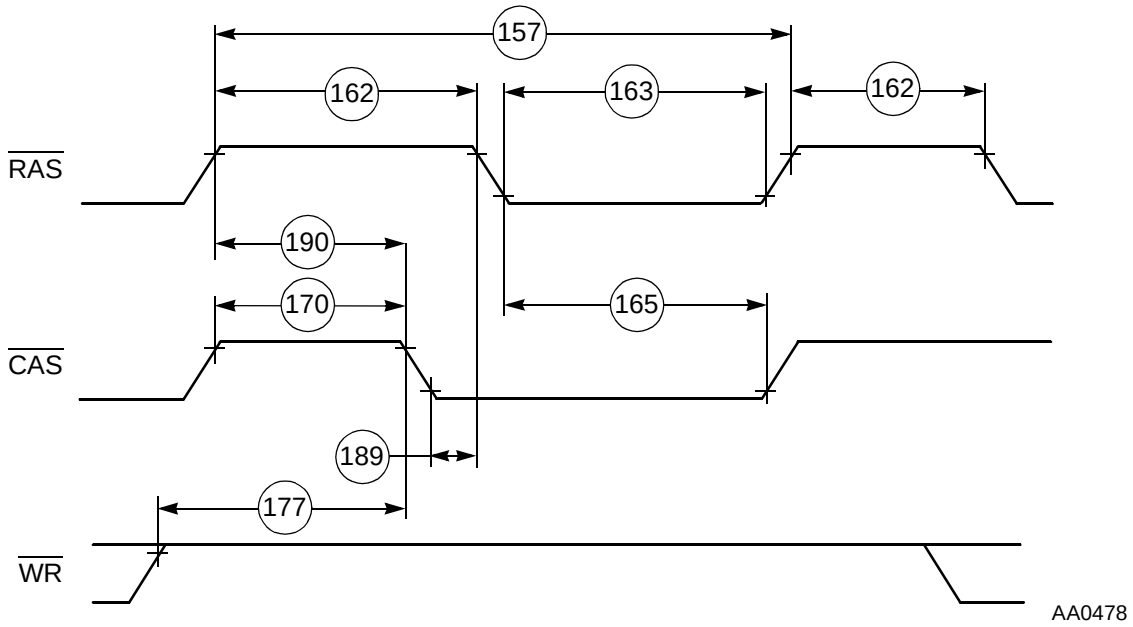


Figure 2-17. DRAM Refresh Access

SERIAL HOST INTERFACE SPI PROTOCOL TIMING

Table 2-17. Serial Host Interface SPI Protocol Timing

No.	Characteristics	Mode	Filter Mode	Expression	Min	Max	Unit
140	Tolerable spike width on clock or data in	—	Bypassed	—	—	0	ns
			Narrow	—	—	50	ns
			Wide	—	—	100	ns
141	Minimum serial clock cycle = t_{SPICC}(min)	Master	Bypassed	$6\times T_C+46$	106	—	ns
			Narrow	$6\times T_C+152$	212	—	ns
			Wide	$6\times T_C+223$	283	—	ns
142	Serial clock high period	Master	Bypassed	$0.5\times t_{SPICC}-10$	43	—	ns
			Narrow	$0.5\times t_{SPICC}-10$	96	—	ns
			Wide	$0.5\times t_{SPICC}-10$	131	—	ns
		Slave	Bypassed	$2.5\times T_C+12$	37	—	ns
			Narrow	$2.5\times T_C+102$	127	—	ns
			Wide	$2.5\times T_C+189$	214	—	ns
143	Serial clock low period	Master	Bypassed	$0.5\times t_{SPICC}-10$	43	—	ns
			Narrow	$0.5\times t_{SPICC}-10$	96	—	ns
			Wide	$0.5\times t_{SPICC}-10$	131	—	ns
		Slave	Bypassed	$2.5\times T_C+12$	37	—	ns
			Narrow	$2.5\times T_C+102$	127	—	ns
			Wide	$2.5\times T_C+189$	214	—	ns
144	Serial clock rise/fall time	Master	—	—	—	10	ns
		Slave	—	—	—	2000	ns

Table 2-17. Serial Host Interface SPI Protocol Timing (Continued)

No.	Characteristics	Mode	Filter Mode	Expression	Min	Max	Unit
146	$\overline{SS}$ assertion to first SCK edge CPHA = 0	Slave	Bypassed	$3.5 \times T_C + 15$	50	—	ns
			Narrow	0	0	—	ns
			Wide	0	0	—	ns
	CPHA = 1	Slave	Bypassed	10	10	—	ns
			Narrow	0	0	—	ns
			Wide	0	0	—	ns
147	Last SCK edge to $\overline{SS}$ not asserted	Slave	Bypassed	12	12	—	ns
			Narrow	102	102	—	ns
			Wide	189	189	—	ns
148	Data input valid to SCK edge (data input set-up time)	Master /Slave	Bypassed	0	0	—	ns
			Narrow	$MAX\{(20-T_C), 0\}$	10	—	ns
			Wide	$MAX\{(40-T_C), 0\}$	30	—	ns
149	SCK last sampling edge to data input not valid	Master /Slave	Bypassed	$2.5 \times T_C + 10$	35	—	ns
			Narrow	$2.5 \times T_C + 30$	55	—	ns
			Wide	$2.5 \times T_C + 50$	75	—	ns
150	$\overline{SS}$ assertion to data out active	Slave	—	2	2	—	ns
151	$\overline{SS}$ deassertion to data high impedance	Slave	—	9	—	9	ns
152	SCK edge to data out valid (data out delay time)	Master /Slave	Bypassed	$2 \times T_C + 33$	—	53	ns
			Narrow	$2 \times T_C + 123$	—	143	ns
			Wide	$2 \times T_C + 210$	—	230	ns
153	SCK edge to data out not valid (data out hold time)	Master /Slave	Bypassed	$T_C + 5$	15	—	ns
			Narrow	$T_C + 55$	65	—	ns
			Wide	$T_C + 106$	116	—	ns
154	$\overline{SS}$ assertion to data out valid (CPHA = 0)	Slave	—	$T_C + 33$	—	43	ns

Table 2-17. Serial Host Interface SPI Protocol Timing (Continued)

No.	Characteristics	Mode	Filter Mode	Expression	Min	Max	Unit
157	First SCK sampling edge to $\overline{\text{HREQ}}$ output deassertion	Slave	Bypassed	$2.5\times T_C+30$	—	55	ns
			Narrow	$2.5\times T_C+120$	—	145	ns
			Wide	$2.5\times T_C+217$	—	242	ns
158	Last SCK sampling edge to $\overline{\text{HREQ}}$ output not deasserted (CPHA = 1)	Slave	Bypassed	$2.5\times T_C+30$	55	—	ns
			Narrow	$2.5\times T_C+80$	105	—	ns
			Wide	$2.5\times T_C+136$	161	—	ns
159	$\overline{\text{SS}}$ deassertion to $\overline{\text{HREQ}}$ output not deasserted (CPHA = 0)	Slave	—	$2.5\times T_C+30$	55	—	ns
160	$\overline{\text{SS}}$ deassertion pulse width (CPHA = 0)	Slave	—	T_C+6	16	—	ns
161	$\overline{\text{HREQ}}$ in assertion to first SCK edge	Master	Bypassed	$0.5 \times t_{SPICC} + 2.5\times T_C+43$	121	—	ns
			Narrow	$0.5 \times t_{SPICC} + 2.5\times T_C+43$	174	—	ns
			Wide	$0.5 \times t_{SPICC} + 2.5\times T_C+43$	209	—	ns
162	$\overline{\text{HREQ}}$ in deassertion to last SCK sampling edge ($\overline{\text{HREQ}}$ in set-up time) (CPHA = 1)	Master	—	0	0	—	ns
163	First SCK edge to $\overline{\text{HREQ}}$ in not asserted ($\overline{\text{HREQ}}$ in hold time)	Master	—	0	0	—	ns

Note: Periodically sampled, not 100% tested

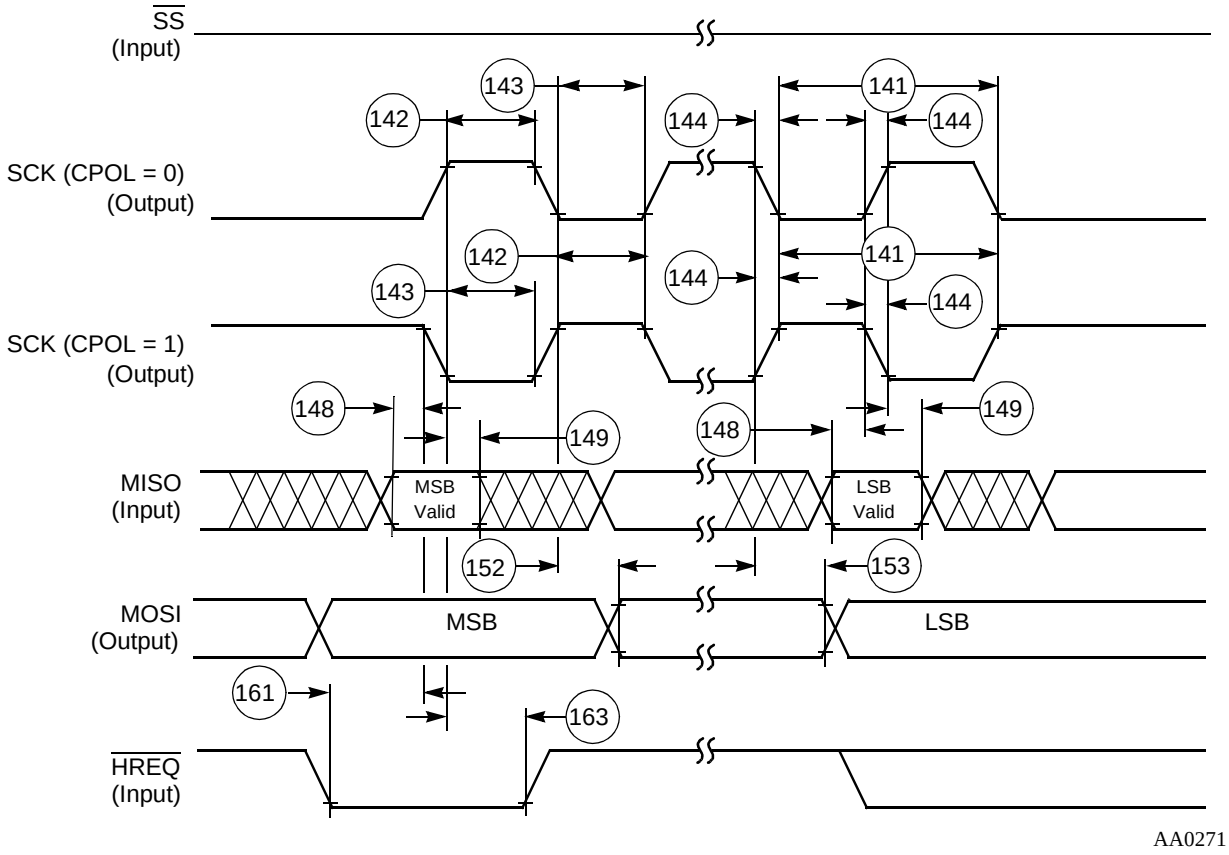


Figure 2-18. SPI Master Timing (CPHA = 0)

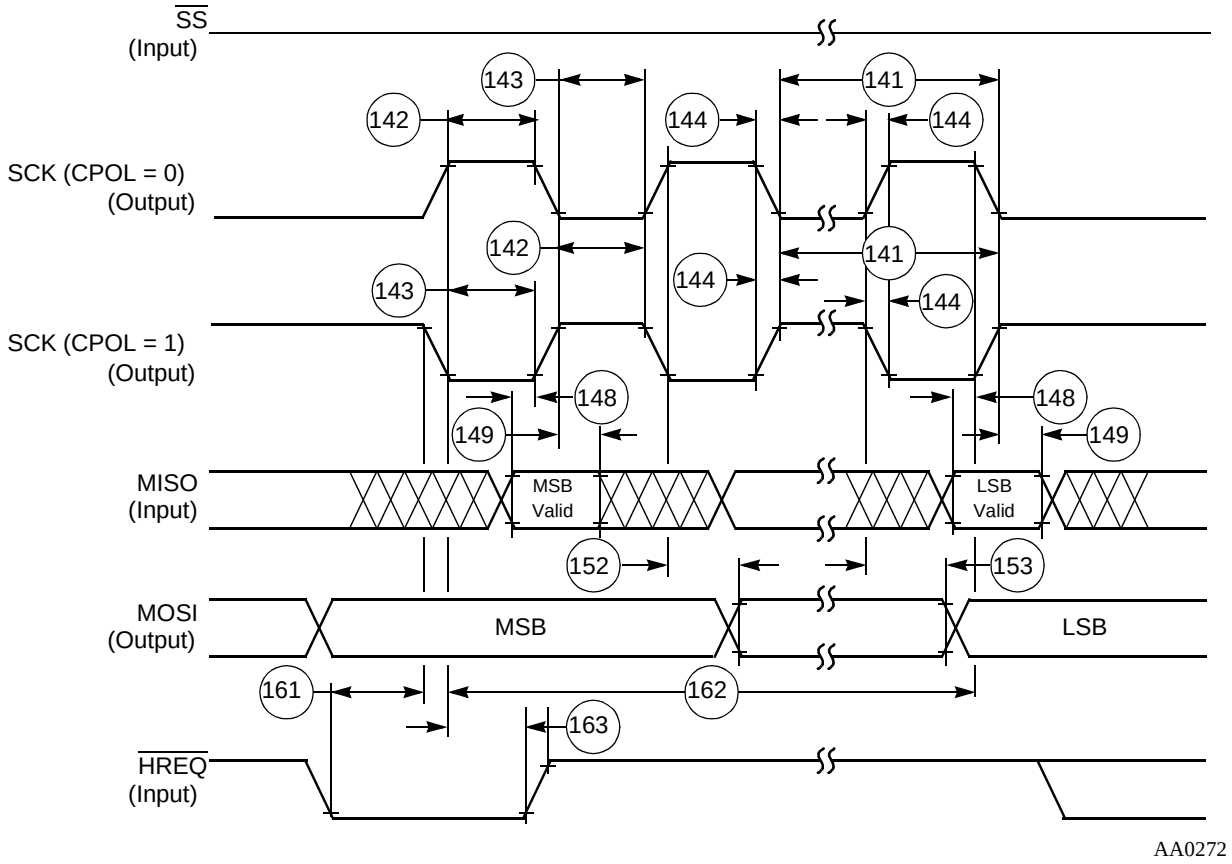


Figure 2-19. SPI Master Timing (CPHA = 1)

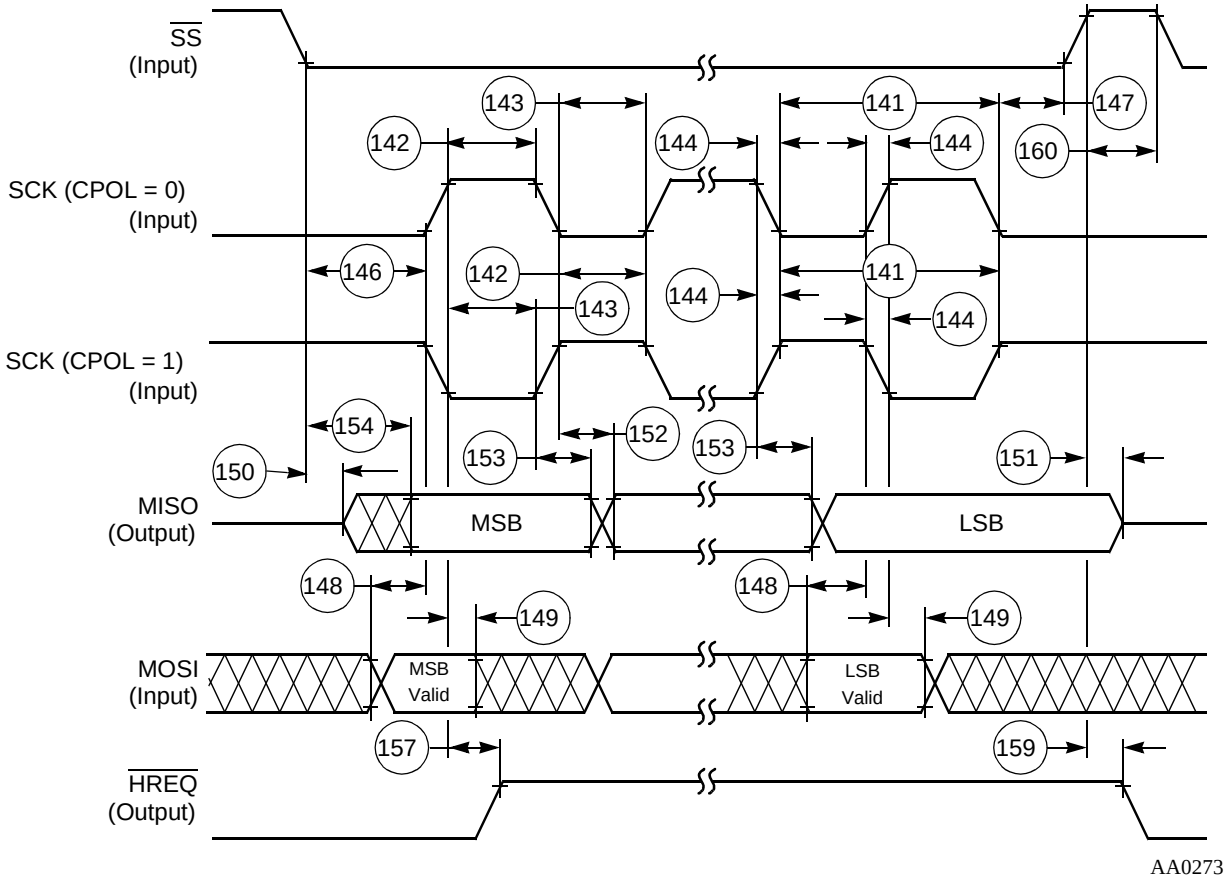


Figure 2-20. SPI Slave Timing (CPHA = 0)

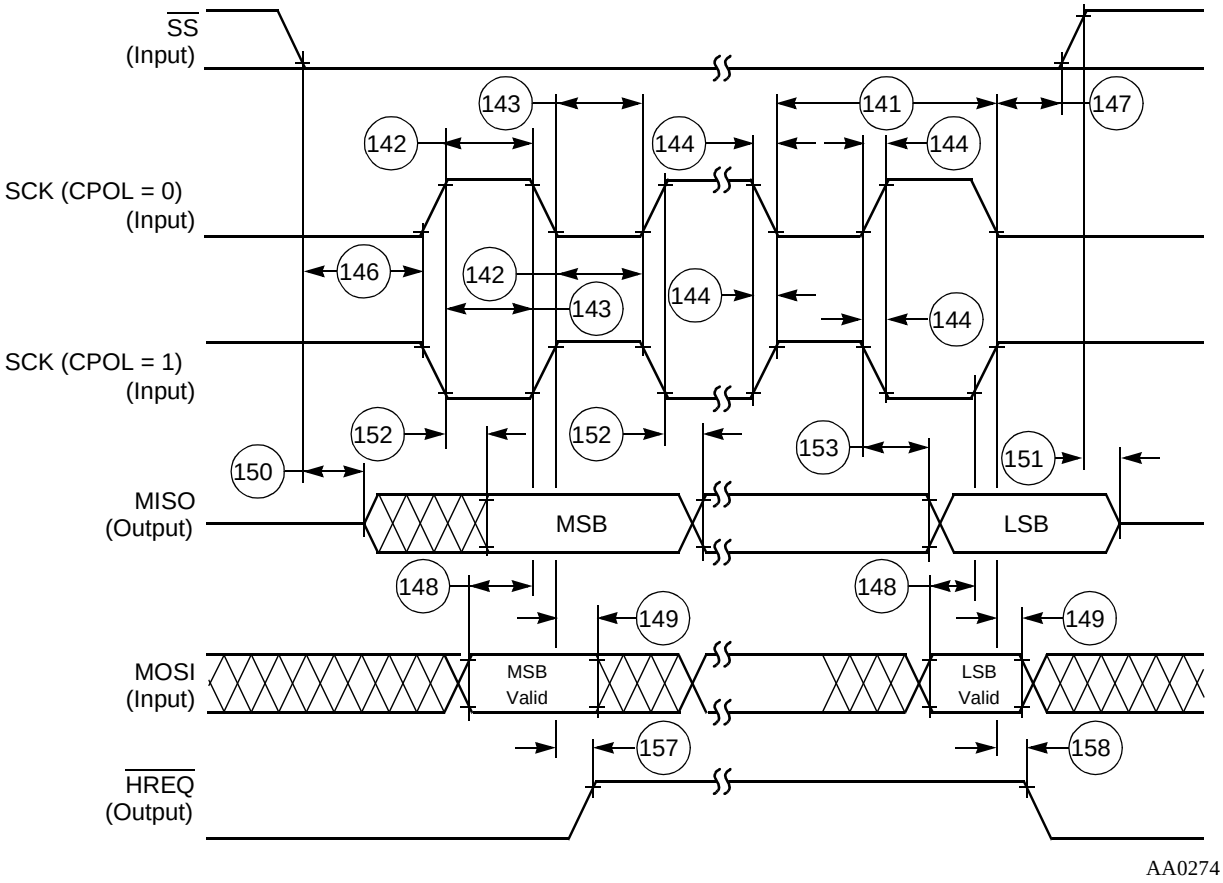


Figure 2-21. SPI Slave Timing (CPHA = 1)

SERIAL HOST INTERFACE (SHI) I2C PROTOCOL TIMING

Table 2-18. SHI I2C Protocol Timing

Standard I2C*							
No.	Characteristics	Symbol/ Expression	Standard-Mode		Fast-Mode		Unit
			Min	Max	Min	Max	
	Tolerable spike width on SCL or SDA						
	Filters bypassed	—	—	0	—	0	ns
	Narrow filters enabled		—	50	—	50	ns
	Wide filters enabled		—	100	—	100	ns
171	SCL clock frequency	F_{SCL}	—	100	—	400	kHz
172	Bus free time	T_{BUF}	4.7	—	1.3	—	µs
173	Start condition set-up time	$T_{SU;STA}$	4.7	—	0.6	—	µs
174	Start condition hold time	$T_{HD;STA}$	4.0	—	0.6	—	µs
175	SCL low period	T_{LOW}	4.7	—	1.3	—	µs
176	SCL high period	T_{HIGH}	4.0	—	1.3	—	µs
177	SCL and SDA rise time	T_R	—	1000	$20 + 0.1 \times C_b$	300	ns
178	SCL and SDA fall time	T_F	—	300	$20 + 0.1 \times C_b$	300	ns
179	Data set-up time	$T_{SU;DAT}$	250	—	100	—	ns
180	Data hold time	$T_{HD;DAT}$	0.0	—	0.0	0.9	µs
181	Stop condition set-up time	$T_{SU;STO}$	4.0	—	0.6	—	µs
182	Capacitive load for each line	C_b	—	400	—	400	pF
183	DSP clock frequency	F_{DSP}					
	Filters bypassed		10.6	—	28.5	—	MHz
	Narrow filters enabled		11.8	—	39.7	—	MHz
	Wide filters enabled		13.1	—	61.0	—	MHz

Table 2-18. SHI I2C Protocol Timing (Continued)

Standard I2C*							
No.	Characteristics	Symbol/ Expression	Standard-Mode		Fast-Mode		Unit
			Min	Max	Min	Max	
184	$\overline{\text{HREQ}}$ in deassertion to last SCL edge ($\overline{\text{HREQ}}$ in set-up time)	$t_{SU;RQI}$	0.0	—	0.0	—	ns
186	First SCL sampling edge to $\overline{\text{HREQ}}$ output deassertion[2]	$T_{NG;RQO}$					ns
	Filters bypassed	$2 \times T_C + 30$	—	50	—	50	
	Narrow filters enabled	$2 \times T_C + 120$	—	140	—	140	
	Wide filters enabled	$2 \times T_C + 208$	—	228	—	228	
187	Last SCL edge to HREQ output not deasserted[2]	$T_{AS;RQO}$					ns
	Filters bypassed	$2 \times T_C + 30$	50	—	50	—	
	Narrow filters enabled	$2 \times T_C + 80$	100	—	100	—	
	Wide filters enabled	$2 \times T_C + 135$	155	—	155	—	
188	HREQ in assertion to first SCL edge	$T_{AS;RQI}$ $0.5 \times T_I 2_{CCP}$ - $0.5 \times T_C$ - 21					ns
	Filters bypassed		4327	—	927	—	
	Narrow filters enabled		4282	—	882	—	
	Wide filters enabled		4238	—	838	—	
Note: R_P (min) = 1.5 k¾							

Programming the Serial Clock

The programmed serial clock cycle, T_{I^2CCP}, is specified by the value of the HDM[5:0] and HRS bits of the HCKR (SHI clock control register).

The expression for T_{I^2CCP} is

$$T_{I^2CCP} = [T_C \times 2 \times (HDM[7:0] + 1) \times (7 \times (1 - HRS) + 1)]$$

where

- HRS is the prescaler rate select bit. When HRS is cleared, the fixed divide-by-eight prescaler is operational. When HRS is set, the prescaler is bypassed.
- HDM[7:0] are the divider modulus select bits.
- A divide ratio from 1 to 64 (HDM[5:0] = 0 to $3F) may be selected.

In I^2C mode, the user may select a value for the programmed serial clock cycle from

$6 \times T_C$ (if HDM[5:0] = $02 and HRS = 1)

to

$4096 \times T_C$ (if HDM[7:0] = $FF and HRS = 0)

The programmed serial clock cycle (T_{I^2CCP}), SCL rise time (T_R), and the filters selected should be chosen in order to achieve the desired SCL frequency, as shown in **Table 2-23**.

Table 2-19. SCL Serial Clock Cycle generated as Master

Filters bypassed	$T_{I^2CCP} + 2.5 \times T_C + 45ns + T_R$
Narrow filters enabled	$T_{I^2CCP} + 2.5 \times T_C + 135ns + T_R$
Wide filters enabled	$T_{I^2CCP} + 2.5 \times T_C + 223ns + T_R$

EXAMPLE:

For DSP clock frequency of 100 MHz (i.e. T_C = 10ns), operating in a standard-mode I^2C environment (F_{SCL} = 100 KHz (i.e. T_{SCL} = 10µs), T_R = 1000ns), with filters bypassed

T_{I^2CCP} = 10µs - 2.5×10ns - 45ns - 1000ns = 8930ns

Choosing HRS = 0 gives

HDM[7:0] = 8930ns / (2× 10ns× 8) - 1 = 55.8

Thus the HDM[7:0] value should be programmed to $38 (=56).

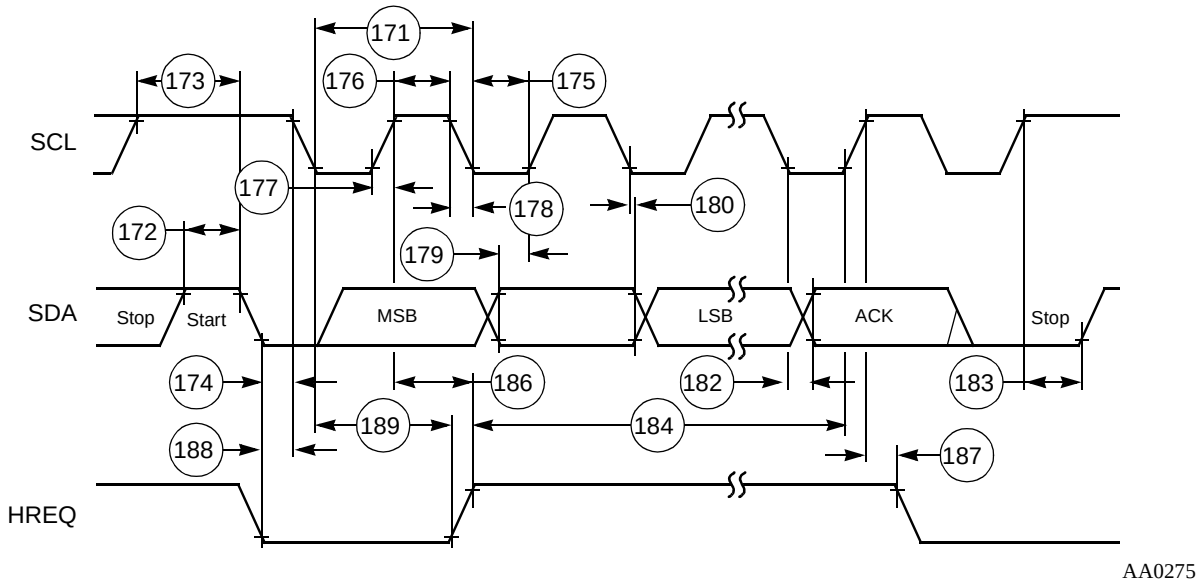


Figure 2-22. I²C Timing

ENHANCED SERIAL AUDIO INTERFACE TIMING

Table 2-20. Enhanced Serial Audio Interface Timing

No.	Characteristics[1, 2, 3]	Symbol	Expression	Min	Max	Condition[4]	Unit
430	Clock cycle[5]	t_{SSICC}	$4 \times T_C$ $3 \times T_C$ TXC:max[3*tc; t454]	40.0 30.0 40.0	— — —	i ck x ck x ck	ns
431	Clock high period • For internal clock • For external clock	—	$2 \times T_C - 10.0$ $1.5 \times T_C$	10.0 15.0	— —		ns
432	Clock low period • For internal clock • For external clock	—	$2 \times T_C - 10.0$ $1.5 \times T_C$	10.0 15.0	— —		ns
433	RXC rising edge to FSR out (bl) high	—	—	— —	37.0 22.0	x ck i ck a	ns
434	RXC rising edge to FSR out (bl) low	—	—	— —	37.0 22.0	x ck i ck a	ns
435	RXC rising edge to FSR out (wr) high[6]	—	—	— —	39.0 24.0	x ck i ck a	ns
436	RXC rising edge to FSR out (wr) low[6]	—	—	— —	39.0 24.0	x ck i ck a	ns
437	RXC rising edge to FSR out (wl) high	—	—	— —	36.0 21.0	x ck i ck a	ns
438	RXC rising edge to FSR out (wl) low	—	—	— —	37.0 22.0	x ck i ck a	ns
439	Data in setup time before RXC (SCK in synchronous mode) falling edge	—	—	0.0 19.0	— —	x ck i ck	ns
440	Data in hold time after RXC falling edge	—	—	5.0 3.0	— —	x ck i ck	ns
441	FSR input (bl, wr) high before RXC falling edge [6]	—	—	23.0 1.0	— —	x ck i ck a	ns
442	FSR input (wl) high before RXC falling edge	—	—	1.0 23.0	— —	x ck i ck a	ns

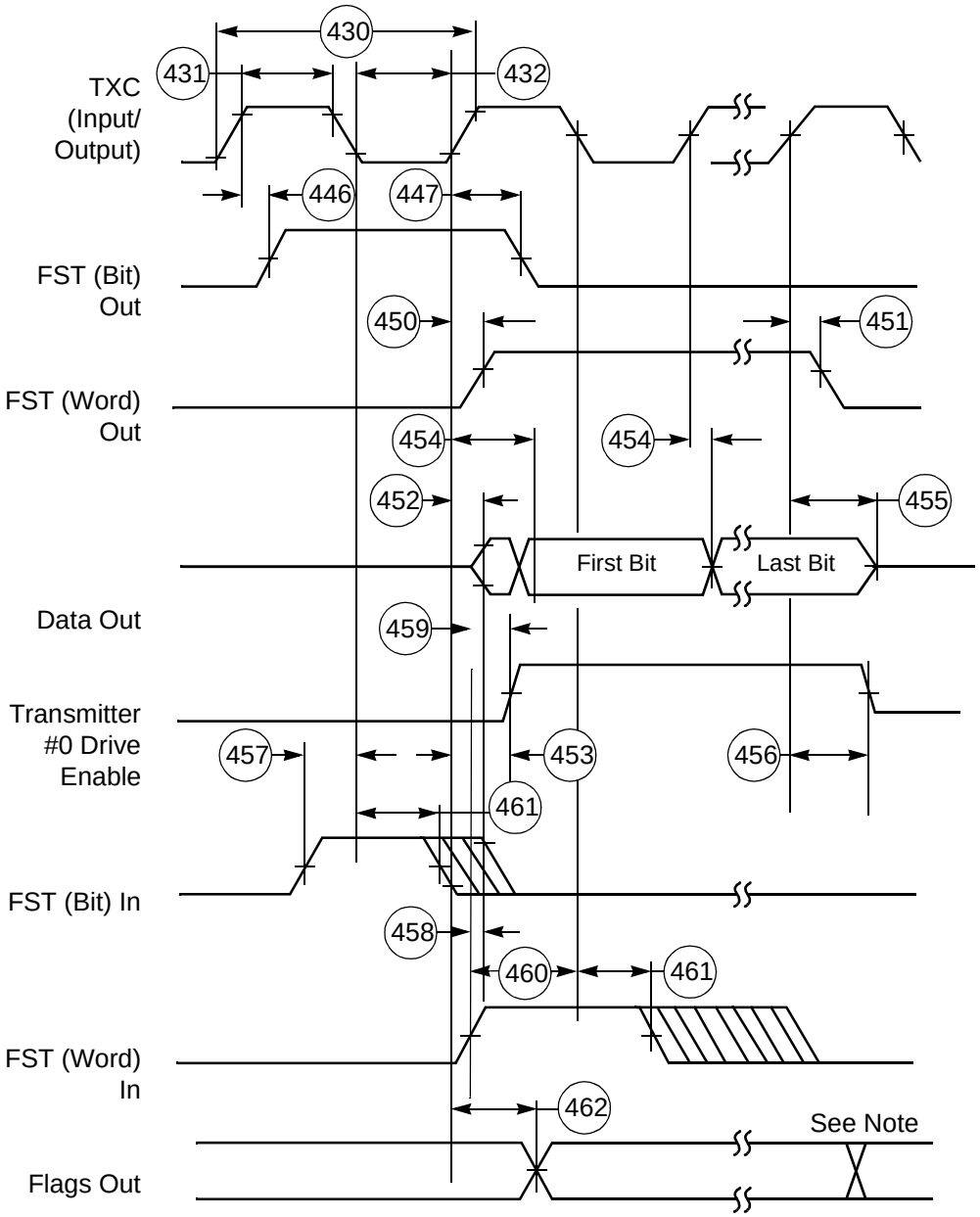
Table 2-20. Enhanced Serial Audio Interface Timing (Continued)

No.	Characteristics[1, 2, 3]	Symbol	Expression	Min	Max	Condition[4]	Unit
443	FSR input hold time after RXC falling edge	—	—	3.0 0.0	— —	x ck i ck a	ns
444	Flags input setup before RXC falling edge	–	—	0.0 19.0	— —	x ck i ck s	ns
445	Flags input hold time after RXC falling edge	—	—	6.0 0.0	— —	x ck i ck s	ns
446	TXC rising edge to FST out (bl) high	—	—	— —	29.0 15.0	x ck i ck	ns
447	TXC rising edge to FST out (bl) low	—	—	— —	31.0 17.0	x ck i ck	ns
448	TXC rising edge to FST out (wr) high[6]	—	—	— —	31.0 17.0	x ck i ck	ns
449	TXC rising edge to FST out (wr) low[6]	—	—	— —	33.0 19.0	x ck i ck	ns
450	TXC rising edge to FST out (wl) high	—	—	— —	30.0 16.0	x ck i ck	ns
451	TXC rising edge to FST out (wl) low	—	—	— —	31.0 17.0	x ck i ck	ns
452	TXC rising edge to data out enable from high impedance	—	—	— —	31.0 17.0	x ck i ck	ns
453	TXC rising edge to transmitter #0 drive enable assertion	—	—	— —	34.0 20.0	x ck i ck	ns
454	TXC rising edge to data out valid	—	$23 + 0.5 \times T_C$ 21.0	— —	28.0 21.0	x ck i ck	ns
455	TXC rising edge to data out high impedance[7]	—	—	— —	31.0 16.0	x ck i ck	ns
456	TXC rising edge to transmitter #0 drive enable deassertion[7]	—	—	— —	34.0 20.0	x ck i ck	ns
457	FST input (bl, wr) setup time before TXC falling edge[6]	—	—	2.0 21.0	— —	x ck i ck	ns
458	FST input (wl) to data out enable from high impedance	–	—	—	27.0	—	ns

Table 2-20. Enhanced Serial Audio Interface Timing (Continued)

No.	Characteristics[1, 2, 3]	Symbol	Expression	Min	Max	Cond-ition[4]	Unit
459	FST input (wl) to transmitter #0 drive enable assertion	—	—	—	31.0	—	ns
460	FST input (wl) setup time before TXC falling edge	—	—	2.0 21.0	— —	x ck i ck	ns
461	FST input hold time after TXC falling edge	—	—	4.0 0.0	— —	x ck i ck	ns
462	Flag output valid after TXC rising edge	—	—	— —	32.0 18.0	x ck i ck	ns
463	HCKR/HCKT clock cycle	—	—	40.0	—		ns
464	HCKT input rising edge to TXC output	—	—	—	27.5		ns
465	HCKR input rising edge to RXC output	—	—	—	27.5		ns

Notes:
1. V_{CC} = 3.16 V ± 0.16 V; T_J = 0°C to +105°C, C_L = 50 pF
2. i ck = internal clock
   x ck = external clock
   i ck a = internal clock, asynchronous mode
   (asynchronous implies that TXC and RXC are two different clocks)
   i ck s = internal clock, synchronous mode
   (synchronous implies that TXC and RXC are the same clock)
3. bl = bit length
   wl = word length
   wr = word length relative
4. TXC(SCKT pin) = transmit clock
   RXC(SCKR pin) = receive clock
   FST(FST pin) = transmit frame sync
   FSR(FSR pin) = receive frame sync
   HCKT(HCKT pin) = transmit high speed clock
   HCKR(HCKR pin) = receive high speed clock
5. For the internal clock, the external clock cycle is defined by Icyc and the ESAI control register.
6. The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but spreads from one serial clock before first bit clock (same as bit length frame sync signal), until the one before last bit clock of the first word in frame.
7. Periodically sampled and not 100% tested



Note: In network mode, output flag transitions can occur at the start of each time slot within the frame. In normal mode, the output flag state is asserted for the entire frame period.

AA0490

Figure 2-23. ESAI Transmitter Timing

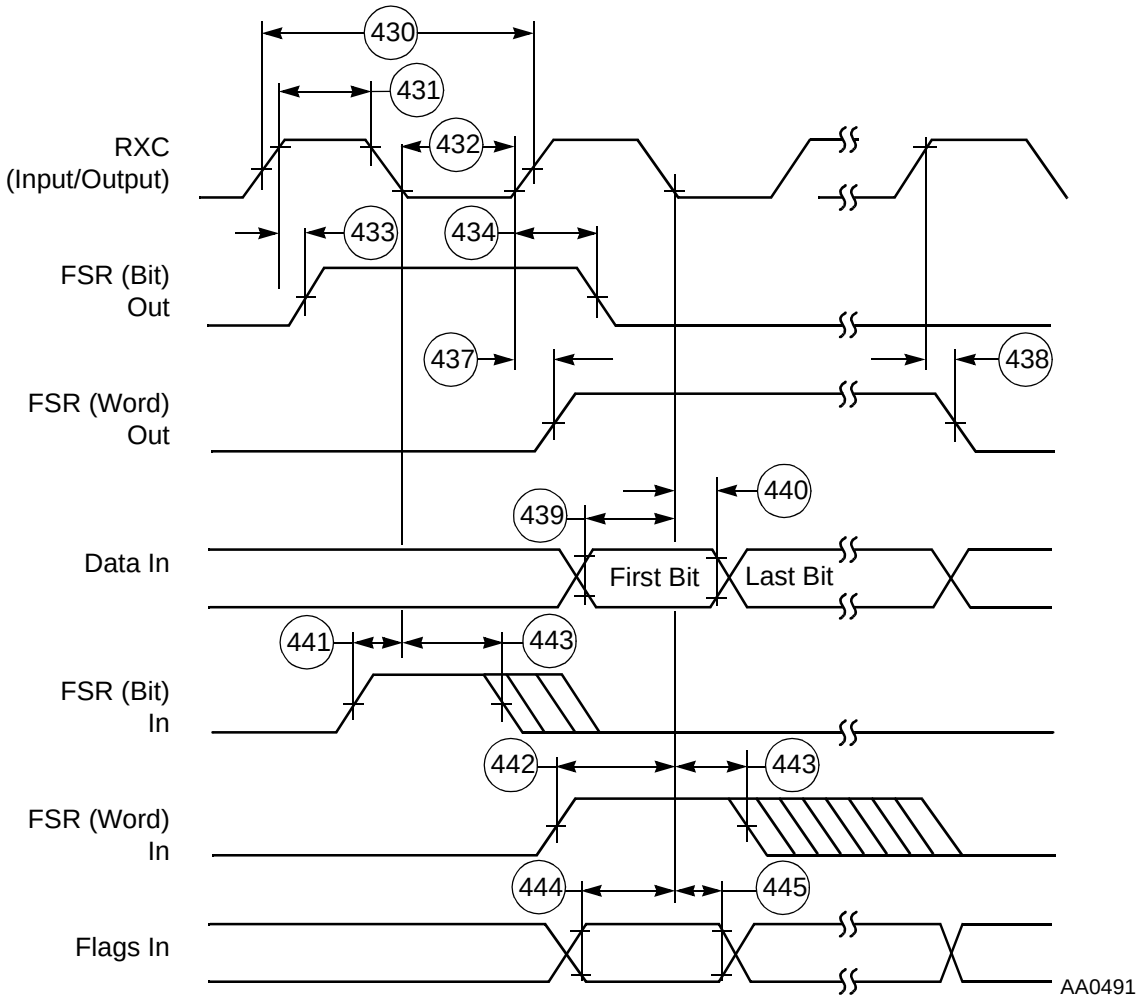


Figure 2-24. ESAI Receiver Timing

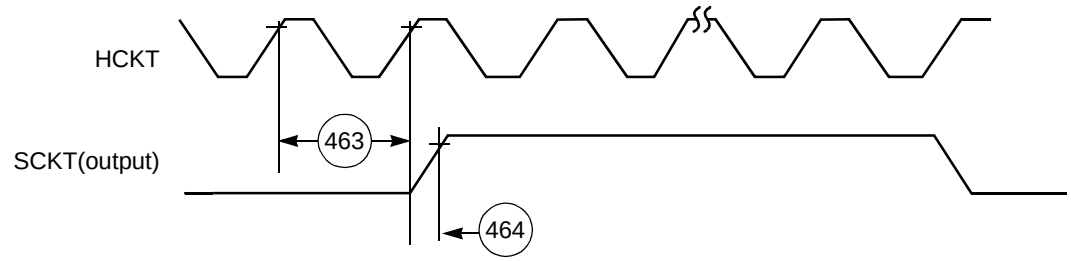


Figure 2-25. ESAI HCKT Timing

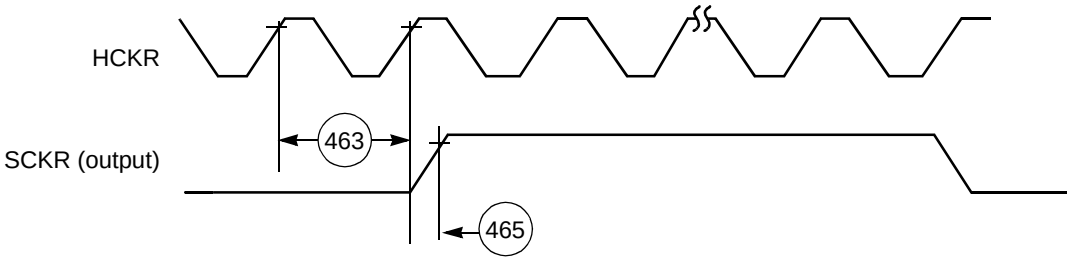


Figure 2-26. ESAI HCKR Timing

GPIO TIMING

Table 2-21. GPIO Timing

No.	Characteristics[1]	Expression	Min	Max	Unit
490[2]	EXTAL edge to GPIO out valid (GPIO out delay time)		—	32.8	ns
491	EXTAL edge to GPIO out not valid (GPIO out hold time)		4.8	—	ns
492	GPIO In valid to EXTAL edge (GPIO in set-up time)		10.2	—	ns
493	EXTAL edge to GPIO in not valid (GPIO in hold time)		1.8	—	ns
494[2]	Fetch to EXTAL edge before GPIO change	$6.75 \times T_C$-1.8	65.7	—	ns
495	GPIO out rise time	—	—	13	ns
496	GPIO out fall time	—	—	13	ns

Notes: 1. V_{CC} = 3.3 V ± 0.16 V; T_J = 0°C to +105°C, C_L = 50 pF
2. Valid only when PLL enabled with multiplication factor equal to one.

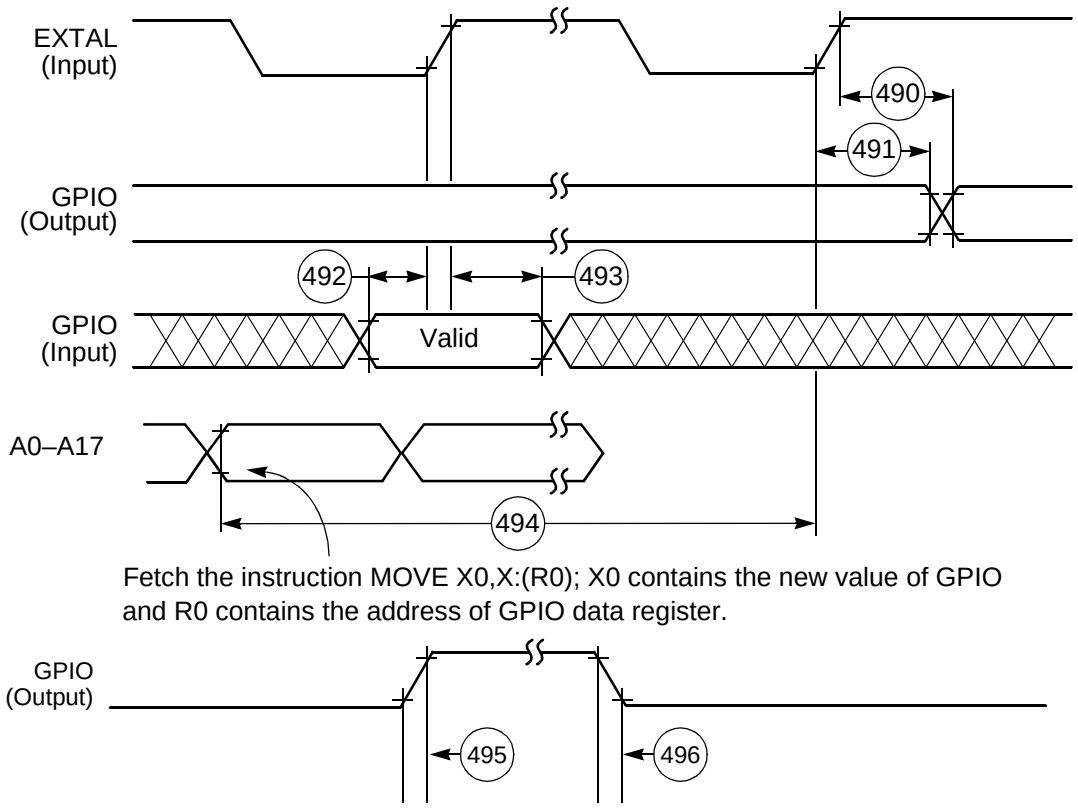


Figure 2-27. GPIO Timing

JTAG TIMING

Table 2-22. JTAG Timing

No.	Characteristics	All frequencies		Unit
		Min	Max	
500	TCK frequency of operation (1/($T_C \times 3$); maximum 22 MHz)	0.0	22.0	MHz
501	TCK cycle time in Crystal mode	45.0	—	ns
502	TCK clock pulse width measured at 1.5 V	20.0	—	ns
503	TCK rise and fall times	0.0	3.0	ns
504	Boundary scan input data setup time	5.0	—	ns
505	Boundary scan input data hold time	24.0	—	ns
506	TCK low to output data valid	0.0	40.0	ns
507	TCK low to output high impedance	0.0	40.0	ns
508	TMS, TDI data setup time	5.0	—	ns
509	TMS, TDI data hold time	25.0	—	ns
510	TCK low to TDO data valid	0.0	44.0	ns
511	TCK low to TDO high impedance	0.0	44.0	ns

Notes: 1. V_{CC} = 3.3 V ± 0.16 V; T_J = 0°C to +105°C, C_L = 50 pF
2. All timings apply to OnCE module data transfers because it uses the JTAG port as an interface.

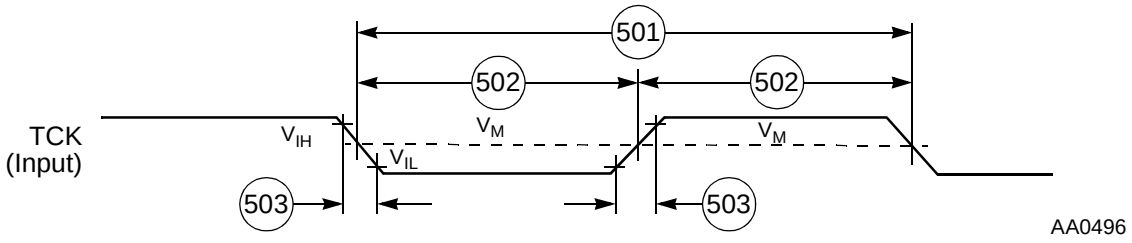


Figure 2-28. Test Clock Input Timing Diagram

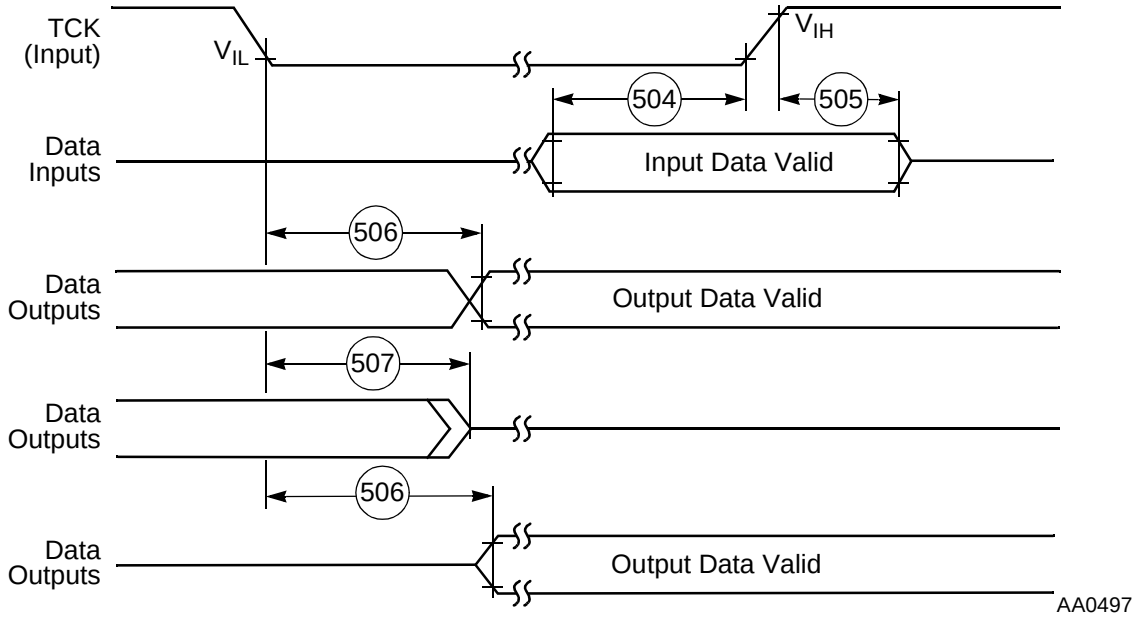


Figure 2-29. Boundary Scan (JTAG) Timing Diagram

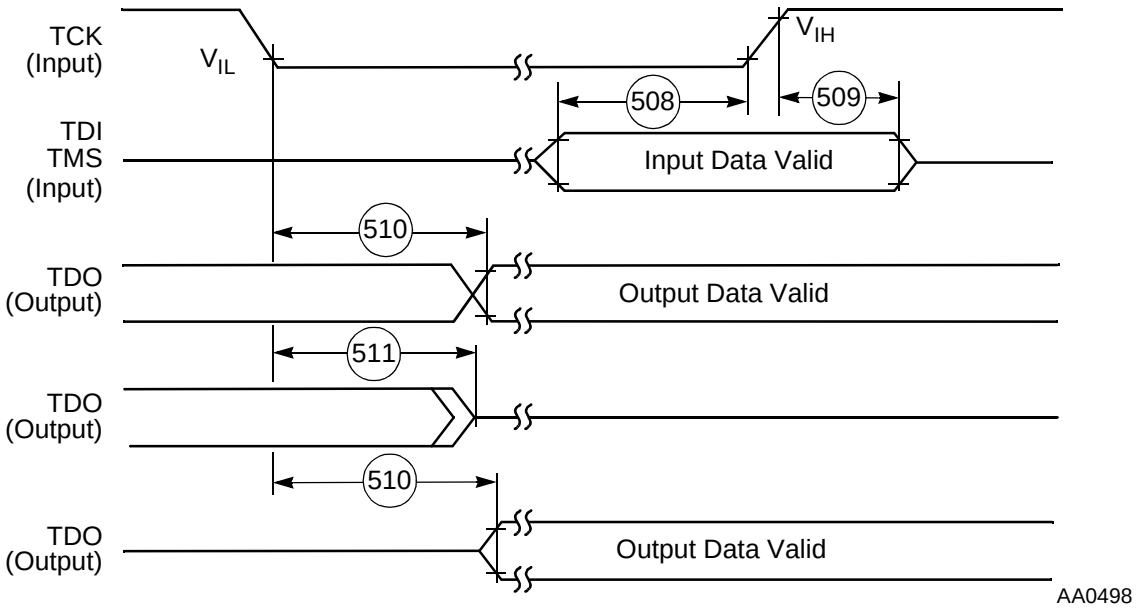


Figure 2-30. Test Access Port Timing Diagram

SECTION 3

PACKAGING

PIN-OUT AND PACKAGE INFORMATION

This section provides information about the available package for this product, including diagrams of the package pinouts and tables describing how the signals described in **Section 1** are allocated for the package. The DSP56364 is available in a 100-pin TQFP package. Tables 3-1 and 3-2 show the pin/name assignments for the packages.

TQFP Package Description

Top view of the 100-pin TQFP package is shown in **Figure 3-1** with its pin-outs. The 100-pin TQFP package mechanical drawing is shown in **Figure 3-2**.

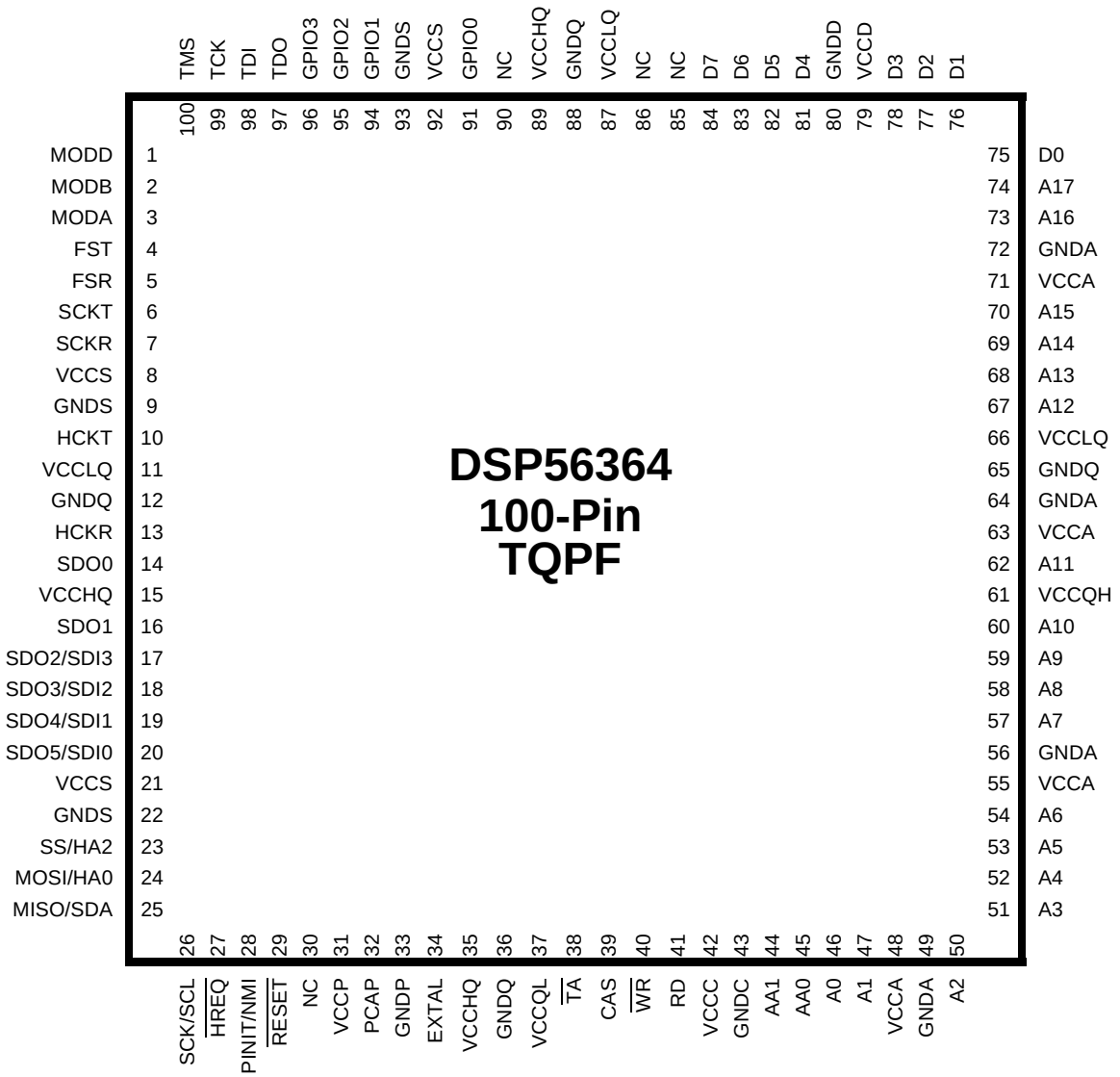


Figure 3-1 DSP56364 100-Pin Thin Quad Flat Pack (TQFP), Top View

Table 3-1 DSP56364 100-Pin TQFP Signal Identification by Pin Number

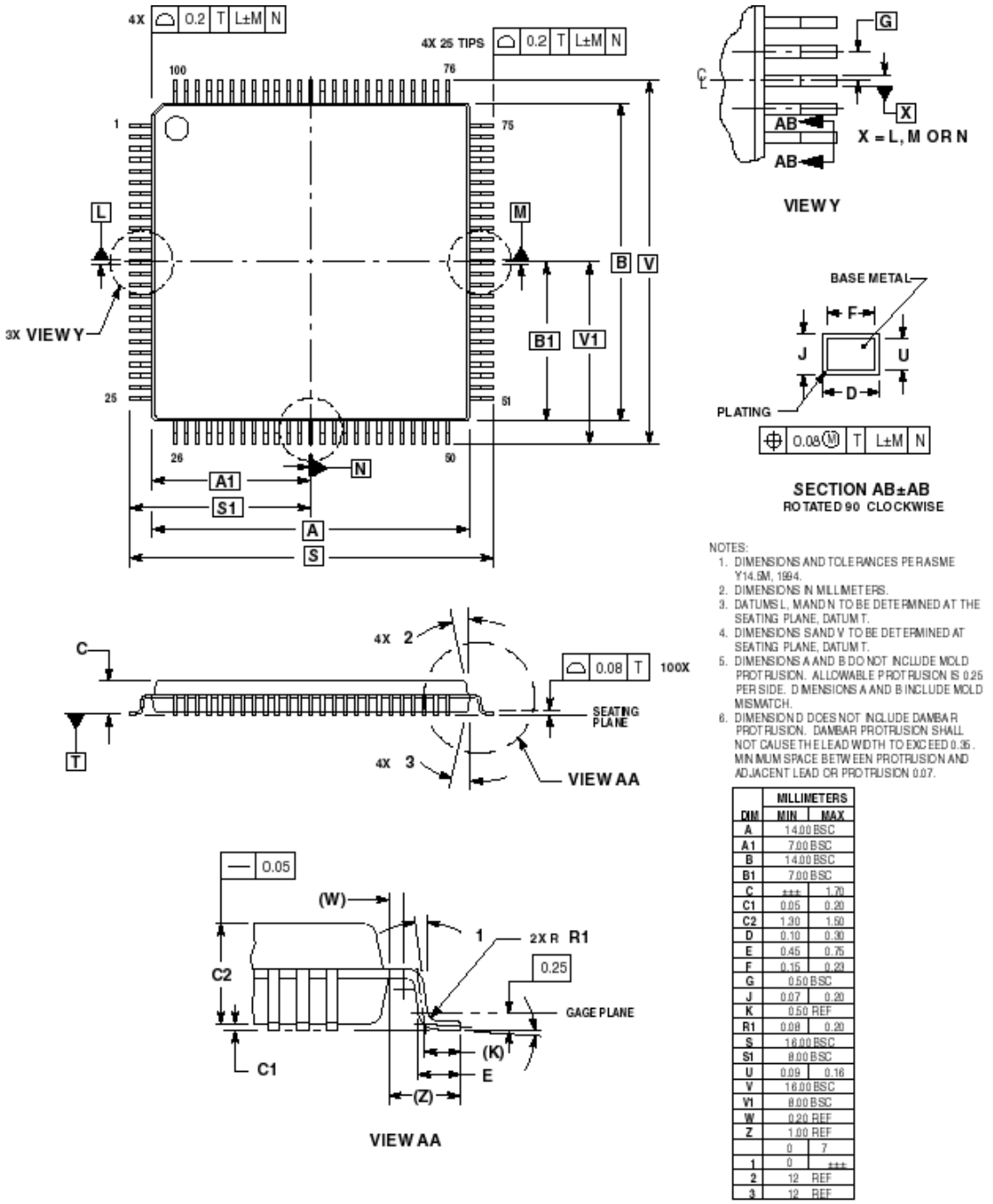
Pin No.	Signal Name	Pin No.	Signal Name	Pin No.		Pin No.	Signal Name
1	MODD/$\overline{\text{IRQD}}$	26	SCK/SCL	51	A3	76	D1
2	MODB/$\overline{\text{IRQB}}$	27	$\overline{\text{HREQ}}$	52	A4	77	D2
3	MODA/$\overline{\text{IRQA}}$	28	PINIT/$\overline{\text{NMI}}$	53	A5	78	D3
4	FST	29	$\overline{\text{RESET}}$	54	A6	79	VCCD
5	FSR	30	No Connect	55	VCCA	80	GNDD
6	SCKT	31	VCCP	56	GNDA	81	D4
7	SCKR	32	PCAP	57	A7	82	D5
8	VCCS	33	GNDP	58	A8	83	D6
9	GNDS	34	EXTAL	59	A9	84	D7
10	HCKT	35	VCCHQ	60	A10	85	No Connect
11	VCCLQ	36	GNDQ	61	VCCHQ	86	No Connect
12	GNDQ	37	VCCLQ	62	A11	87	VCCLQ
13	HCKR	38	$\overline{\text{TA}}$	63	VCCA	88	GNDQ
14	SDO0	39	$\overline{\text{CAS}}$	64	GNDA	89	VCCHQ
15	VCCHQ	40	$\overline{\text{WR}}$	65	GNDQ	90	No Connect
16	SDO1	41	$\overline{\text{RD}}$	66	VCCLQ	91	GPIO0
17	SDO2/SDI3	42	VCCC	67	A12	92	VCCS
18	SDO3/SDI2	43	GNDC	68	A13	93	GNDS
19	SDO4/SDI1	44	AA1/$\overline{\text{RAS1}}$	69	A14	94	GPIO1
20	SDO5/SDI0	45	AA0/$\overline{\text{RAS0}}$	70	A15	95	GPIO2
21	VCCS	46	A0	71	VCCA	96	GPIO3
22	GNDS	47	A1	72	GNDA	97	TDO
23	$\overline{\text{SS}}$/HA2	48	VCCQ	73	A16	98	TDI
24	MOSI/HA0	49	GNDQ	74	A17	99	TCK
25	MISO/SDA	50	A2	75	D0	100	TMS

Note: Signal names are based on configured functionality. Most pins supply a single signal. Some pins provide a signal with dual functionality, such as the MODx/$\overline{\text{IRQx}}$ pins that select an operating mode after $\overline{\text{RESET}}$ is deasserted, but act as interrupt lines during operation.

Table 3-2 DSP56364 100-Pin TQFP Signal Identification by Name

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
A0	46	D4	81	HCKR	13	SDO4/SDI1	19
A1	47	D5	82	HCKT	10	TA	38
A10	60	D6	83	$\overline{\text{HREQ}}$	27	TCK	99
A11	62	D7	84	MISO/SDA	25	TDI	98
A12	67	EXTAL	34	MODA/$\overline{\text{IRQA}}$	3	TD0	97
A13	68	FSR	5	MODB/$\overline{\text{IRQB}}$	2	TMS	100
A14	69	FST	4	MODD/$\overline{\text{IRQD}}$	1	VCCA	48
A15	70	GNDA	49	MOSI/HA0	24	VCCA	55
A16	73	GNDA	56	No Connect	30	VCCA	63
A17	74	GNDA	64	No Connect	85	VCCA	71
A2	50	GNDA	72	No Connect	86	VCCC	42
A3	51	GNDC	43	No Connect	90	VCCD	79
A4	52	GNDD	80	PCAP	32	VCCHQ	15
A5	53	GNDP	33	PINIT/$\overline{\text{NMI}}$	28	VCCHQ	35
A6	54	GNDQ	12	$\overline{\text{RD}}$	41	VCCHQ	61
A7	57	GNDQ	36	$\overline{\text{RESET}}$	29	VCCHQ	89
A8	58	GNDQ	65	SCK/SCL	26	VCCLQ	11
A9	59	GNDQ	88	SCKR	7	VCCLQ	37
AA0	45	GNDS	9	SCKT	6	VCCLQ	66
AA1	44	GNDS	22	SDO0	14	VCCLQ	87
$\overline{\text{CAS}}$	39	GNDS	93	SDO1	16	VCCP	31
D0	75	GPIO0	91	SDO5/SDI0	20	VCCS	8
D1	76	GPIO1	94	$\overline{\text{SS}}$/HA2	23	VCCS	21
D2	77	GPIO2	95	SDO2/SDI3	17	VCCS	92
D3	78	GPIO3	96	SDO3/SDI2	18	$\overline{\text{WR}}$	40

TQFP Package Mechanical Drawing



NOTES:
1. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DATUMS L, M AND N TO BE DETERMINED AT THE SEATING PLANE, DATUM T.
4. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE, DATUM T.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B INCLUDE MOLD MISMATCH.
6. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07.

	MILLIMETERS	
DIM	MIN	MAX
A	14.00 BSC	
A1	7.00 BSC	
B	14.00 BSC	
B1	7.00 BSC	
C	---	1.70
C1	0.05	0.20
C2	1.30	1.50
D	0.10	0.30
E	0.45	0.75
F	0.15	0.23
G	0.50 BSC	
J	0.07	0.20
K	0.50 REF	
R1	0.08	0.20
S	16.00 BSC	
S1	8.00 BSC	
U	0.09	0.16
V	16.00 BSC	
V1	8.00 BSC	
W	0.20 REF	
Z	1.00 REF	
	0	7
1	0	---
2	12 REF	
3	12 REF	

CASE 983±02
ISSUE E

DATE 01/30/96

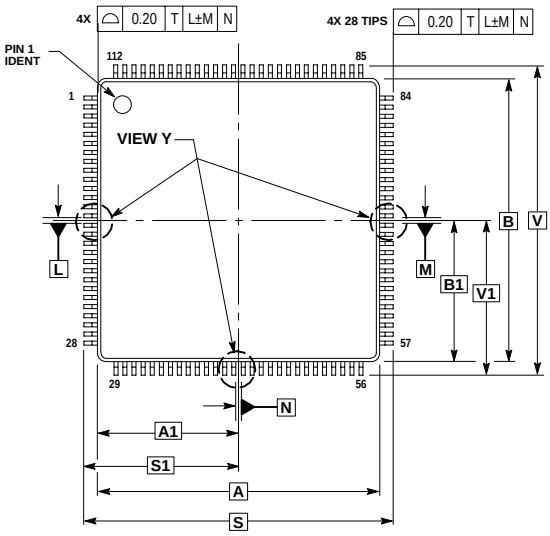
Figure 3-2 DSP56364 100-pin TQFP Package

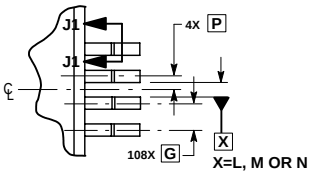
ORDERING DRAWINGS

The detailed package drawing is available on the Motorola web page at:

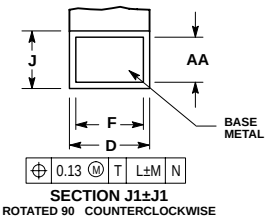
http://mot.sps.com/cgi-bin/cases

Use package 983 for the search.

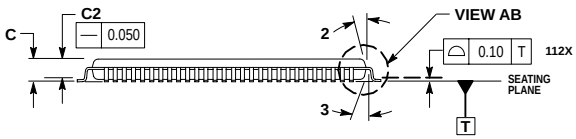


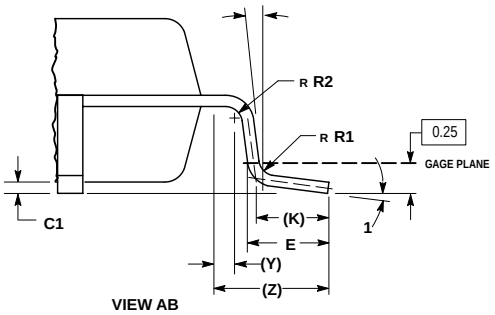


VIEW Y



SECTION J1±J1
ROTATED 90 COUNTERCLOCKWISE





VIEW AB

NOTES:
1. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DATUMS L, M AND N TO BE DETERMINED AT SEATING PLANE, DATUM T.
4. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE, DATUM T.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B INCLUDE MOLD MISMATCH.
6. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.46.

	MILLIMETERS	
DIM	MIN	MAX
A	20.000 BSC	
A1	10.000 BSC	
B	20.000 BSC	
B1	10.000 BSC	
C	---	1.600
C1	0.050	0.150
C2	1.350	1.450
D	0.270	0.370
E	0.450	0.750
F	0.270	0.330
G	0.650 BSC	
J	0.090	0.170
K	0.500 REF	
P	0.325 BSC	
R1	0.100	0.200
R2	0.100	0.200
S	22.000 BSC	
S1	11.000 BSC	
V	22.000 BSC	
V1	11.000 BSC	
Y	0.250 REF	
Z	1.000 REF	
AA	0.090	0.160
	0°	8°
1	3°	7°
2	11°	13°
3	11°	13°

CASE 987±01
ISSUE A

DATE 01/30/96

SECTION 4

DESIGN CONSIDERATIONS

THERMAL DESIGN CONSIDERATIONS

An estimation of the chip junction temperature, T_J, in °C can be obtained from the following equation:

$$T_J = T_A + (P_D \times R_{\theta JA})$$

Where: T_A = ambient temperature °C
R_{qJA} = package junction-to-ambient thermal resistance °C/W
P_D = power dissipation in package W

Historically, thermal resistance has been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance.

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

Where: $R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W
$R_{\theta JC}$ = package junction-to-case thermal resistance °C/W
$R_{\theta CA}$ = package case-to-ambient thermal resistance °C/W

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board (PCB), or otherwise change the thermal dissipation capability of the area surrounding the device on a PCB. This model is most useful for ceramic packages with heat sinks; some 90% of the heat flow is dissipated through the case to the heat sink and out to the ambient environment. For ceramic packages, in situations where the heat flow is split between a path to the case and an alternate path through the PCB, analysis of the device thermal performance may need the additional modeling capability of a system level thermal simulation tool.

The thermal performance of plastic packages is more dependent on the temperature of the PCB to which the package is mounted. Again, if the estimations obtained from $R_{\theta JA}$ do not satisfactorily answer whether the thermal performance is adequate, a system level model may be appropriate.

A complicating factor is the existence of three common ways for determining the junction-to-case thermal resistance in plastic packages.

- To minimize temperature variation across the surface, the thermal resistance is measured from the junction to the outside surface of the package (case) closest to the chip mounting area when that surface has a proper heat sink.
- To define a value approximately equal to a junction-to-board thermal resistance, the thermal resistance is measured from the junction to where the leads are attached to the case.
- If the temperature of the package case (T_T) is determined by a thermocouple, the thermal resistance is computed using the value obtained by the equation $(T_J - T_T)/P_D$.

As noted above, the junction-to-case thermal resistances quoted in this data sheet are determined using the first definition. From a practical standpoint, that value is also suitable for determining the junction temperature from a case thermocouple reading in forced convection environments. In natural convection, using the junction-to-case thermal resistance to estimate junction temperature from a thermocouple reading on the case of the package will estimate a junction temperature slightly hotter than actual temperature. Hence, the new thermal metric, thermal characterization parameter or Ψ_{JT}, has been defined to be $(T_J - T_T)/P_D$. This value gives a better estimate of the junction temperature in natural convection when using the surface temperature of the package. Remember that surface temperature readings of packages are subject to significant errors caused by inadequate attachment of the sensor to the surface and to errors caused by heat loss to the sensor. The recommended technique is to attach a 40-gauge thermocouple wire and bead to the top center of the package with thermally conductive epoxy.

ELECTRICAL DESIGN CONSIDERATIONS

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields. However, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). The suggested value for a pullup or pulldown resistor is 10 k ohm.

Use the following list of recommendations to assure correct DSP operation:

- Provide a low-impedance path from the board power supply to each V_{CC} pin on the DSP and from the board ground to each GND pin.
- Use at least six 0.01–0.1 µF bypass capacitors positioned as close as possible to the four sides of the package to connect the V_{CC} power source to GND.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{CC} and GND pins are less than 1.2 cm (0.5 inch) per capacitor lead.
- Use at least a four-layer PCB with two inner layers for V_{CC} and GND.
- Because the DSP output signals have fast rise and fall times, PCB trace lengths should be minimal. This recommendation particularly applies to the address and data buses as well as the $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQD}}$, and $\overline{\text{TA}}$ pins. Maximum PCB trace lengths on the order of 15 cm (6 inches) are recommended.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{CC} and GND circuits.
- All inputs must be terminated (i.e., not allowed to float) using CMOS levels, except for the three pins with internal pull-up resistors (TMS, TDI, TCK).
- Take special care to minimize noise levels on the V_{CCP} and GND_P pins.
- If multiple DSP56364 devices are on the same board, check for cross-talk or excessive spikes on the supplies due to synchronous operation of the devices.
- RESET must be asserted when the chip is powered up. A stable EXTAL signal must be supplied before deassertion of RESET.

- At power-up, ensure that the voltage difference between the 5 V tolerant pins and the chip V_{CC} never exceeds 3.95 V.

POWER CONSUMPTION CONSIDERATIONS

Power dissipation is a key issue in portable DSP applications. Some of the factors which affect current consumption are described in this section. Most of the current consumed by CMOS devices is alternating current (ac), which is charging and discharging the capacitances of the pins and internal nodes.

Current consumption is described by the following formula:

$$I = C \times V \times f$$

where C = node/pin capacitance
V = voltage swing
f = frequency of node/pin toggle

Example 1 Current Consumption

For a Port A address pin loaded with 50 pF capacitance, operating at 3.3 V, and with a 100 MHz clock, toggling at its maximum possible rate (50 MHz), the current consumption is

$$I = 50 \times 10^{-12} \times 3.3 \times 50 \times 10^{6} = 8.25\text{mA}$$

The maximum internal current (I_{CCI}max) value reflects the typical possible switching of the internal buses on best-case operation conditions, which is not necessarily a real application case. The typical internal current (I_{CCItyp}) value reflects the average switching of the internal buses on typical operating conditions.

For applications that require very low current consumption, do the following:

- Set the EBD bit when not accessing external memory.
- Minimize external memory accesses and use internal memory accesses.
- Minimize the number of pins that are switching.
- Minimize the capacitive load on the pins.
- Connect the unused inputs to pull-up or pull-down resistors.
- Disable unused peripherals.

One way to evaluate power consumption is to use a current per MIPS measurement methodology to minimize specific board effects (i.e., to compensate for measured board current not caused by the DSP). A benchmark power consumption test algorithm is listed in **Appendix A**. Use the test algorithm, specific test current measurements, and the following equation to derive the current per MIPS value.

$$I/MIPS = I/MHz = (I_{typF2} - I_{typF1})/(F2 - F1)$$

where : I_{typF2} = current at F2
I_{typF1} = current at F1
F2 = high frequency (any specified operating frequency)
F1 = low frequency (any specified operating frequency lower than F2)

Note: F1 should be significantly less than F2. For example, F2 could be 66 MHz and F1 could be 33 MHz. The degree of difference between F1 and F2 determines the amount of precision with which the current rating can be determined for an application.

PLL PERFORMANCE ISSUES

The following explanations should be considered as general observations on expected PLL behavior. There is no testing that verifies these exact numbers. These observations were measured on a limited number of parts and were not verified over the entire temperature and voltage ranges.

Input (EXTAL) Jitter Requirements

The allowed jitter on the frequency of EXTAL is 0.5%. If the rate of change of the frequency of EXTAL is slow (i.e., it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (i.e., it does not stay at an extreme value for a long time), then the allowed jitter can be 2%. The phase and frequency jitter performance results are only valid if the input jitter is less than the prescribed values.

SECTION 5

ORDERING INFORMATION

Consult a Motorola Semiconductor sales office or authorized distributor to determine product availability and to place an order.

Table 5-1 Ordering Information

Part	Supply Voltage	Package Type	Pin Count	Frequency (MHz)	Order Number
DSP56364	3.3 V	Thin quad flat pack (TQFP)	100	100	XCB56364FU100
		Quad flat pack (QFP)	112	100	XCB56364PV100

Notes:
1. The DSP56364 can include factory-programmed ROM. The listed 'B' ROM code is a generic unused ROM available to any customer. Variations will be supported for Dolby digital (AC-3), DTS, MPEG2, and other features. These products are only available to authorized licensees of those technologies. Please consult the web site at www.dspaudio.motorola.com for current availability.
2. Future products in the DSP56364 family may include other ROM-based options. For additional information on future part development, or to request customer-specific ROM-based support, call your local Motorola Semiconductor sales office or authorized distributor.

APPENDIX A

IBIS MODEL

```
[IBIS ver]       2.1
[File name]     56364.ibs
[File Rev]      0.0
[Date]        29/6/2000
[Component]    56364
[Manufacturer]  Motorola
[Package]
|variable       typ                   min                 max
R_pkg            45m                   22m                 75m
L_pkg            2.5nH                 1.1nH               4.3nH
C_pkg            1.3pF                 1.2pF               1.4pF


[Pin]signal_name model_name
  1 irqc_              ip5b_i
2 irqb_              ip5b_i
3 irqa_              ip5b_i
4 fst               ip5b_io
5 fsr               ip5b_io
6 sckt               ip5b_io
7 sckr               ip5b_io
8 svcc               power
9 sgnd               gnd
10 hsckt               ip5b_io
11 qvccl               power
12 qgnd               gnd
13 hsckr               ip5b_io
14 sdo0               ip5b_io
15 qvcch               power
16 sdo1               ip5b_io
17 sdo2               ip5b_io
18 sdo3               ip5b_io
19 sdo4               ip5b_io
20 sdo5               ip5b_io
21 svcc               power
22 sgnd               gnd
23 ss_               ip5b_io
24 mosi               ip5b_io
25 sda               ip5b_io
26 sck               ip5b_io
27 hreq_               ip5b_io
28 nmi_               ip5b_i
29 ires_               ip5b_i
31 pvcc               power
32 pcap               power
```

```
33 pgnd              gnd
34 cxtldis_              iexlh_i
35 qvcch              power
36 qgnd              gnd
37 qvccl              power
38 ta_              icbc_o
39 cas_              icbc_o
40 wr_              icbc_o
41 rd_              icbc_o
42 cvcc              power
43 cgnd              gnd
44 aa1              icbc_o
45 aa0              icbc_o
46 eab0              icba_o
47 eab1              icba_o
48 avcc              power
49 agnd              gnd
50 eab2              icba_o
51 eab3              icba_o
52 eab4              icba_o
53 eab5              icba_o
54 eab6              icba_o
55 avcc              power
56 agnd              gnd
57 eab7              icba_o
58 eab8              icba_o
59 eab9              icba_o
60 eab10              icba_o
61 qvcch              power
62 eab11              icba_o
63 avcc              power
64 agnd              gnd
65 qgnd              gnd
66 qvccl              power
67 eab12              icba_o
68 eab13              icba_o
69 eab14              icba_o
70 eab15              icba_o
71 avcc              power
72 agnd              gnd
73 eab16              icba_o
74 eab17              icba_o
75 edb0              icba_io
76 edb1              icba_io
77 edb2              icba_io
78 edb3              icba_io
79 dvcc              power
80 dgnd              gnd
81 edb4              icba_io
82 edb5              icba_io
83 edb6              icba_io
84 edb7              icba_io
87 qvccl              power
```

```
88 qgnd               gnd
89 qvcch               power
91 edb8               ip5b_io
92 svcc               power
93 sgnd               gnd
94 edb9               ip5b_io
95 edb10               ip5b_io
96 edb11               ip5b_io
97 tdo               ip5b_o
98 tdi               ip5b_i
99 tck               ip5b_i
100 tms               ip5b_i
|
[Model]        ip5b_i
Model_type        Input
Polarity        Non-Inverting
Vinl= 0.8000v
Vinh= 2.000v
C_comp        5.00pF        5.00pF        5.00pF
|
|
[Voltage Range]      3.3v      3v      3.6v
[GND_clamp]
|voltage        I(typ)        I(min)        I(max)
|
-3.30e+00   -5.21e+02   -3.65e+02   -5.18e+02
-3.10e+00   -4.69e+02   -3.30e+02   -4.67e+02
-2.90e+00   -4.18e+02   -2.94e+02   -4.16e+02
-2.70e+00   -3.67e+02   -2.59e+02   -3.65e+02
-2.50e+00   -3.16e+02   -2.23e+02   -3.14e+02
-2.30e+00   -2.65e+02   -1.88e+02   -2.63e+02
-2.10e+00   -2.14e+02   -1.52e+02   -2.12e+02
-1.90e+00   -1.63e+02   -1.17e+02   -1.61e+02
-1.70e+00   -1.13e+02   -9.25e+01   -1.10e+02
-1.50e+00   -7.83e+01   -6.88e+01   -7.58e+01
-1.30e+00   -4.43e+01   -4.52e+01   -4.17e+01
-1.10e+00   -1.02e+01   -2.15e+01   -7.67e+00
-9.00e-01   -9.69e-03   -1.18e+00   -7.81e-03
-7.00e-01   -2.83e-04   -5.70e-03   -8.42e-04
-5.00e-01   -1.35e-06   -4.53e-05   -1.00e-05
-3.00e-01   -1.31e-09   -3.74e-07   -8.58e-09
-1.00e-01   -2.92e-11   -3.00e-09   -3.64e-11
0.000e+00   -2.44e-11   -5.14e-10   -2.79e-11
|
[End]|
[Model]        ip5b_io
Model_type        I/O
Polarity        Non-Inverting
Vinl= 0.8000v
Vinh= 2.000v
C_comp        5.00pF        5.00pF        5.00pF
|
|
```

```
[Voltage Range]      3.3v      3v      3.6v
[Pulldown]
|voltage        I(typ)        I(min)        I(max)
|
-3.30e+00   -5.21e+02   -3.65e+02   -5.18e+02
-3.10e+00   -4.69e+02   -3.30e+02   -4.67e+02
-2.90e+00   -4.18e+02   -2.94e+02   -4.16e+02
-2.70e+00   -3.67e+02   -2.59e+02   -3.65e+02
-2.50e+00   -3.16e+02   -2.23e+02   -3.14e+02
-2.30e+00   -2.65e+02   -1.88e+02   -2.63e+02
-2.10e+00   -2.14e+02   -1.52e+02   -2.12e+02
-1.90e+00   -1.63e+02   -1.17e+02   -1.61e+02
-1.70e+00   -1.13e+02   -9.25e+01   -1.10e+02
-1.50e+00   -7.83e+01   -6.88e+01   -7.58e+01
-1.30e+00   -4.43e+01   -4.52e+01   -4.17e+01
-1.10e+00   -1.02e+01   -2.15e+01   -7.69e+00
-9.00e-01   -5.10e-02   -1.18e+00   -5.63e-02
-7.00e-01   -3.65e-02   -2.25e-02   -4.28e-02
-5.00e-01   -2.65e-02   -1.38e-02   -3.12e-02
-3.00e-01   -1.62e-02   -8.35e-03   -1.91e-02
-1.00e-01   -5.49e-03   -2.80e-03   -6.52e-03
1.000e-01   5.377e-03   2.744e-03   6.427e-03
3.000e-01   1.516e-02   7.871e-03   1.823e-02
5.000e-01   2.370e-02   1.252e-02   2.869e-02
7.000e-01   3.098e-02   1.667e-02   3.776e-02
9.000e-01   3.700e-02   2.026e-02   4.544e-02
1.100e+00   4.175e-02   2.324e-02   5.171e-02
1.300e+00   4.531e-02   2.553e-02   5.660e-02
1.500e+00   4.779e-02   2.709e-02   6.023e-02
1.700e+00   4.935e-02   2.803e-02   6.271e-02
1.900e+00   5.013e-02   2.851e-02   6.419e-02
2.100e+00   5.046e-02   2.876e-02   6.494e-02
2.300e+00   5.063e-02   2.892e-02   6.525e-02
2.500e+00   5.075e-02   2.904e-02   6.540e-02
2.700e+00   5.085e-02   2.912e-02   6.549e-02
2.900e+00   5.090e-02   2.876e-02   6.555e-02
3.100e+00   4.771e-02   2.994e-02   6.561e-02
3.300e+00   4.525e-02   3.321e-02   6.182e-02
3.500e+00   4.657e-02   3.570e-02   6.049e-02
3.700e+00   4.904e-02   3.801e-02   6.178e-02
3.900e+00   5.221e-02   4.029e-02   6.450e-02
4.100e+00   5.524e-02   4.253e-02   6.659e-02
4.300e+00   5.634e-02   4.463e-02   6.867e-02
4.500e+00   5.751e-02   4.645e-02   6.970e-02
4.700e+00   5.634e-02   4.786e-02   6.938e-02
4.900e+00   5.648e-02   4.881e-02   6.960e-02
5.100e+00   5.664e-02   4.912e-02   6.983e-02
5.300e+00   5.679e-02   4.795e-02   7.005e-02
5.500e+00   5.693e-02   4.679e-02   7.026e-02
5.700e+00   5.707e-02   4.688e-02   7.049e-02
5.900e+00   5.722e-02   4.700e-02   7.074e-02
6.100e+00   5.741e-02   4.712e-02   7.105e-02
6.300e+00   5.766e-02   4.723e-02   7.147e-02
```

```
6.500e+00   5.801e-02   4.733e-02   7.205e-02
6.600e+00   5.824e-02   4.737e-02   7.242e-02
|
[Pullup]
|voltage        I(typ)        I(min)        I(max)
|
-3.30e+00   2.922e-04   2.177e-04   4.123e-04
-3.10e+00   2.881e-04   2.175e-04   4.021e-04
-2.90e+00   2.853e-04   2.173e-04   3.946e-04
-2.70e+00   2.836e-04   2.172e-04   3.893e-04
-2.50e+00   2.825e-04   2.171e-04   3.857e-04
-2.30e+00   2.819e-04   2.170e-04   3.834e-04
-2.10e+00   2.815e-04   2.169e-04   3.820e-04
-1.90e+00   2.813e-04   2.167e-04   3.812e-04
-1.70e+00   2.812e-04   2.520e-04   3.808e-04
-1.50e+00   2.811e-04   3.078e-02   3.806e-04
-1.30e+00   2.810e-04   2.684e-02   3.804e-04
-1.10e+00   2.809e-04   2.277e-02   3.802e-04
-9.00e-01   2.808e-04   1.864e-02   3.801e-04
-7.00e-01   2.997e-04   1.447e-02   3.799e-04
-5.00e-01   1.750e-02   1.031e-02   3.797e-04
-3.00e-01   1.048e-02   6.181e-03   3.776e-04
-1.00e-01   3.487e-03   2.084e-03   4.568e-03
1.000e-01   -3.40e-03   -2.03e-03   -4.22e-03
3.000e-01   -9.69e-03   -5.71e-03   -1.24e-02
5.000e-01   -1.52e-02   -8.99e-03   -1.95e-02
7.000e-01   -2.02e-02   -1.19e-02   -2.61e-02
9.000e-01   -2.46e-02   -1.43e-02   -3.21e-02
1.100e+00   -2.84e-02   -1.62e-02   -3.73e-02
1.300e+00   -3.14e-02   -1.77e-02   -4.18e-02
1.500e+00   -3.37e-02   -1.88e-02   -4.55e-02
1.700e+00   -3.55e-02   -1.95e-02   -4.85e-02
1.900e+00   -3.68e-02   -2.00e-02   -5.09e-02
2.100e+00   -3.78e-02   -2.04e-02   -5.27e-02
2.300e+00   -3.85e-02   -2.07e-02   -5.41e-02
2.500e+00   -3.91e-02   -2.10e-02   -5.51e-02
2.700e+00   -3.96e-02   -2.12e-02   -5.60e-02
2.900e+00   -4.01e-02   -2.15e-02   -5.67e-02
3.100e+00   -4.04e-02   -2.17e-02   -5.74e-02
3.300e+00   -4.08e-02   -2.18e-02   -5.79e-02
3.500e+00   -4.11e-02   -2.20e-02   -5.84e-02
3.700e+00   -4.14e-02   -2.78e-02   -5.89e-02
3.900e+00   -4.17e-02   -1.20e+00   -5.94e-02
4.100e+00   -4.32e-02   -2.15e+01   -5.98e-02
4.300e+00   -4.08e-01   -4.52e+01   -6.10e-02
4.500e+00   -2.73e+01   -6.89e+01   -6.84e-02
4.700e+00   -6.13e+01   -9.25e+01   -7.73e+00
4.900e+00   -9.54e+01   -1.17e+02   -4.18e+01
5.100e+00   -1.38e+02   -1.52e+02   -7.59e+01
5.300e+00   -1.89e+02   -1.88e+02   -1.11e+02
5.500e+00   -2.40e+02   -2.23e+02   -1.61e+02
5.700e+00   -2.91e+02   -2.59e+02   -2.12e+02
5.900e+00   -3.42e+02   -2.94e+02   -2.63e+02
```

```
6.100e+00   -3.93e+02   -3.30e+02   -3.14e+02
6.300e+00   -4.44e+02   -3.65e+02   -3.65e+02
6.500e+00   -4.95e+02   -4.01e+02   -4.16e+02
6.600e+00   -5.21e+02   -4.18e+02   -4.41e+02
|
[GND_clamp]
|voltage        I(typ)        I(min)        I(max)
|
-3.30e+00   -5.21e+02   -3.65e+02   -5.18e+02
-3.10e+00   -4.69e+02   -3.30e+02   -4.67e+02
-2.90e+00   -4.18e+02   -2.94e+02   -4.16e+02
-2.70e+00   -3.67e+02   -2.59e+02   -3.65e+02
-2.50e+00   -3.16e+02   -2.23e+02   -3.14e+02
-2.30e+00   -2.65e+02   -1.88e+02   -2.63e+02
-2.10e+00   -2.14e+02   -1.52e+02   -2.12e+02
-1.90e+00   -1.63e+02   -1.17e+02   -1.61e+02
-1.70e+00   -1.13e+02   -9.25e+01   -1.10e+02
-1.50e+00   -7.83e+01   -6.88e+01   -7.58e+01
-1.30e+00   -4.43e+01   -4.52e+01   -4.17e+01
-1.10e+00   -1.02e+01   -2.15e+01   -7.67e+00
-9.00e-01   -9.69e-03   -1.18e+00   -7.81e-03
-7.00e-01   -2.83e-04   -5.70e-03   -8.42e-04
-5.00e-01   -1.35e-06   -4.53e-05   -1.00e-05
-3.00e-01   -1.31e-09   -3.74e-07   -8.58e-09
-1.00e-01   -2.92e-11   -3.00e-09   -3.64e-11
0.000e+00   -2.44e-11   -5.14e-10   -2.79e-11
|
[Ramp]
R_load = 50.00
|voltage        I(typ)        I(min)        I(max)
|
|
dV/dt_r        1.030/0.465    0.605/0.676    1.320/0.366
|
|
dV/dt_f        1.290/0.671    0.829/0.122    1.520/0.431
|
[End]|
[Model]        ip5b_o
Model_type        3-state
Polarity        Non-Inverting
C_comp        5.00pF        5.00pF        5.00pF
|
|
[Voltage Range]      3.3v      3v      3.6v
[Pulldown]
|voltage        I(typ)        I(min)        I(max)
|
-3.30e+00   -5.21e+02   -3.65e+02   -5.18e+02
-3.10e+00   -4.69e+02   -3.30e+02   -4.67e+02
-2.90e+00   -4.18e+02   -2.94e+02   -4.16e+02
-2.70e+00   -3.67e+02   -2.59e+02   -3.65e+02
-2.50e+00   -3.16e+02   -2.23e+02   -3.14e+02
```

```
-2.30e+00   -2.65e+02   -1.88e+02   -2.63e+02
-2.10e+00   -2.14e+02   -1.52e+02   -2.12e+02
-1.90e+00   -1.63e+02   -1.17e+02   -1.61e+02
-1.70e+00   -1.13e+02   -9.25e+01   -1.10e+02
-1.50e+00   -7.83e+01   -6.88e+01   -7.58e+01
-1.30e+00   -4.43e+01   -4.52e+01   -4.17e+01
-1.10e+00   -1.02e+01   -2.15e+01   -7.69e+00
-9.00e-01   -5.10e-02   -1.18e+00   -5.63e-02
-7.00e-01   -3.65e-02   -2.25e-02   -4.28e-02
-5.00e-01   -2.65e-02   -1.38e-02   -3.12e-02
-3.00e-01   -1.62e-02   -8.35e-03   -1.91e-02
-1.00e-01   -5.49e-03   -2.80e-03   -6.52e-03
1.000e-01   5.377e-03   2.744e-03   6.427e-03
3.000e-01   1.516e-02   7.871e-03   1.823e-02
5.000e-01   2.370e-02   1.252e-02   2.869e-02
7.000e-01   3.098e-02   1.667e-02   3.776e-02
9.000e-01   3.700e-02   2.026e-02   4.544e-02
1.100e+00   4.175e-02   2.324e-02   5.171e-02
1.300e+00   4.531e-02   2.553e-02   5.660e-02
1.500e+00   4.779e-02   2.709e-02   6.023e-02
1.700e+00   4.935e-02   2.803e-02   6.271e-02
1.900e+00   5.013e-02   2.851e-02   6.419e-02
2.100e+00   5.046e-02   2.876e-02   6.494e-02
2.300e+00   5.063e-02   2.892e-02   6.525e-02
2.500e+00   5.075e-02   2.904e-02   6.540e-02
2.700e+00   5.085e-02   2.912e-02   6.549e-02
2.900e+00   5.090e-02   2.876e-02   6.555e-02
3.100e+00   4.771e-02   2.994e-02   6.561e-02
3.300e+00   4.525e-02   3.321e-02   6.182e-02
3.500e+00   4.657e-02   3.570e-02   6.049e-02
3.700e+00   4.904e-02   3.801e-02   6.178e-02
3.900e+00   5.221e-02   4.029e-02   6.450e-02
4.100e+00   5.524e-02   4.253e-02   6.659e-02
4.300e+00   5.634e-02   4.463e-02   6.867e-02
4.500e+00   5.751e-02   4.645e-02   6.970e-02
4.700e+00   5.634e-02   4.786e-02   6.938e-02
4.900e+00   5.648e-02   4.881e-02   6.960e-02
5.100e+00   5.664e-02   4.912e-02   6.983e-02
5.300e+00   5.679e-02   4.795e-02   7.005e-02
5.500e+00   5.693e-02   4.679e-02   7.026e-02
5.700e+00   5.707e-02   4.688e-02   7.049e-02
5.900e+00   5.722e-02   4.700e-02   7.074e-02
6.100e+00   5.741e-02   4.712e-02   7.105e-02
6.300e+00   5.766e-02   4.723e-02   7.147e-02
6.500e+00   5.801e-02   4.733e-02   7.205e-02
6.600e+00   5.824e-02   4.737e-02   7.242e-02
|
[Pullup]
|voltage        I(typ)        I(min)        I(max)
|
-3.30e+00   2.922e-04   2.177e-04   4.123e-04
-3.10e+00   2.881e-04   2.175e-04   4.021e-04
-2.90e+00   2.853e-04   2.173e-04   3.946e-04
```

```
-2.70e+00   2.836e-04   2.172e-04   3.893e-04
-2.50e+00   2.825e-04   2.171e-04   3.857e-04
-2.30e+00   2.819e-04   2.170e-04   3.834e-04
-2.10e+00   2.815e-04   2.169e-04   3.820e-04
-1.90e+00   2.813e-04   2.167e-04   3.812e-04
-1.70e+00   2.812e-04   2.520e-04   3.808e-04
-1.50e+00   2.811e-04   3.078e-02   3.806e-04
-1.30e+00   2.810e-04   2.684e-02   3.804e-04
-1.10e+00   2.809e-04   2.277e-02   3.802e-04
-9.00e-01   2.808e-04   1.864e-02   3.801e-04
-7.00e-01   2.997e-04   1.447e-02   3.799e-04
-5.00e-01   1.750e-02   1.031e-02   3.797e-04
-3.00e-01   1.048e-02   6.181e-03   3.776e-04
-1.00e-01   3.487e-03   2.084e-03   4.568e-03
1.000e-01   -3.40e-03   -2.03e-03   -4.22e-03
3.000e-01   -9.69e-03   -5.71e-03   -1.24e-02
5.000e-01   -1.52e-02   -8.99e-03   -1.95e-02
7.000e-01   -2.02e-02   -1.19e-02   -2.61e-02
9.000e-01   -2.46e-02   -1.43e-02   -3.21e-02
1.100e+00   -2.84e-02   -1.62e-02   -3.73e-02
1.300e+00   -3.14e-02   -1.77e-02   -4.18e-02
1.500e+00   -3.37e-02   -1.88e-02   -4.55e-02
1.700e+00   -3.55e-02   -1.95e-02   -4.85e-02
1.900e+00   -3.68e-02   -2.00e-02   -5.09e-02
2.100e+00   -3.78e-02   -2.04e-02   -5.27e-02
2.300e+00   -3.85e-02   -2.07e-02   -5.41e-02
2.500e+00   -3.91e-02   -2.10e-02   -5.51e-02
2.700e+00   -3.96e-02   -2.12e-02   -5.60e-02
2.900e+00   -4.01e-02   -2.15e-02   -5.67e-02
3.100e+00   -4.04e-02   -2.17e-02   -5.74e-02
3.300e+00   -4.08e-02   -2.18e-02   -5.79e-02
3.500e+00   -4.11e-02   -2.20e-02   -5.84e-02
3.700e+00   -4.14e-02   -2.78e-02   -5.89e-02
3.900e+00   -4.17e-02   -1.20e+00   -5.94e-02
4.100e+00   -4.32e-02   -2.15e+01   -5.98e-02
4.300e+00   -4.08e-01   -4.52e+01   -6.10e-02
4.500e+00   -2.73e+01   -6.89e+01   -6.84e-02
4.700e+00   -6.13e+01   -9.25e+01   -7.73e+00
4.900e+00   -9.54e+01   -1.17e+02   -4.18e+01
5.100e+00   -1.38e+02   -1.52e+02   -7.59e+01
5.300e+00   -1.89e+02   -1.88e+02   -1.11e+02
5.500e+00   -2.40e+02   -2.23e+02   -1.61e+02
5.700e+00   -2.91e+02   -2.59e+02   -2.12e+02
5.900e+00   -3.42e+02   -2.94e+02   -2.63e+02
6.100e+00   -3.93e+02   -3.30e+02   -3.14e+02
6.300e+00   -4.44e+02   -3.65e+02   -3.65e+02
6.500e+00   -4.95e+02   -4.01e+02   -4.16e+02
6.600e+00   -5.21e+02   -4.18e+02   -4.41e+02
|
[GND_clamp]
|voltage        I(typ)        I(min)        I(max)
|
-3.30e+00   -5.21e+02   -3.65e+02   -5.18e+02
```

```
-3.10e+00   -4.69e+02   -3.30e+02   -4.67e+02
-2.90e+00   -4.18e+02   -2.94e+02   -4.16e+02
-2.70e+00   -3.67e+02   -2.59e+02   -3.65e+02
-2.50e+00   -3.16e+02   -2.23e+02   -3.14e+02
-2.30e+00   -2.65e+02   -1.88e+02   -2.63e+02
-2.10e+00   -2.14e+02   -1.52e+02   -2.12e+02
-1.90e+00   -1.63e+02   -1.17e+02   -1.61e+02
-1.70e+00   -1.13e+02   -9.25e+01   -1.10e+02
-1.50e+00   -7.83e+01   -6.88e+01   -7.58e+01
-1.30e+00   -4.43e+01   -4.52e+01   -4.17e+01
-1.10e+00   -1.02e+01   -2.15e+01   -7.67e+00
-9.00e-01   -9.69e-03   -1.18e+00   -7.81e-03
-7.00e-01   -2.83e-04   -5.70e-03   -8.42e-04
-5.00e-01   -1.35e-06   -4.53e-05   -1.00e-05
-3.00e-01   -1.31e-09   -3.74e-07   -8.58e-09
-1.00e-01   -2.92e-11   -3.00e-09   -3.64e-11
0.000e+00   -2.44e-11   -5.14e-10   -2.79e-11
|
[Ramp]
R_load = 50.00
|voltage        I(typ)        I(min)        I(max)
|
|
dV/dt_r        1.030/0.465    0.605/0.676    1.320/0.366
|
|
dV/dt_f        1.290/0.671    0.829/0.122    1.520/0.431
|
[End]|
[Model]        icba_io
Model_type        I/O
Polarity        Non-Inverting
Vinl= 0.8000v
Vinh= 2.000v
C_comp        5.00pF        5.00pF        5.00pF
|
|
[Voltage Range]      3.3v      3v      3.6v
[Pulldown]
|voltage        I(typ)        I(min)        I(max)
|
-3.30e+00   -5.20e+02   -3.65e+02   -5.18e+02
-3.10e+00   -4.69e+02   -3.30e+02   -4.67e+02
-2.90e+00   -4.18e+02   -2.94e+02   -4.16e+02
-2.70e+00   -3.67e+02   -2.59e+02   -3.65e+02
-2.50e+00   -3.16e+02   -2.23e+02   -3.14e+02
-2.30e+00   -2.65e+02   -1.88e+02   -2.63e+02
-2.10e+00   -2.14e+02   -1.52e+02   -2.12e+02
-1.90e+00   -1.63e+02   -1.17e+02   -1.60e+02
-1.70e+00   -1.13e+02   -9.25e+01   -1.10e+02
-1.50e+00   -7.83e+01   -6.88e+01   -7.58e+01
-1.30e+00   -4.43e+01   -4.52e+01   -4.17e+01
-1.10e+00   -1.02e+01   -2.15e+01   -7.68e+00
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-9.00e-01   -2.70e-02   -1.19e+00   -2.90e-02
-7.00e-01   -1.32e-02   -1.25e-02   -1.63e-02
-5.00e-01   -9.33e-03   -4.69e-03   -1.10e-02
-3.00e-01   -5.75e-03   -2.81e-03   -6.76e-03
-1.00e-01   -1.97e-03   -9.48e-04   -2.32e-03
1.000e-01   1.945e-03   9.285e-04   2.307e-03
3.000e-01   5.507e-03   2.640e-03   6.599e-03
5.000e-01   8.649e-03   4.168e-03   1.048e-02
7.000e-01   1.136e-02   5.504e-03   1.393e-02
9.000e-01   1.364e-02   6.636e-03   1.693e-02
1.100e+00   1.547e-02   7.551e-03   1.950e-02
1.300e+00   1.688e-02   8.240e-03   2.162e-02
1.500e+00   1.299e-01   6.458e-02   2.331e-02
1.700e+00   1.366e-01   6.746e-02   1.755e-01
1.900e+00   1.404e-01   6.916e-02   1.847e-01
2.100e+00   1.423e-01   7.006e-02   1.907e-01
2.300e+00   1.433e-01   7.059e-02   1.940e-01
2.500e+00   1.440e-01   7.098e-02   1.958e-01
2.700e+00   1.445e-01   7.128e-02   1.970e-01
2.900e+00   1.450e-01   7.154e-02   1.979e-01
3.100e+00   1.454e-01   7.176e-02   1.986e-01
3.300e+00   1.458e-01   7.196e-02   1.993e-01
3.500e+00   1.461e-01   7.223e-02   1.999e-01
3.700e+00   1.464e-01   8.810e-02   2.004e-01
3.900e+00   1.469e-01   2.589e+00   2.009e-01
4.100e+00   1.490e-01   1.451e+01   2.015e-01
4.300e+00   1.501e+00   2.658e+01   2.030e-01
4.500e+00   1.813e+01   3.866e+01   2.385e-01
4.700e+00   3.540e+01   5.076e+01   9.563e+00
4.900e+00   5.269e+01   6.461e+01   2.682e+01
5.100e+00   7.541e+01   8.261e+01   4.409e+01
5.300e+00   1.012e+02   1.006e+02   6.258e+01
5.500e+00   1.270e+02   1.186e+02   8.836e+01
5.700e+00   1.527e+02   1.366e+02   1.141e+02
5.900e+00   1.785e+02   1.546e+02   1.399e+02
6.100e+00   2.043e+02   1.726e+02   1.657e+02
6.300e+00   2.301e+02   1.906e+02   1.915e+02
6.500e+00   2.559e+02   2.086e+02   2.173e+02
6.600e+00   2.688e+02   2.176e+02   2.302e+02
|
[Pullup]
|voltage        I(typ)        I(min)        I(max)
|
-3.30e+00   2.686e+02   1.905e+02   2.686e+02
-3.10e+00   2.428e+02   1.725e+02   2.428e+02
-2.90e+00   2.170e+02   1.545e+02   2.170e+02
-2.70e+00   1.912e+02   1.365e+02   1.912e+02
-2.50e+00   1.655e+02   1.185e+02   1.655e+02
-2.30e+00   1.397e+02   1.005e+02   1.397e+02
-2.10e+00   1.139e+02   8.253e+01   1.139e+02
-1.90e+00   8.814e+01   6.454e+01   8.814e+01
-1.70e+00   6.237e+01   5.068e+01   6.237e+01
-1.50e+00   4.389e+01   3.859e+01   4.389e+01
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-1.30e+00   2.662e+01   2.651e+01   2.662e+01
-1.10e+00   9.360e+00   1.444e+01   9.362e+00
-9.00e-01   4.275e-02   2.518e+00   4.663e-02
-7.00e-01   8.208e-03   2.012e-02   1.070e-02
-5.00e-01   5.635e-03   3.518e-03   7.068e-03
-3.00e-01   3.370e-03   2.053e-03   4.233e-03
-1.00e-01   1.118e-03   6.789e-04   1.410e-03
1.000e-01   -1.09e-03   -6.56e-04   -1.38e-03
3.000e-01   -3.12e-03   -1.86e-03   -3.99e-03
5.000e-01   -4.96e-03   -2.93e-03   -6.39e-03
7.000e-01   -6.60e-03   -3.87e-03   -8.59e-03
9.000e-01   -8.04e-03   -4.66e-03   -1.06e-02
1.100e+00   -9.26e-03   -5.30e-03   -1.23e-02
1.300e+00   -1.03e-02   -6.55e-02   -1.38e-02
1.500e+00   -1.25e-01   -6.93e-02   -1.70e-01
1.700e+00   -1.31e-01   -7.19e-02   -1.82e-01
1.900e+00   -1.36e-01   -7.38e-02   -1.91e-01
2.100e+00   -1.40e-01   -7.53e-02   -1.97e-01
2.300e+00   -1.42e-01   -7.65e-02   -2.03e-01
2.500e+00   -1.44e-01   -7.76e-02   -2.07e-01
2.700e+00   -1.46e-01   -7.85e-02   -2.10e-01
2.900e+00   -1.48e-01   -7.93e-02   -2.13e-01
3.100e+00   -1.49e-01   -8.00e-02   -2.15e-01
3.300e+00   -1.50e-01   -8.06e-02   -2.17e-01
3.500e+00   -1.52e-01   -8.13e-02   -2.19e-01
3.700e+00   -1.53e-01   -8.84e-02   -2.21e-01
3.900e+00   -1.54e-01   -1.26e+00   -2.22e-01
4.100e+00   -1.57e-01   -2.16e+01   -2.24e-01
4.300e+00   -5.25e-01   -4.53e+01   -2.27e-01
4.500e+00   -2.74e+01   -6.89e+01   -2.38e-01
4.700e+00   -6.14e+01   -9.26e+01   -7.90e+00
4.900e+00   -9.55e+01   -1.17e+02   -4.20e+01
5.100e+00   -1.38e+02   -1.52e+02   -7.60e+01
5.300e+00   -1.89e+02   -1.88e+02   -1.11e+02
5.500e+00   -2.40e+02   -2.23e+02   -1.61e+02
5.700e+00   -2.91e+02   -2.59e+02   -2.12e+02
5.900e+00   -3.42e+02   -2.94e+02   -2.63e+02
6.100e+00   -3.93e+02   -3.30e+02   -3.14e+02
6.300e+00   -4.44e+02   -3.65e+02   -3.65e+02
6.500e+00   -4.95e+02   -4.01e+02   -4.16e+02
6.600e+00   -5.21e+02   -4.19e+02   -4.42e+02
|
[GND_clamp]
|voltage        I(typ)        I(min)        I(max)
|
-3.30e+00   -5.20e+02   -3.65e+02   -5.18e+02
-3.10e+00   -4.69e+02   -3.30e+02   -4.67e+02
-2.90e+00   -4.18e+02   -2.94e+02   -4.16e+02
-2.70e+00   -3.67e+02   -2.59e+02   -3.65e+02
-2.50e+00   -3.16e+02   -2.23e+02   -3.14e+02
-2.30e+00   -2.65e+02   -1.88e+02   -2.63e+02
-2.10e+00   -2.14e+02   -1.52e+02   -2.12e+02
-1.90e+00   -1.63e+02   -1.17e+02   -1.60e+02
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-1.70e+00   -1.13e+02   -9.25e+01   -1.10e+02
-1.50e+00   -7.83e+01   -6.88e+01   -7.58e+01
-1.30e+00   -4.43e+01   -4.52e+01   -4.17e+01
-1.10e+00   -1.02e+01   -2.15e+01   -7.67e+00
-9.00e-01   -1.22e-02   -1.18e+00   -1.17e-02
-7.00e-01   -5.18e-04   -6.62e-03   -1.56e-03
-5.00e-01   -2.43e-06   -6.64e-05   -1.80e-05
-3.00e-01   -2.33e-09   -6.35e-07   -1.54e-08
-1.00e-01   -2.10e-11   -6.31e-09   -2.99e-11
0.000e+00   -1.70e-11   -1.95e-09   -1.91e-11
|
[POWER_clamp]
|voltage        I(typ)        I(min)        I(max)
|
-3.30e+00   2.686e+02   1.905e+02   2.686e+02
-3.10e+00   2.428e+02   1.725e+02   2.428e+02
-2.90e+00   2.170e+02   1.545e+02   2.170e+02
-2.70e+00   1.912e+02   1.365e+02   1.912e+02
-2.50e+00   1.655e+02   1.185e+02   1.655e+02
-2.30e+00   1.397e+02   1.005e+02   1.397e+02
-2.10e+00   1.139e+02   8.253e+01   1.139e+02
-1.90e+00   8.814e+01   6.454e+01   8.814e+01
-1.70e+00   6.236e+01   5.068e+01   6.237e+01
-1.50e+00   4.389e+01   3.859e+01   4.389e+01
-1.30e+00   2.662e+01   2.651e+01   2.662e+01
-1.10e+00   9.358e+00   1.444e+01   9.359e+00
-9.00e-01   3.399e-02   2.517e+00   3.554e-02
-7.00e-01   3.426e-04   1.577e-02   9.211e-04
-5.00e-01   2.840e-06   7.857e-05   1.655e-05
-3.00e-01   3.401e-09   6.836e-07   1.946e-08
-1.00e-01   6.162e-11   7.379e-09   7.622e-11
0.000e+00   5.758e-11   2.438e-09   6.240e-11
|
[Ramp]
R_load = 50.00
|voltage        I(typ)        I(min)        I(max)
|
|
dV/dt_r        1.680/0.164    1.360/0.329    1.900/0.124
|
|
dV/dt_f        1.690/0.219    1.310/0.442    1.880/0.155
|
[End]|
[Model]        icba_o
Model_type        3-state
Polarity        Non-Inverting
C_comp        5.00pF        5.00pF        5.00pF
|
|
[Voltage Range]      3.3v      3v      3.6v
[Pulldown]
|voltage        I(typ)        I(min)        I(max)
```

```
|
-3.30e+00   -5.20e+02   -3.65e+02   -5.18e+02
-3.10e+00   -4.69e+02   -3.30e+02   -4.67e+02
-2.90e+00   -4.18e+02   -2.94e+02   -4.16e+02
-2.70e+00   -3.67e+02   -2.59e+02   -3.65e+02
-2.50e+00   -3.16e+02   -2.23e+02   -3.14e+02
-2.30e+00   -2.65e+02   -1.88e+02   -2.63e+02
-2.10e+00   -2.14e+02   -1.52e+02   -2.12e+02
-1.90e+00   -1.63e+02   -1.17e+02   -1.60e+02
-1.70e+00   -1.13e+02   -9.25e+01   -1.10e+02
-1.50e+00   -7.83e+01   -6.88e+01   -7.58e+01
-1.30e+00   -4.43e+01   -4.52e+01   -4.17e+01
-1.10e+00   -1.02e+01   -2.15e+01   -7.68e+00
-9.00e-01   -2.70e-02   -1.19e+00   -2.90e-02
-7.00e-01   -1.32e-02   -1.25e-02   -1.63e-02
-5.00e-01   -9.33e-03   -4.69e-03   -1.10e-02
-3.00e-01   -5.75e-03   -2.81e-03   -6.76e-03
-1.00e-01   -1.97e-03   -9.48e-04   -2.32e-03
1.000e-01   1.945e-03   9.285e-04   2.307e-03
3.000e-01   5.507e-03   2.640e-03   6.599e-03
5.000e-01   8.649e-03   4.168e-03   1.048e-02
7.000e-01   1.136e-02   5.504e-03   1.393e-02
9.000e-01   1.364e-02   6.636e-03   1.693e-02
1.100e+00   1.547e-02   7.551e-03   1.950e-02
1.300e+00   1.688e-02   8.240e-03   2.162e-02
1.500e+00   1.299e-01   6.458e-02   2.331e-02
1.700e+00   1.366e-01   6.746e-02   1.755e-01
1.900e+00   1.404e-01   6.916e-02   1.847e-01
2.100e+00   1.423e-01   7.006e-02   1.907e-01
2.300e+00   1.433e-01   7.059e-02   1.940e-01
2.500e+00   1.440e-01   7.098e-02   1.958e-01
2.700e+00   1.445e-01   7.128e-02   1.970e-01
2.900e+00   1.450e-01   7.154e-02   1.979e-01
3.100e+00   1.454e-01   7.176e-02   1.986e-01
3.300e+00   1.458e-01   7.196e-02   1.993e-01
3.500e+00   1.461e-01   7.223e-02   1.999e-01
3.700e+00   1.464e-01   8.810e-02   2.004e-01
3.900e+00   1.469e-01   2.589e+00   2.009e-01
4.100e+00   1.490e-01   1.451e+01   2.015e-01
4.300e+00   1.501e+00   2.658e+01   2.030e-01
4.500e+00   1.813e+01   3.866e+01   2.385e-01
4.700e+00   3.540e+01   5.076e+01   9.563e+00
4.900e+00   5.269e+01   6.461e+01   2.682e+01
5.100e+00   7.541e+01   8.261e+01   4.409e+01
5.300e+00   1.012e+02   1.006e+02   6.258e+01
5.500e+00   1.270e+02   1.186e+02   8.836e+01
5.700e+00   1.527e+02   1.366e+02   1.141e+02
5.900e+00   1.785e+02   1.546e+02   1.399e+02
6.100e+00   2.043e+02   1.726e+02   1.657e+02
6.300e+00   2.301e+02   1.906e+02   1.915e+02
6.500e+00   2.559e+02   2.086e+02   2.173e+02
6.600e+00   2.688e+02   2.176e+02   2.302e+02
|
```

```
[Pullup]
|voltage        I(typ)        I(min)        I(max)
|
-3.30e+00   2.686e+02   1.905e+02   2.686e+02
-3.10e+00   2.428e+02   1.725e+02   2.428e+02
-2.90e+00   2.170e+02   1.545e+02   2.170e+02
-2.70e+00   1.912e+02   1.365e+02   1.912e+02
-2.50e+00   1.655e+02   1.185e+02   1.655e+02
-2.30e+00   1.397e+02   1.005e+02   1.397e+02
-2.10e+00   1.139e+02   8.253e+01   1.139e+02
-1.90e+00   8.814e+01   6.454e+01   8.814e+01
-1.70e+00   6.237e+01   5.068e+01   6.237e+01
-1.50e+00   4.389e+01   3.859e+01   4.389e+01
-1.30e+00   2.662e+01   2.651e+01   2.662e+01
-1.10e+00   9.360e+00   1.444e+01   9.362e+00
-9.00e-01   4.275e-02   2.518e+00   4.663e-02
-7.00e-01   8.208e-03   2.012e-02   1.070e-02
-5.00e-01   5.635e-03   3.518e-03   7.068e-03
-3.00e-01   3.370e-03   2.053e-03   4.233e-03
-1.00e-01   1.118e-03   6.789e-04   1.410e-03
1.000e-01   -1.09e-03   -6.56e-04   -1.38e-03
3.000e-01   -3.12e-03   -1.86e-03   -3.99e-03
5.000e-01   -4.96e-03   -2.93e-03   -6.39e-03
7.000e-01   -6.60e-03   -3.87e-03   -8.59e-03
9.000e-01   -8.04e-03   -4.66e-03   -1.06e-02
1.100e+00   -9.26e-03   -5.30e-03   -1.23e-02
1.300e+00   -1.03e-02   -6.55e-02   -1.38e-02
1.500e+00   -1.25e-01   -6.93e-02   -1.70e-01
1.700e+00   -1.31e-01   -7.19e-02   -1.82e-01
1.900e+00   -1.36e-01   -7.38e-02   -1.91e-01
2.100e+00   -1.40e-01   -7.53e-02   -1.97e-01
2.300e+00   -1.42e-01   -7.65e-02   -2.03e-01
2.500e+00   -1.44e-01   -7.76e-02   -2.07e-01
2.700e+00   -1.46e-01   -7.85e-02   -2.10e-01
2.900e+00   -1.48e-01   -7.93e-02   -2.13e-01
3.100e+00   -1.49e-01   -8.00e-02   -2.15e-01
3.300e+00   -1.50e-01   -8.06e-02   -2.17e-01
3.500e+00   -1.52e-01   -8.13e-02   -2.19e-01
3.700e+00   -1.53e-01   -8.84e-02   -2.21e-01
3.900e+00   -1.54e-01   -1.26e+00   -2.22e-01
4.100e+00   -1.57e-01   -2.16e+01   -2.24e-01
4.300e+00   -5.25e-01   -4.53e+01   -2.27e-01
4.500e+00   -2.74e+01   -6.89e+01   -2.38e-01
4.700e+00   -6.14e+01   -9.26e+01   -7.90e+00
4.900e+00   -9.55e+01   -1.17e+02   -4.20e+01
5.100e+00   -1.38e+02   -1.52e+02   -7.60e+01
5.300e+00   -1.89e+02   -1.88e+02   -1.11e+02
5.500e+00   -2.40e+02   -2.23e+02   -1.61e+02
5.700e+00   -2.91e+02   -2.59e+02   -2.12e+02
5.900e+00   -3.42e+02   -2.94e+02   -2.63e+02
6.100e+00   -3.93e+02   -3.30e+02   -3.14e+02
6.300e+00   -4.44e+02   -3.65e+02   -3.65e+02
6.500e+00   -4.95e+02   -4.01e+02   -4.16e+02
```

```
6.600e+00   -5.21e+02   -4.19e+02   -4.42e+02
|
[GND_clamp]
|voltage        I(typ)        I(min)        I(max)
|
-3.30e+00   -5.20e+02   -3.65e+02   -5.18e+02
-3.10e+00   -4.69e+02   -3.30e+02   -4.67e+02
-2.90e+00   -4.18e+02   -2.94e+02   -4.16e+02
-2.70e+00   -3.67e+02   -2.59e+02   -3.65e+02
-2.50e+00   -3.16e+02   -2.23e+02   -3.14e+02
-2.30e+00   -2.65e+02   -1.88e+02   -2.63e+02
-2.10e+00   -2.14e+02   -1.52e+02   -2.12e+02
-1.90e+00   -1.63e+02   -1.17e+02   -1.60e+02
-1.70e+00   -1.13e+02   -9.25e+01   -1.10e+02
-1.50e+00   -7.83e+01   -6.88e+01   -7.58e+01
-1.30e+00   -4.43e+01   -4.52e+01   -4.17e+01
-1.10e+00   -1.02e+01   -2.15e+01   -7.67e+00
-9.00e-01   -1.22e-02   -1.18e+00   -1.17e-02
-7.00e-01   -5.18e-04   -6.62e-03   -1.56e-03
-5.00e-01   -2.43e-06   -6.64e-05   -1.80e-05
-3.00e-01   -2.33e-09   -6.35e-07   -1.54e-08
-1.00e-01   -2.10e-11   -6.31e-09   -2.99e-11
0.000e+00   -1.70e-11   -1.95e-09   -1.91e-11
|
[POWER_clamp]
|voltage        I(typ)        I(min)        I(max)
|
-3.30e+00   2.686e+02   1.905e+02   2.686e+02
-3.10e+00   2.428e+02   1.725e+02   2.428e+02
-2.90e+00   2.170e+02   1.545e+02   2.170e+02
-2.70e+00   1.912e+02   1.365e+02   1.912e+02
-2.50e+00   1.655e+02   1.185e+02   1.655e+02
-2.30e+00   1.397e+02   1.005e+02   1.397e+02
-2.10e+00   1.139e+02   8.253e+01   1.139e+02
-1.90e+00   8.814e+01   6.454e+01   8.814e+01
-1.70e+00   6.236e+01   5.068e+01   6.237e+01
-1.50e+00   4.389e+01   3.859e+01   4.389e+01
-1.30e+00   2.662e+01   2.651e+01   2.662e+01
-1.10e+00   9.358e+00   1.444e+01   9.359e+00
-9.00e-01   3.399e-02   2.517e+00   3.554e-02
-7.00e-01   3.426e-04   1.577e-02   9.211e-04
-5.00e-01   2.840e-06   7.857e-05   1.655e-05
-3.00e-01   3.401e-09   6.836e-07   1.946e-08
-1.00e-01   6.162e-11   7.379e-09   7.622e-11
0.000e+00   5.758e-11   2.438e-09   6.240e-11
|
[Ramp]
R_load = 50.00
|voltage        I(typ)        I(min)        I(max)
|
|
dV/dt_r        1.680/0.164    1.360/0.329    1.900/0.124
|
```

```
|
dV/dt_f        1.690/0.219    1.310/0.442    1.880/0.155
|
[End]|
[Model]        icbc_o
Model_type        3-state
Polarity        Non-Inverting
C_comp        5.00pF        5.00pF        5.00pF
|
|
[Voltage Range]      3.3v      3v      3.6v
[Pulldown]
|voltage        I(typ)        I(min)        I(max)
|
-3.30e+00   -5.20e+02   -3.65e+02   -5.18e+02
-3.10e+00   -4.69e+02   -3.30e+02   -4.67e+02
-2.90e+00   -4.18e+02   -2.94e+02   -4.16e+02
-2.70e+00   -3.67e+02   -2.59e+02   -3.65e+02
-2.50e+00   -3.16e+02   -2.23e+02   -3.14e+02
-2.30e+00   -2.65e+02   -1.88e+02   -2.63e+02
-2.10e+00   -2.14e+02   -1.52e+02   -2.11e+02
-1.90e+00   -1.63e+02   -1.17e+02   -1.60e+02
-1.70e+00   -1.13e+02   -9.25e+01   -1.10e+02
-1.50e+00   -7.83e+01   -6.88e+01   -7.58e+01
-1.30e+00   -4.42e+01   -4.51e+01   -4.17e+01
-1.10e+00   -1.02e+01   -2.15e+01   -7.67e+00
-9.00e-01   -2.51e-02   -1.18e+00   -2.65e-02
-7.00e-01   -1.30e-02   -1.16e-02   -1.58e-02
-5.00e-01   -9.33e-03   -4.67e-03   -1.10e-02
-3.00e-01   -5.75e-03   -2.81e-03   -6.76e-03
-1.00e-01   -1.97e-03   -9.48e-04   -2.32e-03
1.000e-01   1.945e-03   9.285e-04   2.307e-03
3.000e-01   5.507e-03   2.640e-03   6.599e-03
5.000e-01   8.649e-03   4.168e-03   1.048e-02
7.000e-01   1.136e-02   5.504e-03   1.393e-02
9.000e-01   1.364e-02   6.636e-03   1.693e-02
1.100e+00   1.547e-02   7.551e-03   1.950e-02
1.300e+00   1.688e-02   8.240e-03   2.162e-02
1.500e+00   9.632e-02   4.783e-02   2.331e-02
1.700e+00   1.012e-01   4.994e-02   1.302e-01
1.900e+00   1.039e-01   5.118e-02   1.369e-01
2.100e+00   1.053e-01   5.184e-02   1.412e-01
2.300e+00   1.060e-01   5.223e-02   1.436e-01
2.500e+00   1.065e-01   5.251e-02   1.449e-01
2.700e+00   1.069e-01   5.274e-02   1.458e-01
2.900e+00   1.073e-01   5.293e-02   1.464e-01
3.100e+00   1.076e-01   5.309e-02   1.470e-01
3.300e+00   1.078e-01   5.324e-02   1.475e-01
3.500e+00   1.081e-01   5.344e-02   1.479e-01
3.700e+00   1.083e-01   6.705e-02   1.483e-01
3.900e+00   1.086e-01   2.529e+00   1.487e-01
4.100e+00   1.103e-01   1.438e+01   1.491e-01
4.300e+00   1.437e+00   2.638e+01   1.503e-01
```

```
4.500e+00   1.800e+01   3.839e+01   1.810e-01
4.700e+00   3.519e+01   5.041e+01   9.452e+00
4.900e+00   5.241e+01   6.419e+01   2.664e+01
5.100e+00   7.505e+01   8.210e+01   4.384e+01
5.300e+00   1.007e+02   1.000e+02   6.224e+01
5.500e+00   1.264e+02   1.179e+02   8.794e+01
5.700e+00   1.522e+02   1.359e+02   1.136e+02
5.900e+00   1.779e+02   1.538e+02   1.394e+02
6.100e+00   2.036e+02   1.717e+02   1.651e+02
6.300e+00   2.293e+02   1.896e+02   1.908e+02
6.500e+00   2.550e+02   2.075e+02   2.165e+02
6.600e+00   2.678e+02   2.165e+02   2.293e+02
|
[Pullup]
|voltage        I(typ)        I(min)        I(max)
|
-3.30e+00   2.677e+02   1.896e+02   2.677e+02
-3.10e+00   2.420e+02   1.716e+02   2.420e+02
-2.90e+00   2.163e+02   1.537e+02   2.163e+02
-2.70e+00   1.906e+02   1.358e+02   1.906e+02
-2.50e+00   1.649e+02   1.179e+02   1.649e+02
-2.30e+00   1.392e+02   9.996e+01   1.392e+02
-2.10e+00   1.135e+02   8.205e+01   1.135e+02
-1.90e+00   8.778e+01   6.413e+01   8.778e+01
-1.70e+00   6.208e+01   5.035e+01   6.208e+01
-1.50e+00   4.368e+01   3.834e+01   4.368e+01
-1.30e+00   2.649e+01   2.633e+01   2.649e+01
-1.10e+00   9.302e+00   1.433e+01   9.303e+00
-9.00e-01   3.838e-02   2.477e+00   4.183e-02
-7.00e-01   8.115e-03   1.789e-02   1.045e-02
-5.00e-01   5.634e-03   3.503e-03   7.064e-03
-3.00e-01   3.370e-03   2.053e-03   4.233e-03
-1.00e-01   1.118e-03   6.789e-04   1.410e-03
1.000e-01   -1.09e-03   -6.56e-04   -1.38e-03
3.000e-01   -3.12e-03   -1.86e-03   -3.99e-03
5.000e-01   -4.96e-03   -2.93e-03   -6.39e-03
7.000e-01   -6.60e-03   -3.87e-03   -8.59e-03
9.000e-01   -8.04e-03   -4.66e-03   -1.06e-02
1.100e+00   -9.26e-03   -5.30e-03   -1.23e-02
1.300e+00   -1.03e-02   -4.75e-02   -1.41e-02
1.500e+00   -9.03e-02   -5.02e-02   -1.23e-01
1.700e+00   -9.49e-02   -5.21e-02   -1.31e-01
1.900e+00   -9.84e-02   -5.34e-02   -1.38e-01
2.100e+00   -1.01e-01   -5.45e-02   -1.43e-01
2.300e+00   -1.03e-01   -5.54e-02   -1.47e-01
2.500e+00   -1.05e-01   -5.62e-02   -1.50e-01
2.700e+00   -1.06e-01   -5.68e-02   -1.52e-01
2.900e+00   -1.07e-01   -5.74e-02   -1.54e-01
3.100e+00   -1.08e-01   -5.79e-02   -1.56e-01
3.300e+00   -1.09e-01   -5.84e-02   -1.57e-01
3.500e+00   -1.10e-01   -5.89e-02   -1.59e-01
3.700e+00   -1.11e-01   -6.49e-02   -1.60e-01
3.900e+00   -1.11e-01   -1.23e+00   -1.61e-01
```

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4.100e+00   -1.14e-01   -2.16e+01   -1.62e-01
4.300e+00   -4.76e-01   -4.52e+01   -1.64e-01
4.500e+00   -2.73e+01   -6.89e+01   -1.73e-01
4.700e+00   -6.14e+01   -9.25e+01   -7.82e+00
4.900e+00   -9.54e+01   -1.17e+02   -4.19e+01
5.100e+00   -1.38e+02   -1.52e+02   -7.59e+01
5.300e+00   -1.89e+02   -1.88e+02   -1.11e+02
5.500e+00   -2.40e+02   -2.23e+02   -1.61e+02
5.700e+00   -2.91e+02   -2.59e+02   -2.12e+02
5.900e+00   -3.42e+02   -2.94e+02   -2.63e+02
6.100e+00   -3.93e+02   -3.30e+02   -3.14e+02
6.300e+00   -4.44e+02   -3.65e+02   -3.65e+02
6.500e+00   -4.95e+02   -4.01e+02   -4.16e+02
6.600e+00   -5.20e+02   -4.18e+02   -4.41e+02
|
[GND_clamp]
|voltage        I(typ)        I(min)        I(max)
|
-3.30e+00   -5.20e+02   -3.65e+02   -5.18e+02
-3.10e+00   -4.69e+02   -3.30e+02   -4.67e+02
-2.90e+00   -4.18e+02   -2.94e+02   -4.16e+02
-2.70e+00   -3.67e+02   -2.59e+02   -3.65e+02
-2.50e+00   -3.16e+02   -2.23e+02   -3.14e+02
-2.30e+00   -2.65e+02   -1.88e+02   -2.63e+02
-2.10e+00   -2.14e+02   -1.52e+02   -2.11e+02
-1.90e+00   -1.63e+02   -1.17e+02   -1.60e+02
-1.70e+00   -1.13e+02   -9.25e+01   -1.10e+02
-1.50e+00   -7.83e+01   -6.88e+01   -7.58e+01
-1.30e+00   -4.42e+01   -4.51e+01   -4.17e+01
-1.10e+00   -1.02e+01   -2.15e+01   -7.66e+00
-9.00e-01   -1.03e-02   -1.17e+00   -9.27e-03
-7.00e-01   -3.74e-04   -5.73e-03   -1.14e-03
-5.00e-01   -1.72e-06   -5.06e-05   -1.28e-05
-3.00e-01   -1.67e-09   -4.65e-07   -1.10e-08
-1.00e-01   -2.03e-11   -4.80e-09   -2.71e-11
0.000e+00   -1.69e-11   -1.61e-09   -1.89e-11
|
[POWER_clamp]
|voltage        I(typ)        I(min)        I(max)
|
-3.30e+00   2.677e+02   1.896e+02   2.677e+02
-3.10e+00   2.420e+02   1.716e+02   2.420e+02
-2.90e+00   2.163e+02   1.537e+02   2.163e+02
-2.70e+00   1.906e+02   1.358e+02   1.906e+02
-2.50e+00   1.649e+02   1.179e+02   1.649e+02
-2.30e+00   1.392e+02   9.996e+01   1.392e+02
-2.10e+00   1.135e+02   8.205e+01   1.135e+02
-1.90e+00   8.778e+01   6.413e+01   8.778e+01
-1.70e+00   6.208e+01   5.035e+01   6.208e+01
-1.50e+00   4.368e+01   3.834e+01   4.368e+01
-1.30e+00   2.649e+01   2.633e+01   2.649e+01
-1.10e+00   9.300e+00   1.433e+01   9.301e+00
-9.00e-01   2.962e-02   2.475e+00   3.075e-02
```

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-7.00e-01   2.501e-04   1.354e-02   6.708e-04
-5.00e-01   2.066e-06   6.280e-05   1.204e-05
-3.00e-01   2.487e-09   5.128e-07   1.417e-08
-1.00e-01   5.672e-11   5.639e-09   6.832e-11
0.000e+00   5.334e-11   1.992e-09   5.783e-11
|
[Ramp]
R_load = 50.00
|voltage        I(typ)        I(min)        I(max)
|
|
dV/dt_r        1.570/0.200    1.210/0.411    1.810/0.149
|
|
dV/dt_f        1.590/0.304    1.170/0.673    1.800/0.205
|
[End]|
[Model]        ipbw_i
Model_type        Input
Polarity        Non-Inverting
Vinl= 0.8000v
Vinh= 2.000v
C_comp        5.00pF        5.00pF        5.00pF
|
|
[Voltage Range]      3.3v      3v      3.6v
[GND_clamp]
|voltage        I(typ)        I(min)        I(max)
|
-3.30e+00   -5.20e+02   -3.65e+02   -5.17e+02
-3.10e+00   -4.69e+02   -3.29e+02   -4.66e+02
-2.90e+00   -4.18e+02   -2.94e+02   -4.15e+02
-2.70e+00   -3.67e+02   -2.58e+02   -3.64e+02
-2.50e+00   -3.16e+02   -2.23e+02   -3.13e+02
-2.30e+00   -2.65e+02   -1.88e+02   -2.62e+02
-2.10e+00   -2.14e+02   -1.52e+02   -2.11e+02
-1.90e+00   -1.63e+02   -1.17e+02   -1.60e+02
-1.70e+00   -1.13e+02   -9.24e+01   -1.10e+02
-1.50e+00   -7.82e+01   -6.87e+01   -7.57e+01
-1.30e+00   -4.42e+01   -4.51e+01   -4.16e+01
-1.10e+00   -1.02e+01   -2.15e+01   -7.64e+00
-9.00e-01   -7.17e-03   -1.16e+00   -4.87e-03
-7.00e-01   -1.14e-04   -4.39e-03   -3.03e-04
-5.00e-01   -4.86e-07   -2.55e-05   -2.73e-06
-3.00e-01   -5.19e-10   -1.91e-07   -2.57e-09
-1.00e-01   -1.91e-11   -2.47e-09   -2.19e-11
0.000e+00   -1.68e-11   -1.17e-09   -1.84e-11
|
[POWER_clamp]
|voltage        I(typ)        I(min)        I(max)
|
-3.30e+00   2.667e+02   1.885e+02   2.667e+02
-3.10e+00   2.411e+02   1.707e+02   2.411e+02
```

```
-2.90e+00   2.155e+02   1.528e+02   2.155e+02
-2.70e+00   1.898e+02   1.350e+02   1.898e+02
-2.50e+00   1.642e+02   1.172e+02   1.642e+02
-2.30e+00   1.386e+02   9.935e+01   1.386e+02
-2.10e+00   1.130e+02   8.152e+01   1.130e+02
-1.90e+00   8.739e+01   6.369e+01   8.739e+01
-1.70e+00   6.178e+01   4.999e+01   6.178e+01
-1.50e+00   4.346e+01   3.806e+01   4.346e+01
-1.30e+00   2.634e+01   2.613e+01   2.634e+01
-1.10e+00   9.237e+00   1.421e+01   9.237e+00
-9.00e-01   2.454e-02   2.430e+00   2.488e-02
-7.00e-01   8.741e-05   1.104e-02   2.050e-04
-5.00e-01   6.316e-07   4.079e-05   2.961e-06
-3.00e-01   8.479e-10   2.484e-07   3.721e-09
-1.00e-01   4.420e-11   3.001e-09   4.943e-11
0.000e+00   4.215e-11   1.346e-09   4.543e-11
|
[End]|
[Model]        ipbw_io
Model_type        I/O
Polarity        Non-Inverting
Vinl= 0.8000v
Vinh= 2.000v
C_comp        5.00pF        5.00pF        5.00pF
|
|
[Voltage Range]      3.3v      3v      3.6v
[Pulldown]
|voltage        I(typ)        I(min)        I(max)
|
-3.30e+00   -5.20e+02   -3.65e+02   -5.17e+02
-3.10e+00   -4.69e+02   -3.29e+02   -4.66e+02
-2.90e+00   -4.18e+02   -2.94e+02   -4.15e+02
-2.70e+00   -3.67e+02   -2.58e+02   -3.64e+02
-2.50e+00   -3.16e+02   -2.23e+02   -3.13e+02
-2.30e+00   -2.65e+02   -1.88e+02   -2.62e+02
-2.10e+00   -2.14e+02   -1.52e+02   -2.11e+02
-1.90e+00   -1.63e+02   -1.17e+02   -1.60e+02
-1.70e+00   -1.13e+02   -9.24e+01   -1.10e+02
-1.50e+00   -7.82e+01   -6.87e+01   -7.57e+01
-1.30e+00   -4.42e+01   -4.51e+01   -4.17e+01
-1.10e+00   -1.02e+01   -2.15e+01   -7.66e+00
-9.00e-01   -3.69e-02   -1.17e+00   -3.79e-02
-7.00e-01   -2.52e-02   -1.67e-02   -2.81e-02
-5.00e-01   -1.83e-02   -9.77e-03   -2.04e-02
-3.00e-01   -1.11e-02   -5.89e-03   -1.24e-02
-1.00e-01   -3.77e-03   -1.98e-03   -4.20e-03
1.000e-01   3.729e-03   1.940e-03   4.177e-03
3.000e-01   1.076e-02   5.578e-03   1.216e-02
5.000e-01   1.723e-02   8.907e-03   1.965e-02
7.000e-01   2.311e-02   1.191e-02   2.663e-02
9.000e-01   2.836e-02   1.455e-02   3.305e-02
1.100e+00   3.292e-02   1.680e-02   3.887e-02
```

```
1.300e+00   3.675e-02   1.862e-02   4.404e-02
1.500e+00   3.979e-02   1.997e-02   4.850e-02
1.700e+00   4.205e-02   2.085e-02   5.223e-02
1.900e+00   4.347e-02   2.136e-02   5.518e-02
2.100e+00   4.413e-02   2.162e-02   5.728e-02
2.300e+00   4.445e-02   2.176e-02   5.843e-02
2.500e+00   4.465e-02   2.186e-02   5.899e-02
2.700e+00   4.479e-02   2.194e-02   5.931e-02
2.900e+00   4.492e-02   2.200e-02   5.953e-02
3.100e+00   4.502e-02   2.206e-02   5.971e-02
3.300e+00   4.511e-02   2.211e-02   5.986e-02
3.500e+00   4.519e-02   2.219e-02   5.999e-02
3.700e+00   4.526e-02   3.324e-02   6.010e-02
3.900e+00   4.536e-02   2.452e+00   6.021e-02
4.100e+00   4.614e-02   1.423e+01   6.032e-02
4.300e+00   1.344e+00   2.615e+01   6.065e-02
4.500e+00   1.783e+01   3.808e+01   8.548e-02
4.700e+00   3.495e+01   5.001e+01   9.298e+00
4.900e+00   5.208e+01   6.371e+01   2.640e+01
5.100e+00   7.463e+01   8.154e+01   4.352e+01
5.300e+00   1.002e+02   9.937e+01   6.184e+01
5.500e+00   1.259e+02   1.172e+02   8.745e+01
5.700e+00   1.515e+02   1.350e+02   1.131e+02
5.900e+00   1.771e+02   1.529e+02   1.387e+02
6.100e+00   2.027e+02   1.707e+02   1.643e+02
6.300e+00   2.283e+02   1.885e+02   1.899e+02
6.500e+00   2.539e+02   2.064e+02   2.155e+02
6.600e+00   2.667e+02   2.153e+02   2.283e+02
|
[Pullup]
|voltage        I(typ)        I(min)        I(max)
|
-3.30e+00   2.667e+02   1.885e+02   2.667e+02
-3.10e+00   2.411e+02   1.707e+02   2.411e+02
-2.90e+00   2.155e+02   1.528e+02   2.155e+02
-2.70e+00   1.898e+02   1.350e+02   1.898e+02
-2.50e+00   1.642e+02   1.172e+02   1.642e+02
-2.30e+00   1.386e+02   9.935e+01   1.386e+02
-2.10e+00   1.130e+02   8.152e+01   1.130e+02
-1.90e+00   8.739e+01   6.369e+01   8.739e+01
-1.70e+00   6.178e+01   4.999e+01   6.178e+01
-1.50e+00   4.346e+01   3.806e+01   4.346e+01
-1.30e+00   2.635e+01   2.613e+01   2.635e+01
-1.10e+00   9.243e+00   1.421e+01   9.245e+00
-9.00e-01   5.536e-02   2.435e+00   6.260e-02
-7.00e-01   2.847e-02   2.689e-02   3.437e-02
-5.00e-01   2.025e-02   1.265e-02   2.451e-02
-3.00e-01   1.208e-02   7.503e-03   1.467e-02
-1.00e-01   3.994e-03   2.474e-03   4.868e-03
1.000e-01   -3.88e-03   -2.38e-03   -4.76e-03
3.000e-01   -1.11e-02   -6.76e-03   -1.37e-02
5.000e-01   -1.76e-02   -1.06e-02   -2.20e-02
7.000e-01   -2.35e-02   -1.40e-02   -2.95e-02
```

```
9.000e-01   -2.86e-02   -1.69e-02   -3.63e-02
1.100e+00   -3.30e-02   -1.93e-02   -4.23e-02
1.300e+00   -3.65e-02   -2.10e-02   -4.75e-02
1.500e+00   -3.92e-02   -2.22e-02   -5.17e-02
1.700e+00   -4.12e-02   -2.29e-02   -5.51e-02
1.900e+00   -4.26e-02   -2.35e-02   -5.77e-02
2.100e+00   -4.36e-02   -2.38e-02   -5.97e-02
2.300e+00   -4.43e-02   -2.42e-02   -6.11e-02
2.500e+00   -4.49e-02   -2.44e-02   -6.22e-02
2.700e+00   -4.54e-02   -2.47e-02   -6.31e-02
2.900e+00   -4.58e-02   -2.49e-02   -6.38e-02
3.100e+00   -4.61e-02   -2.50e-02   -6.44e-02
3.300e+00   -4.65e-02   -2.52e-02   -6.49e-02
3.500e+00   -4.68e-02   -2.54e-02   -6.54e-02
3.700e+00   -4.70e-02   -2.99e-02   -6.58e-02
3.900e+00   -4.73e-02   -1.19e+00   -6.62e-02
4.100e+00   -4.81e-02   -2.15e+01   -6.66e-02
4.300e+00   -4.00e-01   -4.51e+01   -6.72e-02
4.500e+00   -2.72e+01   -6.87e+01   -7.21e-02
4.700e+00   -6.12e+01   -9.24e+01   -7.70e+00
4.900e+00   -9.52e+01   -1.17e+02   -4.17e+01
5.100e+00   -1.37e+02   -1.52e+02   -7.57e+01
5.300e+00   -1.88e+02   -1.88e+02   -1.10e+02
5.500e+00   -2.39e+02   -2.23e+02   -1.60e+02
5.700e+00   -2.90e+02   -2.58e+02   -2.11e+02
5.900e+00   -3.41e+02   -2.94e+02   -2.62e+02
6.100e+00   -3.92e+02   -3.29e+02   -3.13e+02
6.300e+00   -4.43e+02   -3.65e+02   -3.64e+02
6.500e+00   -4.94e+02   -4.00e+02   -4.15e+02
6.600e+00   -5.20e+02   -4.18e+02   -4.41e+02
|
[GND_clamp]
|voltage        I(typ)        I(min)        I(max)
|
-3.30e+00   -5.20e+02   -3.65e+02   -5.17e+02
-3.10e+00   -4.69e+02   -3.29e+02   -4.66e+02
-2.90e+00   -4.18e+02   -2.94e+02   -4.15e+02
-2.70e+00   -3.67e+02   -2.58e+02   -3.64e+02
-2.50e+00   -3.16e+02   -2.23e+02   -3.13e+02
-2.30e+00   -2.65e+02   -1.88e+02   -2.62e+02
-2.10e+00   -2.14e+02   -1.52e+02   -2.11e+02
-1.90e+00   -1.63e+02   -1.17e+02   -1.60e+02
-1.70e+00   -1.13e+02   -9.24e+01   -1.10e+02
-1.50e+00   -7.82e+01   -6.87e+01   -7.57e+01
-1.30e+00   -4.42e+01   -4.51e+01   -4.16e+01
-1.10e+00   -1.02e+01   -2.15e+01   -7.64e+00
-9.00e-01   -7.17e-03   -1.16e+00   -4.87e-03
-7.00e-01   -1.14e-04   -4.39e-03   -3.03e-04
-5.00e-01   -4.86e-07   -2.55e-05   -2.73e-06
-3.00e-01   -5.19e-10   -1.91e-07   -2.57e-09
-1.00e-01   -1.91e-11   -2.47e-09   -2.19e-11
0.000e+00   -1.68e-11   -1.17e-09   -1.84e-11
|
```

```
[POWER_clamp]
|voltage        I(typ)        I(min)        I(max)
|
-3.30e+00   2.667e+02   1.885e+02   2.667e+02
-3.10e+00   2.411e+02   1.707e+02   2.411e+02
-2.90e+00   2.155e+02   1.528e+02   2.155e+02
-2.70e+00   1.898e+02   1.350e+02   1.898e+02
-2.50e+00   1.642e+02   1.172e+02   1.642e+02
-2.30e+00   1.386e+02   9.935e+01   1.386e+02
-2.10e+00   1.130e+02   8.152e+01   1.130e+02
-1.90e+00   8.739e+01   6.369e+01   8.739e+01
-1.70e+00   6.178e+01   4.999e+01   6.178e+01
-1.50e+00   4.346e+01   3.806e+01   4.346e+01
-1.30e+00   2.634e+01   2.613e+01   2.634e+01
-1.10e+00   9.237e+00   1.421e+01   9.237e+00
-9.00e-01   2.454e-02   2.430e+00   2.488e-02
-7.00e-01   8.741e-05   1.104e-02   2.050e-04
-5.00e-01   6.316e-07   4.079e-05   2.961e-06
-3.00e-01   8.479e-10   2.484e-07   3.721e-09
-1.00e-01   4.420e-11   3.001e-09   4.943e-11
0.000e+00   4.215e-11   1.346e-09   4.543e-11
|
[Ramp]
R_load = 50.00
|voltage        I(typ)        I(min)        I(max)
|
|
dV/dt_r        1.140/0.494    0.699/0.978    1.400/0.354
|
|
dV/dt_f        1.150/0.505    0.642/0.956    1.350/0.350
|
[End]|
[Model]        iexlh_i
Model_type        Input
Polarity        Non-Inverting
Vinl= 0.8000v
Vinh= 2.000v
C_comp        5.00pF        5.00pF        5.00pF
|
|
[Voltage Range]      3.3v      3v      3.6v
[GND_clamp]
|voltage        I(typ)        I(min)        I(max)
|
-3.30e+00   -5.21e+02   -3.66e+02   -5.18e+02
-3.10e+00   -4.70e+02   -3.30e+02   -4.67e+02
-2.90e+00   -4.19e+02   -2.95e+02   -4.16e+02
-2.70e+00   -3.68e+02   -2.59e+02   -3.65e+02
-2.50e+00   -3.17e+02   -2.24e+02   -3.14e+02
-2.30e+00   -2.66e+02   -1.89e+02   -2.63e+02
-2.10e+00   -2.15e+02   -1.53e+02   -2.12e+02
-1.90e+00   -1.64e+02   -1.18e+02   -1.61e+02
```

```
-1.70e+00   -1.14e+02   -9.34e+01   -1.11e+02
-1.50e+00   -7.93e+01   -6.98e+01   -7.68e+01
-1.30e+00   -4.53e+01   -4.62e+01   -4.28e+01
-1.10e+00   -1.13e+01   -2.26e+01   -8.78e+00
-9.00e-01   -7.94e-03   -1.87e+00   -3.77e-03
-7.00e-01   -1.62e-06   -5.11e-03   -7.69e-07
-5.00e-01   -3.45e-10   -1.40e-05   -1.72e-10
-3.00e-01   -1.29e-11   -3.90e-08   -1.38e-11
-1.00e-01   -1.10e-11   -8.67e-10   -1.19e-11
0.000e+00   -1.01e-11   -7.13e-10   -1.10e-11
|
[POWER_clamp]
|voltage        I(typ)        I(min)        I(max)
|
-3.30e+00   2.653e+02   1.870e+02   2.653e+02
-3.10e+00   2.398e+02   1.693e+02   2.398e+02
-2.90e+00   2.143e+02   1.516e+02   2.143e+02
-2.70e+00   1.888e+02   1.339e+02   1.888e+02
-2.50e+00   1.633e+02   1.162e+02   1.633e+02
-2.30e+00   1.378e+02   9.847e+01   1.378e+02
-2.10e+00   1.123e+02   8.076e+01   1.123e+02
-1.90e+00   8.682e+01   6.305e+01   8.682e+01
-1.70e+00   6.133e+01   4.947e+01   6.133e+01
-1.50e+00   4.313e+01   3.766e+01   4.313e+01
-1.30e+00   2.614e+01   2.585e+01   2.614e+01
-1.10e+00   9.145e+00   1.404e+01   9.145e+00
-9.00e-01   1.797e-02   2.364e+00   1.797e-02
-7.00e-01   3.667e-06   7.589e-03   3.667e-06
-5.00e-01   7.730e-10   2.072e-05   7.748e-10
-3.00e-01   2.293e-11   5.767e-08   2.476e-11
-1.00e-01   2.096e-11   1.163e-09   2.278e-11
0.000e+00   2.004e-11   9.618e-10   2.186e-11
|
[End]
```

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