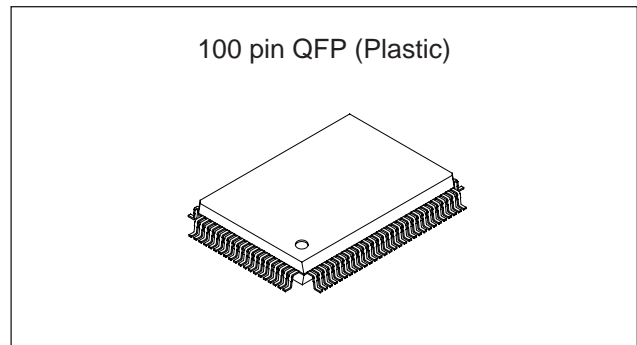


CMOS 8-bit Single Chip Microcomputer

Description

The CXP82032/82040/82052/82060 is a CMOS 8-bit single chip microcomputer integrating on a single chip an A/D converter, serial interface, timer/counter, time-base timer, capture timer/counter, fluorescent display panel controller/driver, remote control reception circuit, and PWM output besides the basic configurations of 8-bit CPU, ROM, RAM, and I/O port.

The CXP82032/82040/82052/82060 also provides sleep/stop function that enables lower power consumption.



Features

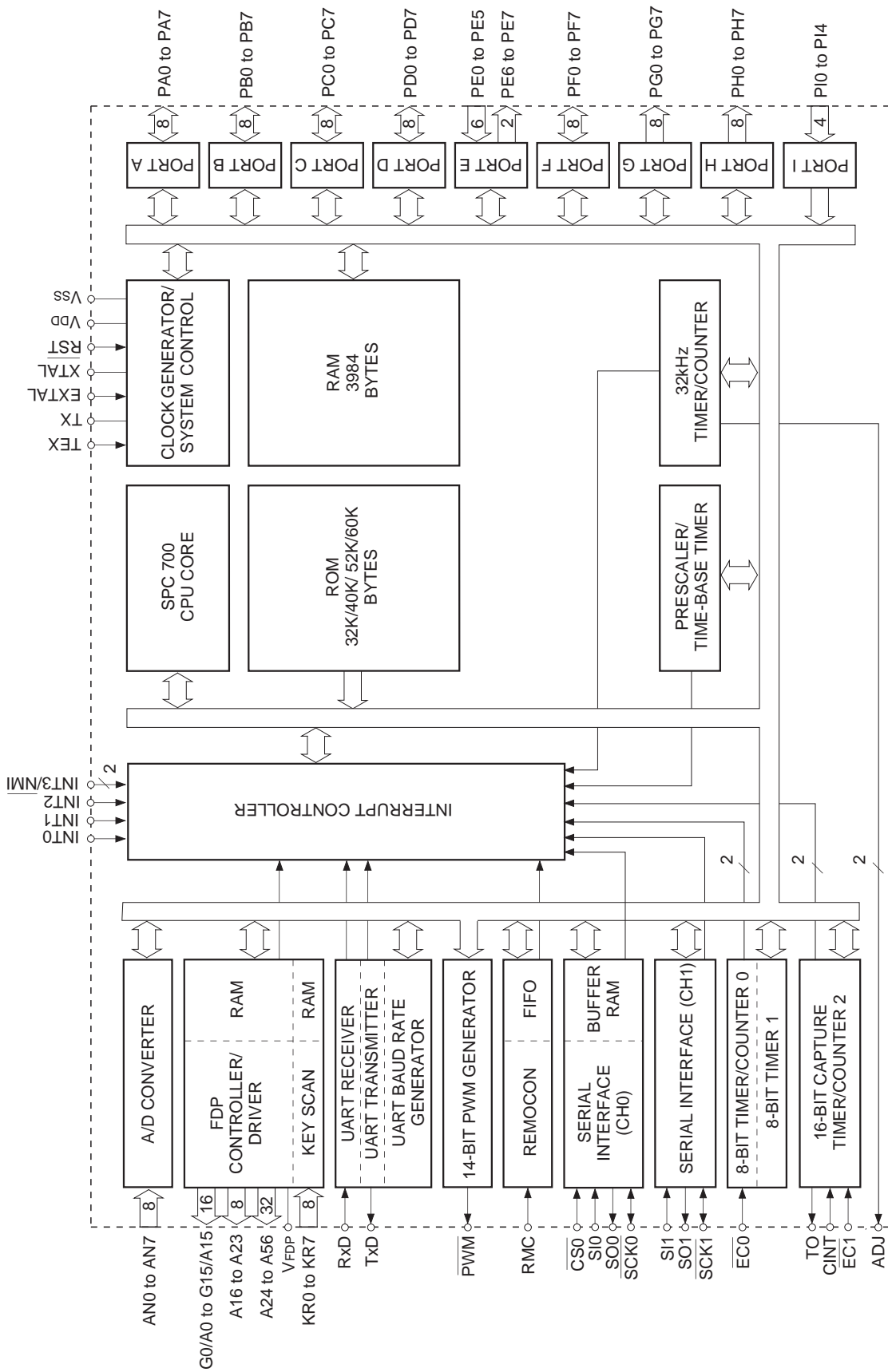
- Wide-range instruction system (213 instructions) to cover various types of data
 - 16-bit arithmetic/multiplication and division/boolean bit operation instructions
- Minimum instruction cycle
 - 250ns at 16MHz operation
 - 122µs at 32kHz operation
- Incorporated ROM capacity
 - 32k bytes (CXP82032)
 - 40k bytes (CXP82040)
 - 52K bytes (CXP82052)
 - 60K bytes (CXP82060)
- Incorporated RAM capacity
 - 3984 bytes (including fluorescent display area)
- Peripheral functions
 - A/D converter
 - 8 bits, 8 channels, successive approximation method (Conversion time of 3.25µs/16MHz)
 - Serial interface
 - Buffer RAM incorporated (Auto transfer for 1 to 32 bytes), 1 channel
 - 8-bit clock synchronized type (MSB/LSB first selectable), 1 channel
 - Start-stop synchronized type (UART), 1 channel
 - Timers
 - 8-bit timer, 8-bit timer/counter, 19-bit time-base timer
 - 16-bit capture timer/counter, 32kHz timer/counter
 - Fluorescent display panel controller/driver
 - Supports the universal grid fluorescent display panel.
 - High voltage drive output port of 56 pins (40V)
 - Maximum of 640 segments display possible
 - Display timing number of 1 to 20
 - Dimmer function
 - Incorporated pull-down resistor (Mask option)
 - Hardware key scan function (Maximum of 16 × 8 key matrix supportable)
 - Remote control reception circuit
 - 8-bit pulse measurement counter, 6-stage FIFO
 - PWM output
 - 14 bits, 1 channel
- Interruption
 - 17 factors, 15 vectors, multi-interruption possible
- Standby mode
 - Sleep/stop
- Package
 - 100-pin plastic QFP
 - CXP82000 100-pin ceramic QFP
- Piggy/evaluation chip

Structure

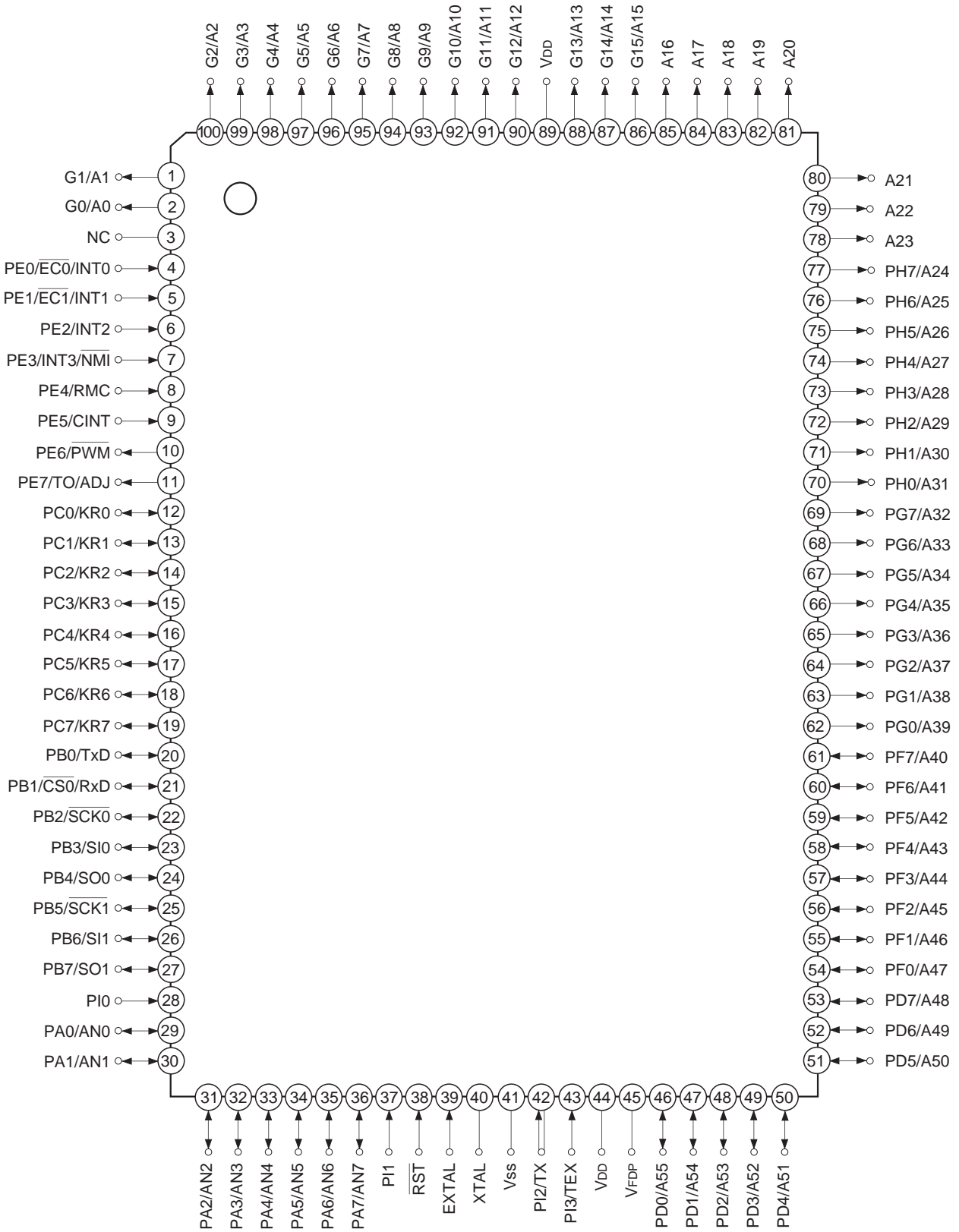
Silicon gate CMOS IC

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Block Diagram



Pin Assignment (Top View)



- Note)** 1. NC (Pin 3) is left open.
 2. VDD (Pins 44 and 89) must be connected to VDD.

Pin Description

| Symbol | I/O | Functions | | |
|---------------------------------------|--------------------------|---|--|--|
| PA0/AN0 to PA7/AN7 | I/O/ Analog input | (Port A) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of the pull-up resistor can be set through the program in a unit of 4 bits. (8 pins) | Analog inputs to A/D converter. (8 pins) | |
| PB0/TxD | I/O/Output | (Port B) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of the pull-up resistor can be set through the program in a unit of 4 bits. (8 pins) | UART transmission data output. | |
| PB1/ $\overline{\text{CS0}}$ / RxD | I/O/Input/ Input | | Chip select input for serial interface (CH0). | UART reception data input pin. |
| PB2/ $\overline{\text{SCK0}}$ | I/O/I/O | | Serial clock I/O (CH0). | |
| PB3/SI0 | I/O/Input | | Serial data input (CH0). | |
| PB4/SO0 | I/O/Output | | Serial data output (CH0). | |
| PB5/ $\overline{\text{SCK1}}$ | I/O/I/O | | Serial clock I/O (CH1). | |
| PB6/SI1 | I/O/Input | | Serial data input (CH1). | |
| PB7/SO1 | I/O/Output | | Serial data output (CH1). | |
| PC0/KR0 to PC7/KR7 | I/O/Input | (Port C) 8-bit I/O port. I/O can be set in a unit of single bits. Can drive 12mA sink current. Incorporation of the pull-up resistor can be set through the program in a unit of 4 bits. (8 pins) | Serves as key return inputs when operating key scan with fluorescent display panel (FDP) segment signal. (8 pins) | |
| PD0/A55 to PD7/A48 | I/O/Output | (Port D) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins) | FDP segment signal (anode connection) outputs. | |
| PE0/INT0/ EC0 | Input/Input/ Input | (Port E) 8-bit port. Lower 6 bits are for inputs; upper 2 bits are for outputs. (8 pins) | Inputs for external interruption request. (4 pins) | External event inputs for timer/counter. (2 pins) |
| PE1/INT1/ EC1 | Input/Input/ Input | | | Non-maskable interruption request input. |
| PE2/INT2 | Input/Input | | Remote control reception circuit input. | |
| PE3/INT3/ NMI | Input/Input/ Input | | External capture input to 16-bit timer/counter. | |
| PE4/RMC | Input/Input | | 14-bit PWM output. | |
| PE5/CINT | Input/Input | | Output for the 16-bit timer/counter rectangular waves, and 32kHz oscillation frequency division. | |
| PE6/ $\overline{\text{PWM}}$ | Output/Output | | | |
| PE7/TO/ ADJ | Output/Output/ Output | | | |

| Symbol | I/O | Functions | |
|--------------------------|---------------|---|--|
| PF0/A47 to PF7/A40 | I/O/Output | (Port F) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins) | FDP segment signal (anode connection) outputs. (8 pins) |
| PG0/A39 to PG7/A32 | Output/Output | (Port G) 8-bit output port. (8 pins) | FDP segment signal (anode connection) outputs. (8 pins) |
| PH0/A31 to PH7/A24 | Output/Output | (Port H) 8-bit output port. (8 pins) | FDP segment signal (anode connection) outputs. (8 pins) |
| PI0 | Input | (Port I) 4-bit input port. (4 pins) | Crystal connectors for 32kHz timer/counter clock oscillation. For usage as event counter, input to TEX, and leave TX open. |
| PI1 | Input | | |
| PI2/TX | Input | | |
| PI3/TEX | Input/Input | | |
| A16 to A23 | Output | FDP segment signal (anode connection) outputs. (8 pins) | |
| G0/A0 to G15/A15 | Output/Output | Outputs for FDP timing signals (grid connection)/segment signals (anode connection). (16 pins) | |
| V _{FDP} | | FDP voltage supply when incorporated pull-down (PD) resistor is set by mask option. | |
| EXTAL | Input | Crystal connectors for system clock oscillation. When the clock is supplied externally, input to EXTAL; opposite phase clock should be input to XTAL. | |
| XTAL | | | |
| $\overline{\text{RST}}$ | Input | Low-level active, system reset. | |
| NC | | NC. Under normal operation, leave this pin open. | |
| V _{DD} | | V _{CC} supply. | |
| V _{SS} | | GND. | |

I/O Circuit Format for Pins

| Pin | Circuit format | After a reset |
|--|---|---------------|
| <p>PA0/AN0 to PA7/AN7</p> <p>8 pins</p> | <p>Port A</p> <p>Pull-up resistor "0" after a reset</p> <p>Port A data</p> <p>Port A direction "0" after a reset</p> <p>Internal data bus</p> <p>RD (Port A)</p> <p>Port A input selection "0" after a reset</p> <p>Input multiplexer</p> <p>A/D converter</p> <p>IP Input protection circuit</p> <p>* Pull-up transistor approx. 100kΩ</p> | <p>Hi-Z</p> |
| <p>PB0/TxD PB1/CS0/RxD PB3/SI0 PB6/SI1</p> <p>4 pins</p> | <p>Port B</p> <p>Pull-up resistor "0" after a reset</p> <p>Port B data</p> <p>Port B direction "0" after a reset</p> <p>Internal data bus</p> <p>RD (Port B)</p> <p>CS0 SI0 SI1 RxD</p> <p>Schmitt input (PB0/TxD excluded)</p> <p>IP</p> <p>* Pull-up transistor approx. 100kΩ</p> | <p>Hi-Z</p> |
| <p>PB2/SCK0 PB5/SCK1</p> <p>2 pins</p> | <p>Port B</p> <p>Pull-up resistor "0" after a reset</p> <p>SCK OUT</p> <p>Serial clock output enable</p> <p>Port B output selection "0" after a reset</p> <p>Port B data</p> <p>Port B direction "0" after a reset</p> <p>Internal data bus</p> <p>RD (Port B)</p> <p>SCK IN</p> <p>Schmitt input</p> <p>IP</p> <p>* Pull-up transistor approx. 100kΩ</p> | <p>Hi-Z</p> |

| Pin | Circuit format | After a reset |
|---|--|-------------------|
| <p>PB4/SO0 PB7/SO1</p> <p>2 pins</p> | <p>Port B</p> <p>* Pull-up transistor approx. 100kΩ</p> | <p>Hi-Z</p> |
| <p>PC0/KR0 to PC7/KR7</p> <p>8 pins</p> | <p>Port C</p> <p>*1 Large current 12mA *2 Pull-up transistor approx. 100kΩ</p> | <p>Hi-Z</p> |
| <p>PE0/$\overline{EC0}$/INT0 PE1/$\overline{EC1}$/INT1 PE2/INT2 PE3/INT3/$\overline{NM1}$ PE4/RMC PE5/CINT</p> <p>6 pins</p> | <p>Port E</p> | <p>Hi-Z</p> |
| <p>PE6/\overline{PWM}</p> <p>1 pin</p> | <p>Port E</p> | <p>High level</p> |

| Pin | Circuit format | After a reset |
|---|---|--|
| <p>PE7/TO/ADJ</p> <p>1 pin</p> | <p>Port E</p> <p>Internal reset signal</p> <p>Port E data</p> <p>"1" after a reset TO</p> <p>ADJ16K*1</p> <p>ADJ2K*2</p> <p>MPX</p> <p>Port E output selection (upper)</p> <p>Port E output selection (lower)</p> <p>"00" after a reset</p> <p>TO output enable</p> <p>*1 ADJ signal is a frequency dividing output for 32kHz oscillation frequency adjustment. ADJ2K can be used for buzzer output.</p> <p>*2 Pull-up transistor approx. 150kΩ</p> | <p>High level (High level at ON resistance of pull-up transistor during a reset)</p> |
| <p>PD0/A55 to PD7/A48 PF0/A47 to PF7/A40</p> <p>16 pins</p> | <p>Port D</p> <p>Port F</p> <p>Segment output data</p> <p>Output selection control signal ("0" after a reset)</p> <p>Port D and F data</p> <p>Port D and F direction</p> <p>"1" after a reset</p> <p>Internal data bus</p> <p>RD (Ports D and F)</p> <p>* High voltage drive transistor</p> | <p>Hi-Z or Low level (when PD resistor is connected)</p> |
| <p>PG0/A39 to PG7/A32 PH0/A31 to PH7/A24</p> <p>16 pins</p> | <p>Port G</p> <p>Port H</p> <p>Segment output data</p> <p>Output selection control signal ("0" after a reset)</p> <p>Port G and H data</p> <p>"0" after a reset</p> <p>Internal data bus</p> <p>RD (Ports G and H)</p> <p>* High voltage drive transistor</p> <p>Mask option</p> <p>Pull-down resistor</p> <p>V_{FDP}</p> | <p>Hi-Z or Low level (when PD resistor is connected)</p> |
| <p>A16 to A23</p> <p>8 pins</p> | <p>Segment output data</p> <p>Output selection control signal ("0" after a reset)</p> <p>Mask option</p> <p>Pull-down resistor</p> <p>V_{FDP}</p> <p>* High voltage drive transistor</p> | <p>Hi-Z or Low level (when PD resistor is connected)</p> |

| Pin | Circuit format | After a reset |
|--|---|--|
| <p>G0/A0 to G15/A15</p> <p>16 pins</p> | <p>Segment output data Timing output data Output selection control signal ("0" after a reset)</p> <p>Mask option (OP)</p> <p>Pull-down resistor</p> <p>V_{FDP}</p> <p>* High voltage drive transistor</p> | <p>Hi-Z or Low level (when PD resistor is connected)</p> |
| <p>EXTAL XTAL</p> <p>2 pins</p> | <ul style="list-style-type: none"> • Diagram shows circuit composition during oscillation. • Feedback resistor is removed and XTAL becomes High level during stop. | <p>Oscillation</p> |
| <p>PI0 PI1</p> <p>2 pins</p> | <p>Internal data bus</p> <p>RD (Port I)</p> | <p>Hi-Z</p> |
| <p>PI2/TX PI3/TEX</p> <p>2 pins</p> | <p>TEX oscillation circuit control "1" after a reset</p> <p>Internal data bus</p> <p>Internal data bus</p> <p>Clock input</p> <p>RD</p> <p>RD</p> | <p>Oscillation stop Port input</p> |
| <p>$\overline{\text{RST}}$</p> <p>1 pin</p> | <p>Pull-up resistor</p> <p>Mask option (OP)</p> <p>Schmitt input</p> | <p>Low level</p> |

Absolute Maximum Ratings

(V_{SS} = 0V reference)

| Item | Symbol | Rating | Unit | Remarks |
|---------------------------------|-------------------|---|------|---|
| Supply voltage | V _{DD} | -0.3 to +7.0 | V | |
| FDP display supply voltage | V _{FDP} | -40* ² to +7.0* ¹ | V | |
| Input voltage | V _{IN} | -0.3 to +7.0* ¹ | V | |
| Output voltage | V _{OUT} | -0.3 to +7.0* ¹ | V | |
| Display output voltage | V _{OD} | -40* ² to +7.0* ¹ | V | |
| High level output current | I _{OH} | -5 | mA | All pins excluding display outputs* ³ (value per pin) |
| | I _{ODH1} | -15 | mA | Display outputs A20 to A55 (value per pin) |
| | I _{ODH2} | -50 | mA | Display outputs G0/A0 to G15/A15, and A16 to A19 (value per pin) |
| High level total output current | ∑I _{OH} | -30 | mA | Total for all pins excluding display outputs |
| | ∑I _{ODH} | -120 | mA | Total for all display outputs |
| Low level output current | I _{OL} | 15 | mA | Pins excluding large current output (value per pin) |
| | I _{OLC} | 20 | mA | Large current output pins* ⁴ (value per pin) |
| Low level total output current | ∑I _{OL} | 100 | mA | Total for all output pins |
| Operating temperature | T _{opr} | -20 to +75 | °C | |
| Storage temperature | T _{stg} | -55 to +150 | °C | |
| Allowable power dissipation | P _D | 600 | mW | |

*¹ V_{IN}, V_{OUT} and V_{OD} must not exceed V_{DD} + 0.3V.

*² V_{FDP} and V_{OD} must not exceed V_{DD} - 40V.

*³ Specifies output current of general-purpose I/O ports.

*⁴ The large current drive transistor is the N-CH transistor of Port C (PC).

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions

(V_{SS} = 0V reference)

| Item | Symbol | Min. | Max. | Unit | Remarks |
|--------------------------|-------------------|-----------------------|-----------------------|------|---|
| Supply voltage | V _{DD} | 4.5 | 5.5 | V | Guaranteed operation range during 1/2 and 1/4 frequency dividing operation mode |
| | | 3.5 | 5.5 | V | During 1/16 frequency dividing operation mode or sleep mode |
| | | 2.7 | 5.5 | V | Guaranteed operation range with TEX clock |
| | | 2.5 | 5.5 | V | Guaranteed data hold range during stop |
| High level input voltage | V _{IH} | 0.7V _{DD} | V _{DD} | V | *1 |
| | V _{IHS} | 0.8V _{DD} | V _{DD} | V | *2 |
| | V _{IHH} | 0.7V _{DD} | V _{DD} | V | *3 |
| | V _{IHEX} | V _{DD} - 0.4 | V _{DD} + 0.3 | V | EXTAL *4 |
| Low level input voltage | V _{IL} | 0 | 0.3V _{DD} | V | *1 |
| | V _{ILS} | 0 | 0.2V _{DD} | V | *2 |
| | V _{ILH} | 0 | 0.7 | V | *3 |
| | V _{ILEX} | -0.3 | 0.4 | V | EXTAL *4 |
| Operating temperature | Topr | -20 | +75 | °C | |

*1 Value for each pin of normal input port (PA, PB0, PB4, PB7, PC).

*2 Value of the following pins: $\overline{\text{RST}}$, $\overline{\text{CINT}}$, $\overline{\text{CS0/TxD}}$, $\overline{\text{RxD}}$, $\overline{\text{SI0}}$, $\overline{\text{SI1}}$, $\overline{\text{SCK0}}$, $\overline{\text{SCK1}}$, $\overline{\text{EC0/INT0}}$, $\overline{\text{EC1/INT1}}$, $\overline{\text{INT2}}$, $\overline{\text{INT3/NMI}}$, $\overline{\text{RMC}}$.

*3 Value of the following pins: PD, PF.

*4 Specifies only during external clock input.

Electrical Characteristics

DC Characteristics

(Ta = -20 to +75°C, Vss = 0V reference)

| Item | Symbol | Pins | Conditions | Min. | Typ. | Max. | Unit |
|---|------------------|---|---|------|------|------|------|
| High level output voltage | V _{OH} | PA to PD, PE6, PE7, PF to PH | V _{DD} = 4.5V, I _{OH} = -0.5mA | 4.0 | | | V |
| | | | V _{DD} = 4.5V, I _{OH} = -1.2mA | 3.5 | | | V |
| Low level output voltage | V _{OL} | PA to PC, PE6, PE7 | V _{DD} = 4.5V, I _{OL} = 1.8mA | | | 0.4 | V |
| | | | V _{DD} = 4.5V, I _{OL} = 3.6mA | | | 0.6 | V |
| | | PC | V _{DD} = 4.5V, I _{OL} = 12.0mA | | | 1.5 | V |
| Input current | I _{IHE} | EXTAL | V _{DD} = 5.5V, V _{IH} = 5.5V | 0.5 | | 40 | μA |
| | I _{ILE} | | V _{DD} = 5.5V, V _{IL} = 0.4V | -0.5 | | -40 | μA |
| | I _{IHT} | TEX | V _{DD} = 5.5V, V _{IL} = 5.5V | 0.1 | | 10 | μA |
| | I _{ILT} | | V _{DD} = 5.5V, V _{IL} = 0.4V | -0.1 | | -10 | μA |
| | I _{ILR} | $\overline{\text{RST}}^{*1}$ | V _{DD} = 5.5V, V _{IL} = 0.4V | -1.5 | | -400 | μA |
| | I _{IL} | PA to PC* ² | | | | -50 | μA |
| | | | V _{DD} = 4.5V, V _{IL} = 4.0V | -3.3 | | | μA |
| Display output current | I _{OH} | A20 to A55 | | -8 | | | mA |
| | | G0/A0 to G15/A15 A16 to A19 | V _{DD} = 4.5V V _{OH} = V _{DD} - 2.5V | -30 | | | mA |
| Open drain output leakage current (P-CH Tr off state) | I _{IOL} | G0/A0 to G15/A15 A16 to A55 | V _{DD} = 5.5V V _{OL} = V _{DD} - 35V V _{FDP} = V _{DD} - 35V | | | -20 | μA |
| Pull-down resistor* ³ | R _L | G0/A0 to G15/A15 A16 to A55 | V _{DD} = 5V V _{OD} - V _{FDP} = 30V | 30 | 70 | 220 | kΩ |
| I/O leakage current | I _{Iz} | PA to PC* ² , PD* ⁴ , PE0 to PE5, PF* ⁴ , PI, $\overline{\text{RST}}^{*1}$ | V _{DD} = 5.5V V _I = 0, 5.5V | | | ±10 | μA |

| Item | Symbol | Pins | Conditions | Min. | Typ. | Max. | Unit |
|------------------------|---|---|--|------|------|------|------|
| Power supply current*5 | I _{DD1} | V _{DD} | 1/2 frequency dividing operation mode | | 23 | 50 | mA |
| | | | V _{DD} = 5.5V, 16MHz crystal oscillation (C ₁ = C ₂ = 15pF) | | | | |
| | I _{DD2} | | V _{DD} = 3V, 32kHz crystal oscillation (C ₁ = C ₂ = 47pF) | | 30 | 100 | μA |
| | I _{DDS1} | | Sleep mode | | 1.2 | 8 | mA |
| | | | V _{DD} = 5.5V, 16MHz crystal oscillation (C ₁ = C ₂ = 15pF) | | | | |
| | I _{DDS2} | | V _{DD} = 3V, 32kHz crystal oscillation (C ₁ = C ₂ = 47pF) | | 12 | 30 | μA |
| I _{DDS3} | Stop mode V _{DD} = 5.5V, termination of 16MHz and 32kHz crystal oscillation | | | | 10 | μA | |
| Input capacity | C _{IN} | PA to PC, PD*4, PE0 to PE5, PF*4, PI, EXTAL, TEX, $\overline{\text{RST}}$ | Clock 1MHz 0V for all pins excluding measured pins | | 10 | 20 | pF |

*1 $\overline{\text{RST}}$ specifies the input current when pull-up resistor has been selected; leakage current when no resistor has been selected.

*2 PA to PC pins specify the input current when pull-up resistor has been selected; leakage current when no resistor has been selected.

*3 When incorporated pull-down resistor has been selected through mask option.

*4 PD and PF pins are used as inputs by program. They specify pull-down resistor when no resistor has been selected by mask option.

*5 When all pins are open.

AC Characteristics

(1) Clock timing

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V reference)

| Item | Symbol | Pin | Conditions | Min. | Typ. | Max. | Unit |
|--|------------|---------------|---|-------------|--------|------|------|
| System clock frequency | fc | XTAL EXTAL | Fig. 1, Fig. 2 | 1 | | 16 | MHz |
| System clock input pulse width | tXL tXH | EXTAL | Fig. 1, Fig. 2 External clock drive | 28 | | | ns |
| System clock input rise time, fall time | tCR tCF | EXTAL | Fig. 1, Fig. 2 External clock drive | tsys + 50*1 | | 200 | ns |
| Event count input clock pulse width | tEH tEL | EC0, EC1 | Fig. 3 | | | | ns |
| Event count input clock rise time, fall time | tER tEF | EC0, EC1 | Fig. 3 | | | 20 | ms |
| System clock frequency | fc | TEX TX | VDD = 2.7 to 5.5V Fig. 2 (32kHz clock applied condition) | | 32.768 | | kHz |
| Event count input pulse width | tTL tTH | TEX | Fig. 3 | 10 | | | μs |
| Event count input rise time, fall time | tTR tTF | TEX | Fig. 3 | | | 20 | ms |

*1 tsys indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (CLC: 00FEh).

tsys [ns] = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

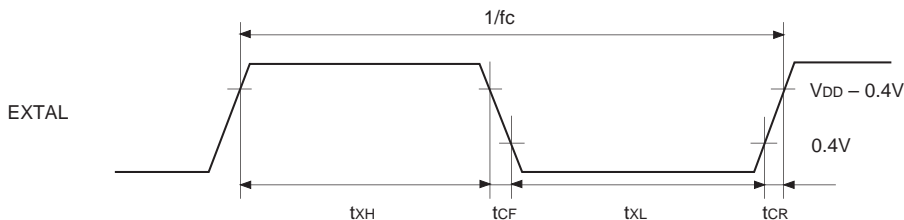


Fig. 1. Clock timing

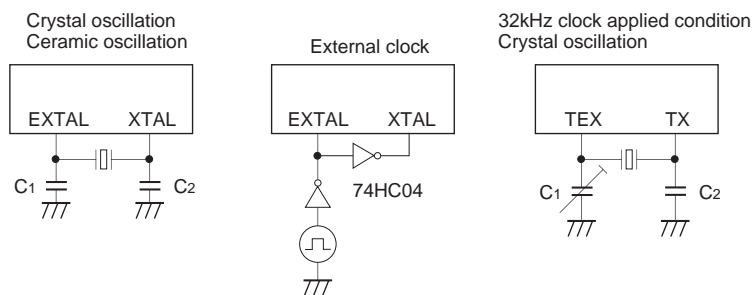


Fig. 2. Clock applied conditions

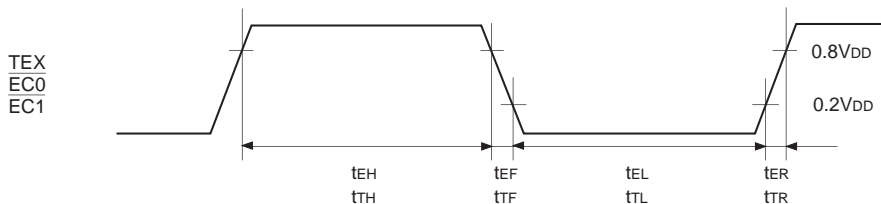


Fig. 3. Event count clock timing

(2) Serial transfer (CH0)

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, Vss = 0V reference)

| Item | Symbol | Pin | Conditions | Min. | Max. | Unit |
|---------------------------------------|------------------------------------|------|---|-------------------------|------------------------|------|
| CS0 ↓ → SCK0 delay time | t _{DCSK} | SCK0 | Chip select transfer mode (SCK0 = output mode) | | t _{sys} + 200 | ns |
| CS0 ↑ → SCK0 float delay time | t _{DCSKF} | SCK0 | Chip select transfer mode (SCK0 = output mode) | | t _{sys} + 200 | ns |
| CS0 ↓ → SO0 delay time | t _{DCSO} | SO0 | Chip select transfer mode | | t _{sys} + 200 | ns |
| CS0 ↑ → SO0 float delay time | t _{DCSOF} | SO0 | Chip select transfer mode | | t _{sys} + 200 | ns |
| CS0 High level width | t _{WHCS} | CS0 | Chip select transfer mode | t _{sys} + 200 | | ns |
| SCK0 cycle time | t _{KCY} | SCK0 | Input mode | 2t _{sys} + 200 | | ns |
| | | | Output mode | 16000/fc | | ns |
| SCK0 High, Low level width | t _{KH} t _{KL} | SCK0 | Input mode | t _{sys} + 100 | | ns |
| | | | Output mode | 8000/fc - 50 | | ns |
| SI0 input set-up time (for SCK0 ↑) | t _{SIK} | SI0 | SCK0 input mode | 100 | | ns |
| | | | SCK0 output mode | 200 | | ns |
| SI0 input hold time (for SCK0 ↑) | t _{KSI} | SI0 | SCK0 input mode | t _{sys} + 200 | | ns |
| | | | SCK0 output mode | 100 | | ns |
| SCK0 ↓ → SO0 delay time | t _{KSO} | SO0 | SCK0 input mode | | t _{sys} + 200 | ns |
| | | | SCK0 output mode | | 100 | ns |

Note 1) t_{sys} indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (CLC: 00FEh).

t_{sys} [ns] = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

Note 2) The load condition for the SCK0 output mode, SO0 output delay time is 50pF + 1TTL.

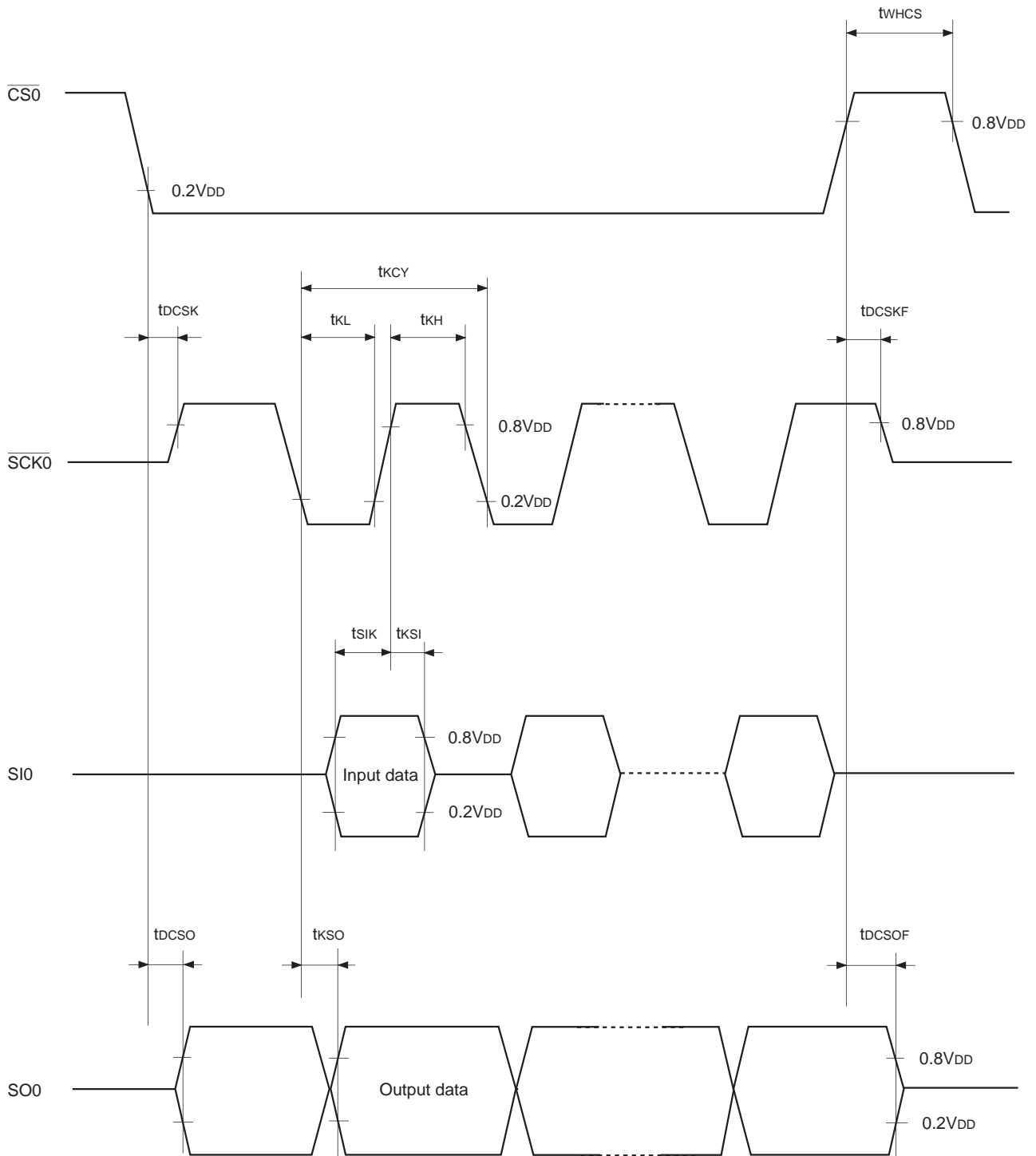


Fig. 4. Serial transfer CH0 timing

Serial transfer (CH1)

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

| Item | Symbol | Pin | Condition | Min. | Max. | Unit |
|--|----------------------|------|-----------------|-----------------|------|------|
| SCK1 cycle time | t_{kCY} | SCK1 | Input mode | 1000 | | ns |
| | | | Ouput mode | $16000/f_c$ | | ns |
| SCK1 High, Low level width | t_{kH} t_{kL} | SCK1 | Input mode | 400 | | ns |
| | | | Ouput mode | $8000/f_c - 50$ | | ns |
| SI1 input set-up time (for SCK1 \uparrow) | t_{sIK} | SI1 | SCK1 input mode | 100 | | ns |
| | | | SCK1 ouput mode | 200 | | ns |
| SI1 input hold time (for SCK1 \uparrow) | t_{kSI} | SI1 | SCK1 input mode | 200 | | ns |
| | | | SCK1 ouput mode | 100 | | ns |
| SCK1 $\downarrow \rightarrow$ SO1 delay time | t_{kSO} | SO1 | SCK1 input mode | | 200 | ns |
| | | | SCK1 ouput mode | | 100 | ns |

Note) The load condition for the SCK1 output mode, SO1 output delay time is $50\text{pF} + 1\text{TTL}$.

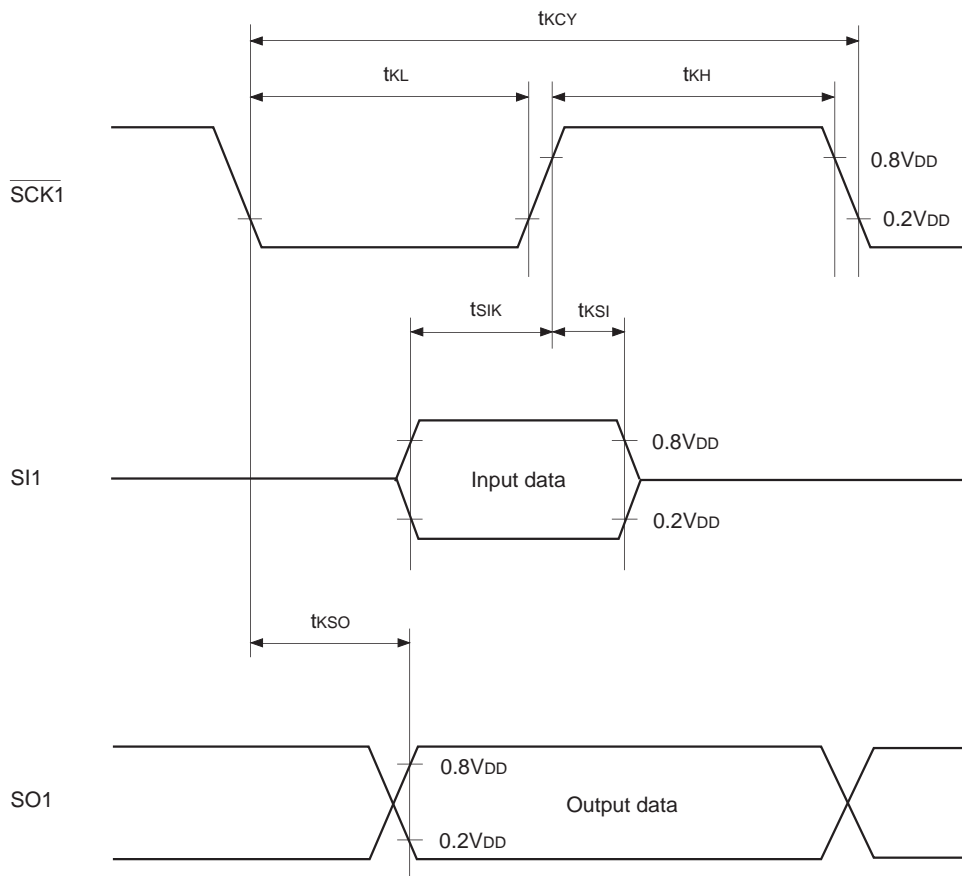
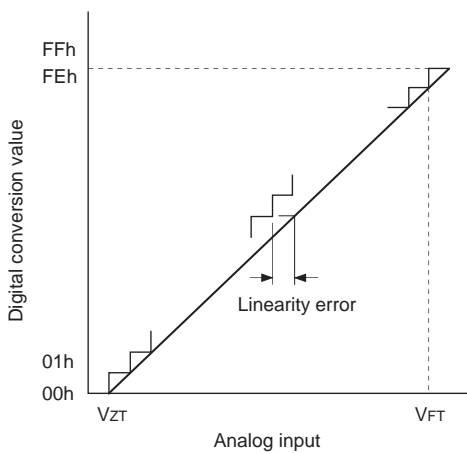


Fig. 5. Serial transfer CH1 timing

(3) A/D converter characteristics

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V reference)

| Item | Symbol | Pin | Condition | Min. | Typ. | Max. | Unit |
|-------------------------------|--------|------------|-------------------------------------|-----------|------|------|------|
| Resolution | | | | | | 8 | Bits |
| Linearity error | | | | | | ±3 | LSB |
| Zero transition voltage | VZT*1 | | Ta = 25°C VDD = 5.0V VSS = 0V | -10 | 10 | 70 | mV |
| Full-scale transition voltage | VFT*2 | | | 4910 | 4970 | 5030 | mV |
| Conversion time | tCONV | | | 26/fADC*3 | | | µs |
| Sampling time | tSAMP | | | 6/fADC*3 | | | µs |
| Analog input voltage | VIAN | AN0 to AN7 | | 0 | | VDD | V |



- *1 VZT: Value at which the digital conversion value changes from 00h to 01h and vice versa.
- *2 VFT: Value at which the digital conversion value changes from FEh to FFh and vice versa.
- *3 fADC indicates the below values due to the contents of bit 6 (CKS) of the A/D control register (ADC: 00F9h) and bits 7 (PCK1) and 6 (PCK0) of the clock control register (CLC: 00FEh).
 $f_{ADC} = f_c$ (CKS = "0"), $f_c/2$ (CKS = "1")
 However, the selection for $f_{ADC} = f_c$ (CKS = "0") is limited in the clock range of $f_c = 1$ to 14MHz (VDD = 4.5 to 5.5V).

Fig. 6. Definition of A/D converter terms

(4) Interruption, reset input (Ta = -20 to +75°C, VDD = 4.5 to 5.5V, Vss = 0V reference)

| Item | Symbol | Pin | Condition | Min. | Max. | Unit |
|--|------------------------------------|--|-----------|-------|------|------|
| External interruption High, Low level width | t _{IH} t _{IL} | INT0 INT1 INT2 $\overline{\text{NMI/INT3}}$ | | 1 | | μs |
| Reset input Low level width | t _{RSL} | $\overline{\text{RST}}$ | | 32/fc | | μs |

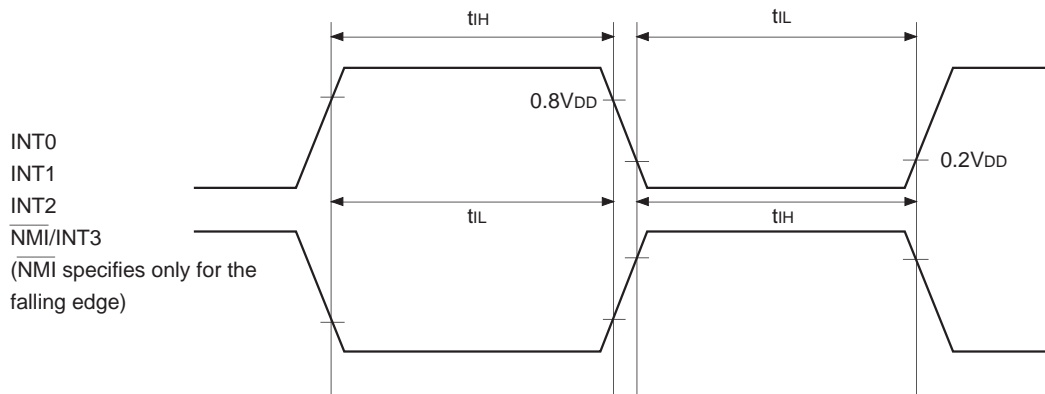


Fig. 7. Interruption input timing

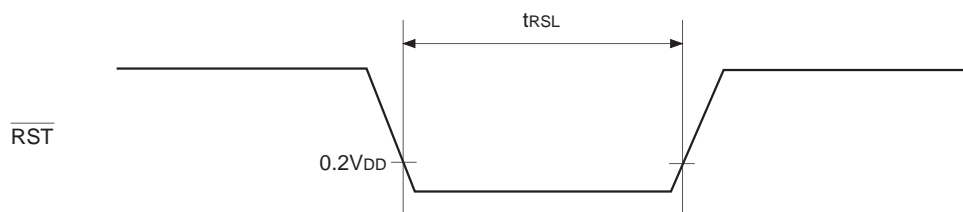


Fig. 8. $\overline{\text{RST}}$ input timing

Appendix

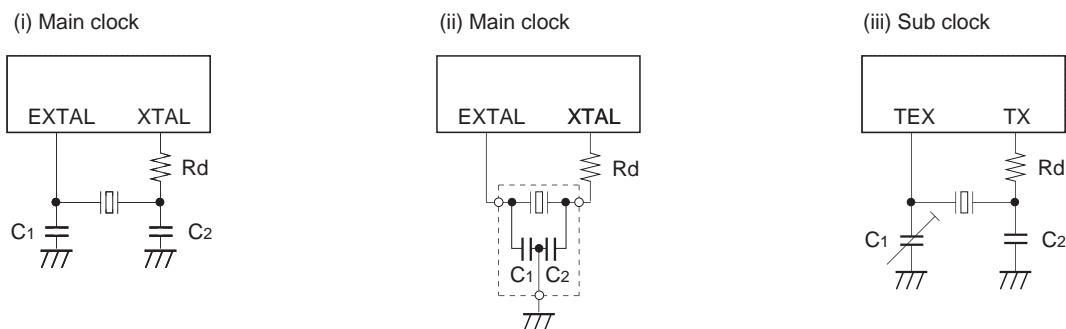


Fig. 9. Recommended oscillation circuit

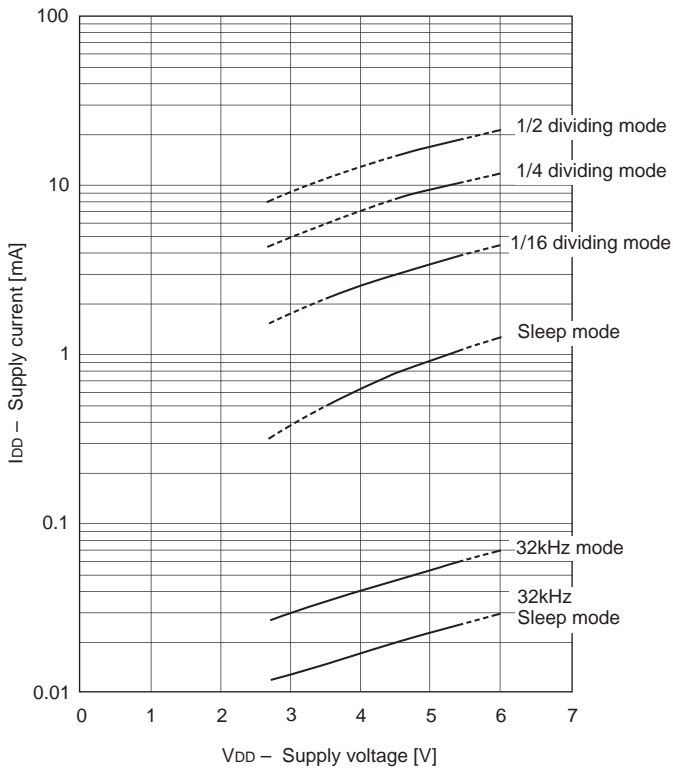
| Manufacturer | Model | fc (MHz) | C1 (pF) | C2 (pF) | Rd (Ω) | Circuit example | Remarks |
|------------------------|-----------------|-----------|---------|---------|--------|-----------------|-------------|
| MURATA MFG CO., LTD. | CSA10.0MTZ | 10.0 | 30 | 30 | 0 | (i) | |
| | CSA12.0MTZ | 12.0 | | | | | |
| | CSA16.00MXZ040 | 16.0 | 5 | 5 | | | |
| | CST10.0MTW* | 10.0 | 30 | 30 | | (ii) | |
| | CST12.0MTW* | 12.0 | | | | | |
| | CST16.00MXW0C1* | 16.0 | 5 | 5 | | | |
| RIVER ELETEC CO., LTD | HC-49/U03 | 8.0 | 18 | 18 | 330 | (i) | |
| | | 12.0 | 12 | 12 | | | |
| | | 16.0 | 10 | 10 | | | |
| KINSEKI LTD. | HC-49/U (-S) | 8.0 | 10 | 10 | 0 | | |
| | | 12.0 | 5 | 5 | | | |
| | | 16.0 | Open | Open | | | |
| Seiko Instruments Inc. | VTC-200 SP-T | 32.768kHz | 18 | 18 | 330k | (iii) | CL = 12.5pF |

Models marked with an asterisk (*) have the built-in ground capacitance (C1, C2).

Characteristics Curve

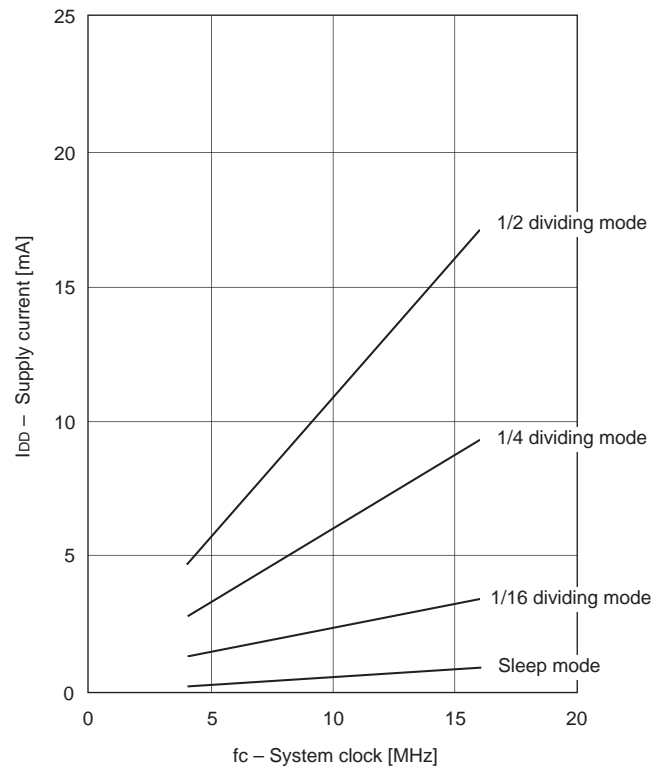
I_{DD} vs. V_{DD}

(T_a = 25°C, Typical)



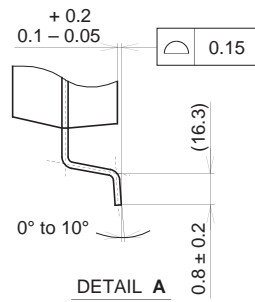
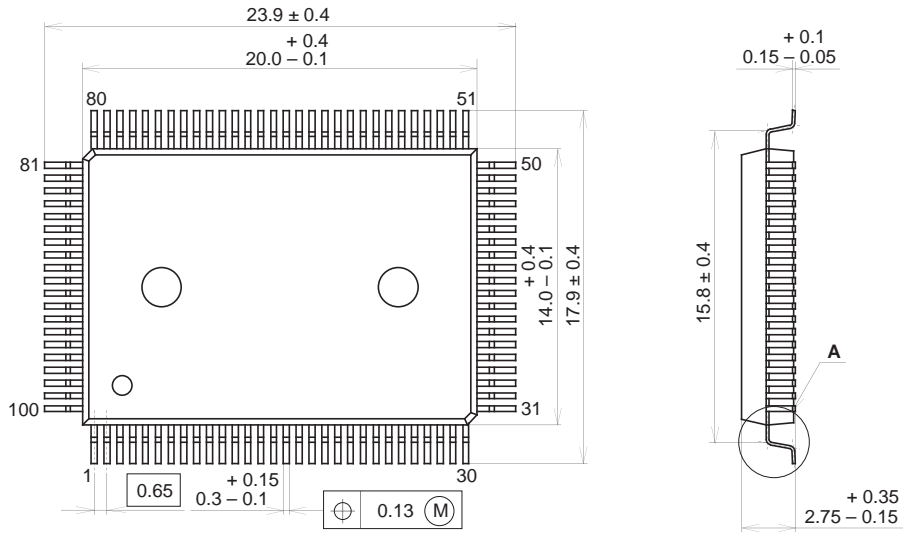
I_{DD} vs. f_c

(V_{DD} = 5V, T_a = 25°C, Typical)



Package Outline Unit: mm

100PIN QFP (PLASTIC)



| | |
|------------|---------------|
| SONY CODE | QFP-100P-L01 |
| EIAJ CODE | QFP100-P-1420 |
| JEDEC CODE | _____ |

PACKAGE STRUCTURE

| | |
|------------------|-----------------|
| PACKAGE MATERIAL | EPOXY RESIN |
| LEAD TREATMENT | SOLDER PLATING |
| LEAD MATERIAL | 42/COPPER ALLOY |
| PACKAGE MASS | 1.7g |