General Semiconductor Industries, Inc.
SQUARE D COMPANY

2N6922, 2N6922A
2N6923, 2N6923A
2N6926, 2N6926A
2N6927, 2N6927A

T-33-13

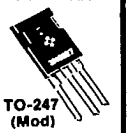
HIGH POWER NPN Switch Plus®III TRANSISTORS

These NPN silicon transistors offer an unprecedented combination of speed and ruggedness for use in high speed switching systems. This unique series also features General Semiconductor Industries' planar C^2R manufacturing process to provide surface stabilization for high voltage operation and to enhance long term reliablity.

- **Off-line Power Supplies**
- **Inverters/Converters**
- **Switching Amplifiers**
- **Switching Regulators**

TO-204AA — 2N6922 (A), 23 (A)
TO-247 — 2N6926 (A), 27 (A)


TO-204AA


TO-247 (Mod)

NPN
UP TO 850V V_{CEV}
UP TO 500V INDUCTIVE SWITCHING
At Rated Current
20A I_C (MAX)
15A SWITCHING
35ns t_c TYPICAL

Switch Plus®III

***MAXIMUM RATINGS** (T_C = 25°C unless otherwise noted.)

SYMBOL	DESCRIPTION	2N6922/A	2N6923/A	2N6926/A	2N6927/A	UNIT
V_{CEV}	Collector-Emitter Voltage, Blocking	550/850	550/850	550/850	550/850	Volts
$V_{CEX(sus)}$	Collector-Emitter Voltage, Inductive Switching	450	500	450	500	Volts
$V_{CEO(sus)}$	Collector-Emitter Voltage, Sustaining	400	450	400	450	Volts
V_{EBO}	Emitter Base Voltage	8.0		8.0		Volts
I_C	Collector Current—Continuous/Peak	20/30		20/30		Amps
I_E	Emitter Current—Continuous/Peak	30/40		30/40		Amps
I_B	Base Current—Continuous/Peak	10/15		10/15		Amps
P_D	Total Power Dissipation @ T_C = 25°C	220		125		Watts
$T_{J(oper)}$ T_{stg}	Operating and Storage Junction Temperature Range	- 65 to +200		-55 to +150		°C

***ELECTRICAL CHARACTERISTICS** (Applies to all types unless otherwise noted.)

			T_C = 25°C		T_C = 100°C		
SYMBOL	CONDITIONS	PART NO/NOTES	MIN.	MAX.	MIN.	MAX.	UNIT
OFF-STATE							
$V_{CEO(sus)}$	I_C = 50mA	2N6922, 6 (A) 2N6923, 7 (A)	400 450				Volts
I_{CEV}	V_{CE} = Rated V_{CEV}, V_{EB} = 1.5V			1.0			mA
I_{CEV}	V_{CE} = 0.8 Rated V_{CEV}, V_{EB} = 1.5V			10		100	μA
I_{EBO}	V_{EB} = 8.0V			1.0			mA
ON-STATE							
h_{FE}	I_C = 15A, V_{CE} = 2.0V	Pulsed: Notes 1 & 2	8.0				
$V_{CE(sat)}$	I_C = 15A, I_B = 3.0A			1.0		1.5	Volts
$V_{CE(sat)}$	I_C = 20A, I_B = 5.0A			2.0			Volts
$V_{CE(sat)}$	I_C = 30A, I_B = 10A	Pulsed: Notes 1 & 3		5.0			Volts
$V_{BE(sat)}$	I_C = 15A, I_B = 3.0A	Pulsed: Notes 1 & 2		1.5			Volts
DYNAMIC							
f_T	V_{CE} = 10V, I_C = 1.0A, f = 10MHz	Pulsed: Note 2	15	50			MHz
C_{obo}	V_{CB} = 10V, f = 1.0MHz		200	500			pF
t_d	I_C = 15A, I_{B1} = 3.0A — **Resistive Load** $V_{CC} = V_{CEX(sus)}$			20			ns
t_r				50			ns
t_{sd} (t_f)	**Current Source Load**	Measured to 10V		1.0		3.0	μs
t_{sv}	**Inductive Load**			1.0		1.5	μs
t_{rv}	I_C = 15A, I_{B1} = 3.0A, I_{B2} = 6.0A, t_p = 30μsec, L = 100μH, $V_{CLAMP} = V_{CEX(sus)}$			30		40	ns
t_{fi}				30		40	ns
t_c				50		70	ns
THERMAL							
$R_{\theta JC}$	V_{CE} = 10V, I_C = 10A	2N6922, 3 (A)		0.8			°C/W
$R_{\theta JC}$	V_{CE} = 10V, I_C = 5.0A	2N6926, 7 (A)		1.0			°C/W

Notes: 1) Measured using Kelvin connections.
2) Pulse measurement conditions: Length = 300μs. Duty cycle < 2%.
3) Pulse measurement conditions: Length = 10μs. Duty cycle < 2%.

*JEDEC registered data.

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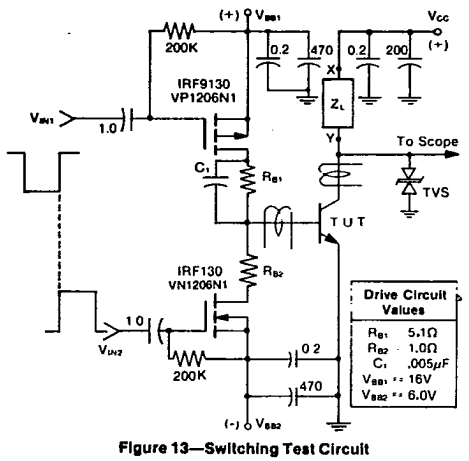

Figure 13—Switching Test Circuit

Load Circuit Values				
Test	$V_{CE(PK)}$	V_{CC}	Z_L	TVS
Resistive				
2N6922, 6	—	450V	30Ω	—
2N6923, 7	—	500V	33Ω	—
Inductive				
2N6922, 6	450V	50V	100μH	2 - SA160CA
2N6923, 7	500V	50V	100μH	2 - SA170CA
Dynamic Saturation	—	50V	Fig. 14	—

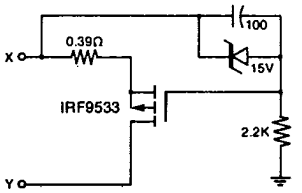

Figure 14—Current Source Load (Z_L)

Notes:

1. Capacitance values in μFd.
2. For inductive switching, the Transient Voltage Suppressor (TVS) diode is selected to allow $V_{CE(PK)}$ to equal rated $V_{CEX(sus)}$. Since some overshoot caused by circuit inductance and TVS heating is inevitable, the specified TVS breakdown voltage will be about 100 volts less than $V_{CEX(sus)}$. Correct voltage may be achieved by stacking TVS diodes and by making minor adjustments in the duty cycle.
3. For resistive switching, R_L is composed of a stack of 2W carbon resistors which may need to be trimmed to obtain the correct I_C. For inductive switching, $I_C \approx T_{ON} V_{CC}/L$. V_{CC} may need minor adjustment to obtain correct I_C. Duty cycle ≤ 1%.
4. Proper circuit performance is only achieved by a circuit layout which minimizes lead inductance. The emitter of the T.U.T. must be the ground focal point. To minimize stray coupling, a double sided heavy foil P.C.B. is suggested for the driver stage.
5. View the voltage across power supply lines and adjust bypassing so that ringing is a small percentage of signal levels. Sprague Extralytic ® and metalized stacked film capacitors are used for supply bypassing.
6. Base current should be viewed with a current probe. C_1 is chosen to achieve an essentially flat topped current pulse. V_{BB1} and V_{BB2} are adjusted to obtain correct values for the base currents, I_{B1} and I_{B2}.
7. Ground loops through the scope and pulse generator must be avoided. A differential amplifier scope input is often the best solution when a ground loop is encountered.

*Registered trademark of Sprague Electric Co.

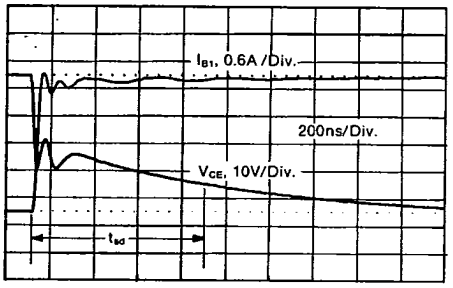

Figure 15—Dynamic Saturation Waveforms

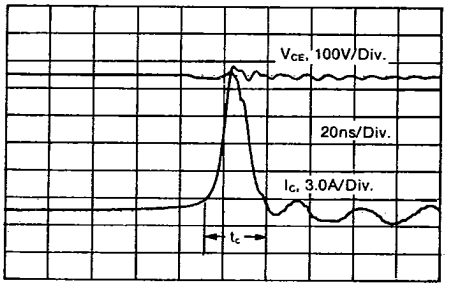

Figure 16—Crossover Waveforms

Digitized Waveforms

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NPN SWITCHING TRANSISTORS

INDUCTIVE TURN-OFF CHARACTERISTICS

CROSSOVER TIME

Figure 7—Effect of Collector Current Proportional Drive

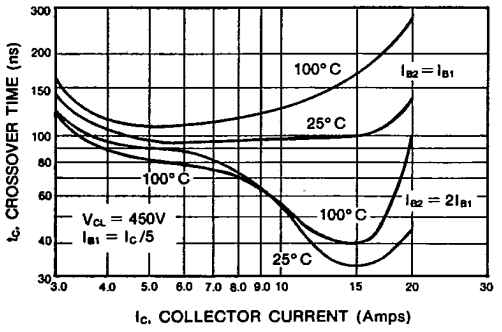


Figure 9—Effect of Collector Current Fixed Drive

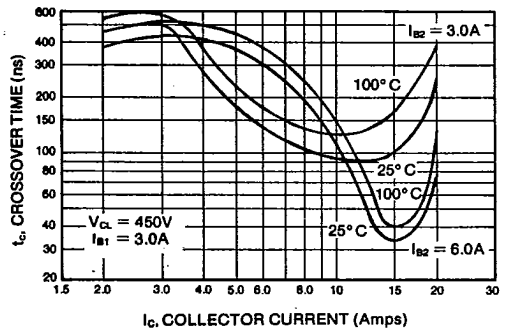
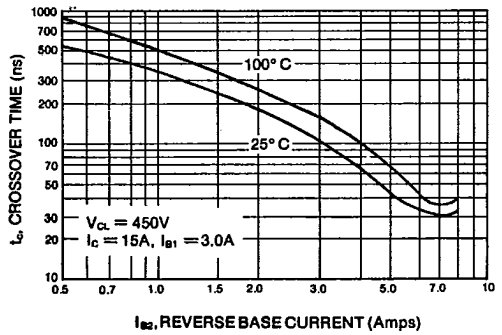


Figure 11—Effect of Reverse Drive



CURRENT FALL TIME

Figure 8—Effect of Collector Current Proportional Drive

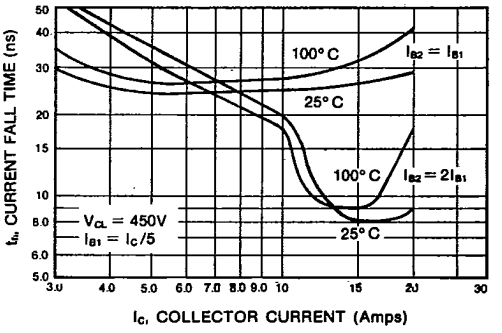


Figure 10—Effect of Collector Current Fixed Drive

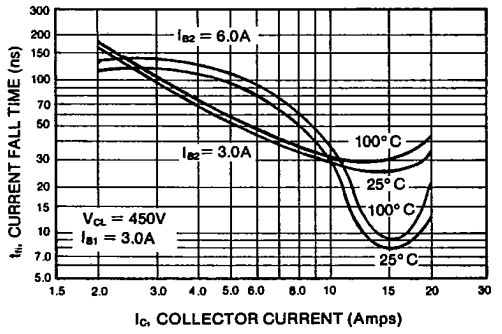
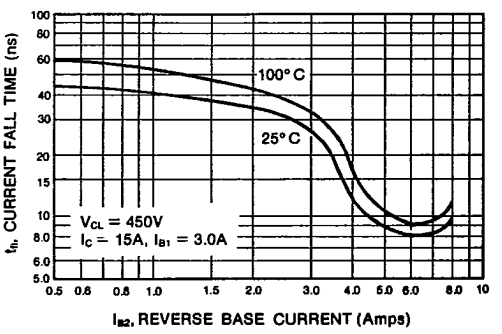


Figure 12—Effect of Reverse Drive



2N6922, 2N6922A, 2N6923, 2N6923A, 2N6926, 2N6926A, 2N6927, 2N6927A

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TURN ON TIME

Figure 1—Rise Time

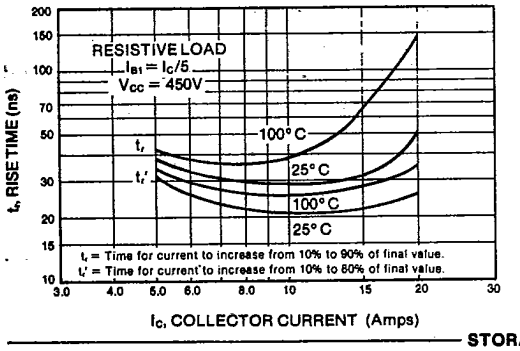
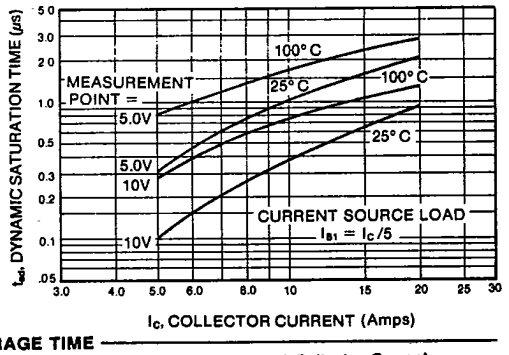


Figure 2—Dynamic Saturation Time



STORAGE TIME

Figure 3—Effect of Collector Current Proportional Drive

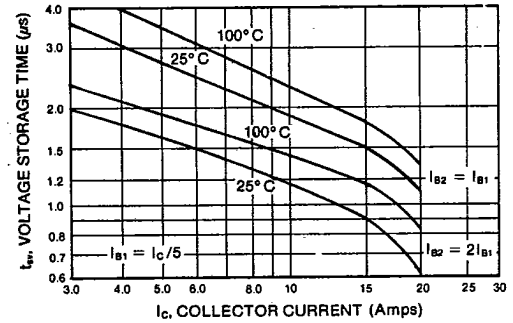


Figure 4—Effect of Collector Current Fixed Drive

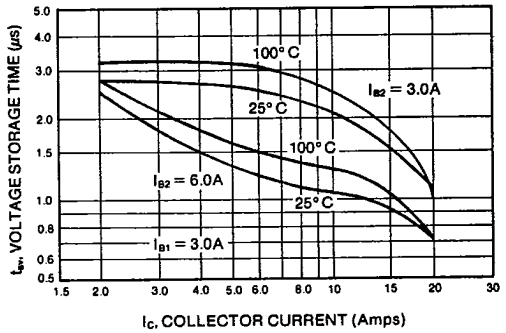


Figure 5—Effect of Pulse Width

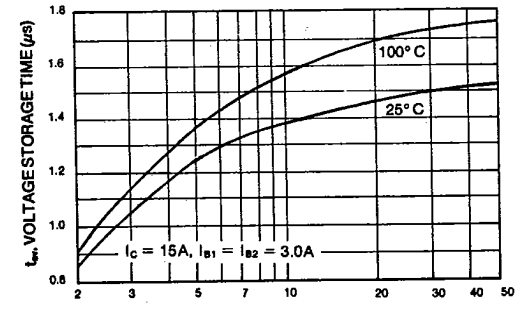
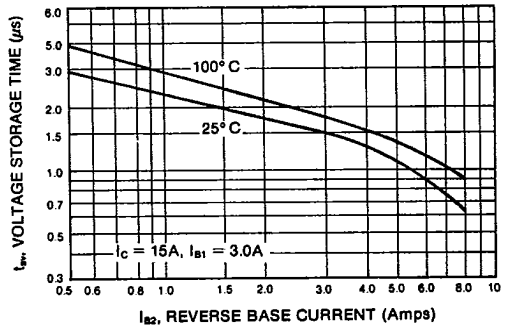


Figure 6—Effect of Reverse Drive



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NPN SWITCHING TRANSISTORS

2N6922, 2N6922A, 2N6923, 2N6923A, 2N6926, 2N6926A, 2N6927, 2N6927A

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TYPICAL DC CHARACTERISTICS & RATINGS

Figure 17—DC Current Gain

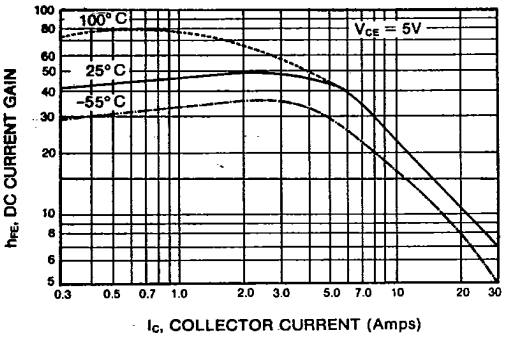


Figure 18—Forward Biased Safe Operating Area

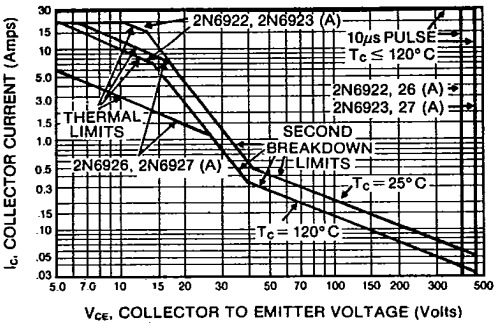


Figure 19—Saturation Voltage

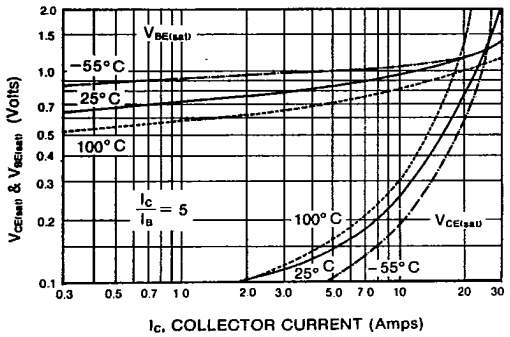


Figure 20—Power Derating

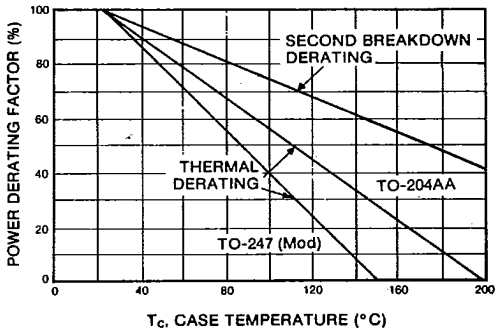


Figure 21—Saturation Region

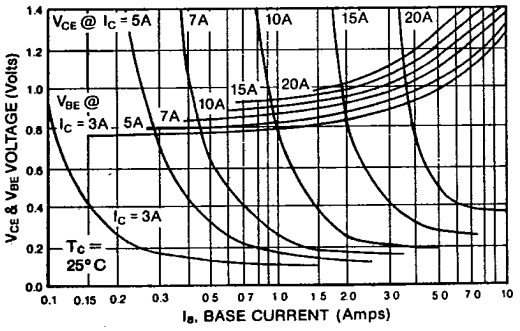
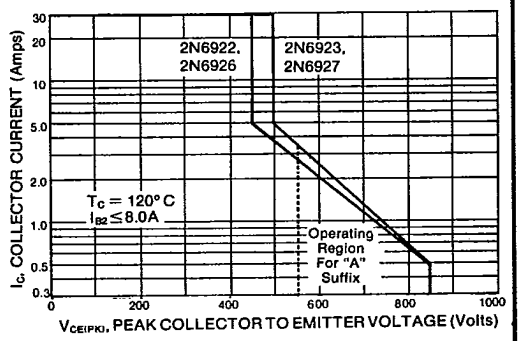


Figure 22—Reverse Bias Safe Operating Area



2N6922, 2N6922A, 2N6923, 2N6923A, 2N6926, 2N6926A, 2N6927, 2N6927A

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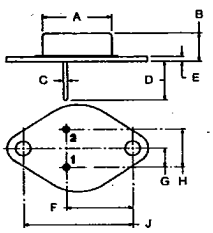
Package Outline TO-204AA

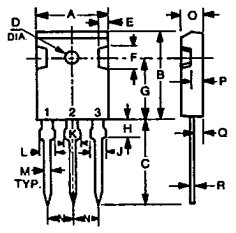


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	—	.875	—	22.23
B	.250	.450	6.35	11.43
C	.038	.043	.97	1.09
D	.312	—	7.92	—
E	—	.135	—	3.43
F	.655	.675	16.64	17.15
G	.205	.225	5.21	5.72
H	.420	.440	10.67	11.18
J	1.177	1.197	29.90	30.40

Pin 1 Base
2 Emitter
Case Collector

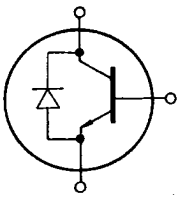
(FORMERLY TO-3)

Package Outline TO-247



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	—	0.669	—	17.00
B	—	0.866	—	22.00
C	0.748	—	19.00	—
D	0.122	0.138	3.10	3.50
E	0.087 TYP.		2.20 TYP.	
F	0.217 TYP.		5.50 TYP.	
G	0.583	0.598	14.80	15.20
H	—	0.177	—	4.50
J	—	0.098	—	2.50
K	—	0.138	—	3.50
L	—	0.098	—	2.50
M	0.039	0.055	1.00	1.40
N	0.207	0.222	5.25	5.65
O	0.185	0.209	4.70	5.30
P	0.079 TYP.		2.00 TYP.	
Q	0.063	0.106	2.10	2.70
R	0.018	0.033	0.45	0.85

Pin 1, Base; Pin 2, Collector; Pin 3, Emitter.



Note:
The technology utilized to produce these devices results in an internal diode between the collector and emitter. In some cases this may eliminate the need for an external diode to clamp inductive loads. At 20 A, t_{rr} = 600 ns and V_F = 1.25V (typical).

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NPN SWITCHING TRANSISTORS