PM5362

TUPP-PLUS

SONET/SDH TRIBUTARY UNIT PAYLOAD PROCESSOR / PERFORMANCE MONITOR

DATA SHEET ERRATA

ISSUE 4: NOVEMBER 2000

REVISION HISTORY

Issue No.	Issue Date	Details of Change
1	May 1999	This document contains changes to the data sheet revision 6 and details device errata.
2	September 1999	This document describes new functional errata and recommendations applicable to Revision B of the device.
3	October 2000	Aligns with Revision C of the device. Removed the following functional errata from issue 2: Device May Corrupt Data After Reset, Device May Fail to Detect FIFO Over-or-Underflow Condition and Device May Fail to Recover From FIFO Over-or-Underflow Condition. Added datasheet discrepancies 2.2-2.3: ITMF Pulse Ignorance Error and Device ID Revision Number. Added new functional errata 3.1: Outgoing V1 in Locked Mode Not Aligned to H4 Marker on OTMF Pin.
4	November 2000	Aligns with Revision C of the device. Added datasheet discrepancies 2.4-2.5: IDDOP1 and IDDOP2 Max Parameters; TU3 In-band Error Report.

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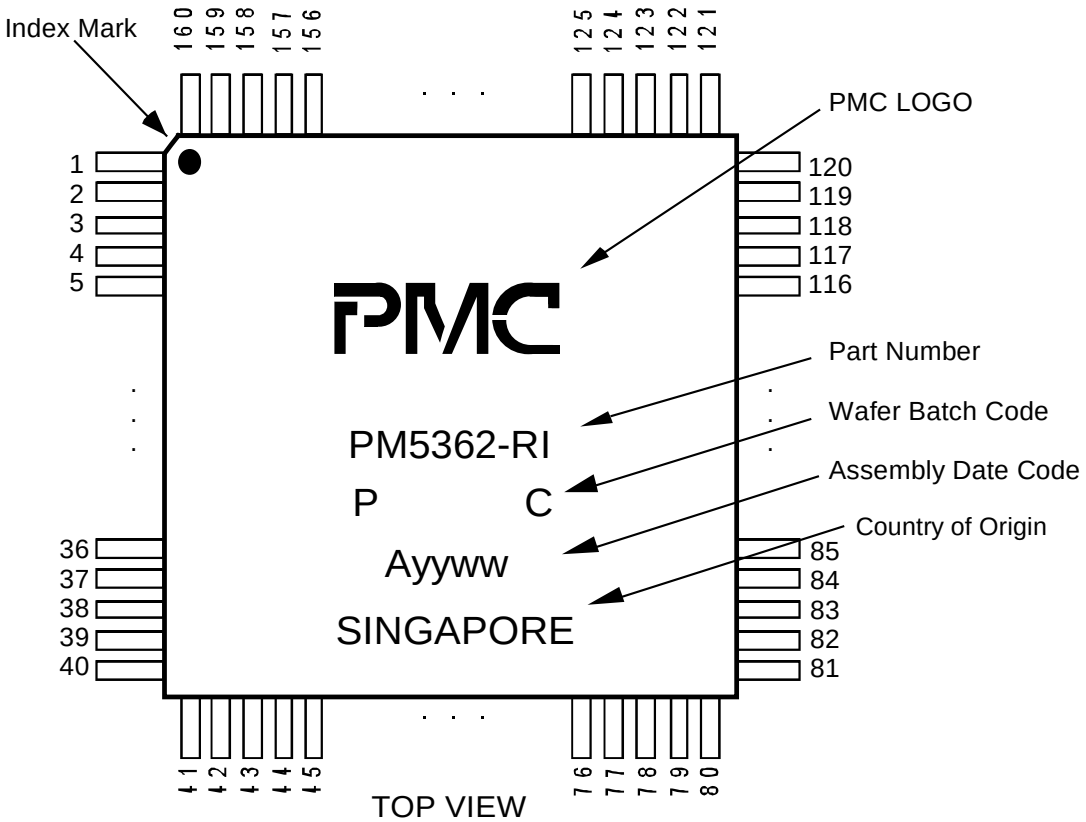
1 ISSUE 4 ERRATA

This Issue 4 Errata notifies that changes have been made to Issue 6 of the PMC-1951010 data sheet. It describes datasheet and functional discrepancies in Revision C of TUPP-PLUS, and provides a summary of recommended workarounds.

The Issue 6 Datasheet and Issue 4 Errata supersede all prior editions and versions.

1.1 Device Identification

The information in this document applies only to the PM5362 TUPP-PLUS Revision C device. The device revision is marked at the end of the wafer batch code on the face of the device.



2 DATASHEET DISCREPANCIES

Legend

1. unaltered text is unchanged to add context to changes

2. new material is bold and italicized

~~3. obsolete material is struck out~~

4. comments specific to this document are in italics

5. A vertical bar on the right margin indicates that this is a new item which was not present in the previous issue of this document.

NOTE: All items in Section 2 are documentation changes only.

2.1 Telecom Bus Cannot be Operated in Mixed Incoming Nibble and Outgoing Byte Mode

The TUPP PLUS does not function properly in mixed incoming nibble and outgoing byte mode.

Therefore, IBMODE (pin 145, page 13) may not be set low when OBMODE (pin 146, page 14) is set high. All other combinations of IBMODE and OBMODE are allowed: IBMODE low and OBMODE low, IBMODE high and OBMODE high, or IBMODE high and OBMODE low.

This device problem will not be fixed in the PM5262 TUPP Plus.

In the device datasheet, the description on page 13 should read:

Pin name	Type	Pin	Function
IBMODE	Input	145	The incoming byte interface mode signal (IBMODE) configures the incoming interface mode of the TUPP-PLUS. When IBMODE is set low, nibble interface mode is selected. SCLK must be connected to GSCLK[0]. IC1J1, IPL, ITMF, IDP, ID[3:0] are sampled on the rising edge of NSCLK. When IBMODE is set high, byte interface mode is selected. IC1J1, IPL, ITMF, IDP, ID[7:0] are sampled on the rising edge of SCLK. IBMODE has an integral pull-up

			resister. ***Note: The TUPP Plus will not operate correctly when IBMODE (pin 145, incoming interface mode) is set low and OBMODE (pin 146, outgoing interface mode) is set high.***

In the device data sheet, the description on page 14 should read:

Pin name	Type	Pin	Function
OBMODE	Input	146	The outgoing byte interface mode signal (OBMODE) configures the outgoing interface mode of the TUPP-PLUS. When OBMODE is set low, nibble interface mode is selected. SCLK must be connected to GSCLK[0]. OTMF, OC1J1 and OPL are sampled on the rising edge of NSCLK. ODP, OTPL, OTV5, OD[3:0], AIS, IDLE, LC1J1V1, LPL, and LOM[3:1] are updated on the rising edge of NSCLK. When OBMODE is set high, byte interface mode is selected. OTMF, OC1J1 and OPL are sampled on the rising edge of SCLK. ODP, OTPL, OTV5, OD[7:0], AIS, IDLE, LC1J1V1, LPL, and LOM[3:1] are updated on the rising edge of SCLK. OBMODE has an integral pull-up resister. ***Note: The TUPP Plus will not operate correctly when IBMODE (pin 145, incoming interface mode) is set low and OBMODE (pin 146, outgoing interface mode) is set high.***

2.2 ITMF Pulse Ignorance Error

The following changes are made to the pin description of the ITMF pin found in page 17 of the device datasheet:

Pin Name	Type	Pin No.	Function
ITMF	Input	52	The active high incoming tributary multiframe (ITMF) signal identifies the first frame of the tributary multiframe for each STS-1 synchronous payload envelope, AU3, or AU4 administrative unit. ITMF is enabled by the setting the ITMFEN register bit high. When ITMFEN bit is low, the path overhead H4 byte is used to determine tributary multiframe boundaries. ITMF is selectable to pulse high during the third byte after J1 of the first tributary or during the H4 byte which indicates that the next frame is the first frame of the tributary multiframe. Selection between marking each H4 or the third byte after each J1 is controlled by the ITMFH4 register bit. Pulses on ITMF are only effective during the H4 or third byte after each J1 byte positions, as appropriate. ~~ITMF is ignored at other byte positions~~. ***When ITMFH4 is low, ITMF can be set high for the entire first frame of the tributary multiframe. ITMF must be low for the 2nd, 3rd, and 4th frame of the tributary multiframe. When ITMFH4 is high, ITMF can be set high for the entire fourth frame of the tributary multiframe. ITMF must be low for the 1st, 2nd and 3rd frame of the tributary multiframe.*** In incoming byte interface mode (IBMODE set high), ITMF is sampled on the rising edge of SCLK. In incoming nibble interface mode (IBMODE set low), ITMF marks the more significant nibble of H4 or the third byte after J1, as appropriate. It is ignored at the less significant nibble timeslots. ITMF is sampled on the rising edge of NSCLK.

2.3 Device ID Revision Number

The device ID revision number is changed to reflect Revision C in Register 03H as shown below:

Register 03H: Master Reset and Identity

Bit	Type	Function	Default
Bit 7	R/W	RESET	0
Bit 6	R	TYPE	1
Bit 5	R	ID[5]	0
Bit 4	R	ID[4]	0
Bit 3	R	ID[3]	0
Bit 2	R	ID[2]	0
Bit 1	R	ID[1]	~~0~~***1***
Bit 0	R	ID[0]	~~1~~***0***

2.4 IDDOP1 and IDDOP2 Max Parameters

The IDDOP1 and IDDOP2 parameters from Table 6 (TUPP PLUS DC Characteristics) of the TUPP PLUS datasheet are changed to 215mA and 100mA respectively as shown below:

Table 6 - TUPP-PLUS D.C. Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{DDOP1}	Operating Current Processing Tributaries			***215*** ~~185~~	mA	V_{DD} = 5.5 V, Outputs Unloaded, SCLK = 19.44 MHz, Alternating Data, Processing Tributaries
I_{DDOP2}	Operating Current Tributary Processing Disabled			***100*** ~~80~~	mA	V_{DD} = 5.5 V, Outputs Unloaded, SCLK = 19.44 MHz, Alternating Data, Tributary Processors Bypassed

2.5 TU3 In-band Error Report

The TUPP PLUS device does not support TU3 in-band error reporting. This feature is removed from the TUPP PLUS datasheet. Modifications pertaining to this change, including section 8.4.4 (In-band Error Report) and Register 13DH, 23DH, 33DH: RTOP, TU3 or TU #1 in TUG2 #1 to TUG2 #7, In Band Error Reporting Configuration, are shown below:

8.4.4 In-band Error Report

The in-band error report block optionally modifies the ~~G1 byte of outgoing TU3 streams or the~~ V5 byte of outgoing non-TU3 streams to report the number of detected BIP errors and tributary path alarms. In-band error reporting is enabled by the IBER register bits in the RTOP In-band Error Reporting Configuration registers.

~~When in-band error reporting is enabled for TU3 streams, bits 1 to 4 of the G1 byte is set to reflect the count of the number of BIP-8 errors detected in the previous frame. Bit 5 reports the RDI status. It is set high when the tributary path alarms named in the Tributary Remote Defect Indication Control registers is detected and the corresponding enable register bits is also set high. Similarly, bit 6 reports the auxiliary RDI status. It is set high when the tributary path alarms named in the Tributary Auxiliary Remote Defect Indication Control registers is detected and the corresponding enable register bits is also set high. Bits 7 and 8 are unmodified.~~

When in-band error reporting is enabled for non-TU3 streams, bit 3 of the V5 byte is set high when a BIP-2 error is detected in the previous multiframe. Bit 4 reports the RDI status. It is set high when the tributary path alarms named in the Tributary Remote Defect Indication Control registers is detected and the corresponding enable register bits is also set high. Similarly, bit 8 reports the auxiliary RDI status. It is set high when the tributary path alarms named in the Tributary Auxiliary Remote Defect Indication Control registers is detected and the corresponding enable register bits is also set high. Bits 1, 2, 5, 6 and 7 are unmodified.

Register 13DH, 23DH, 33DH: RTOP, ~~TU3 or~~ TU #1 in TUG2 #1 to TUG2 #7, In Band Error Reporting Configuration

Bit	Type	Function	Default
Bit 7		Unused	x
Bit 6	R/W	IBER7	0
Bit 5	R/W	IBER6	0
Bit 4	R/W	IBER5	0

Bit	Type	Function	Default
Bit 3	R/W	IBER4	0
Bit 2	R/W	IBER3	0
Bit 1	R/W	IBER2	0
Bit 0	R/W	IBER1	0

This register enables the inband error reporting mode of the tributaries TU #1 in TUG2 #1 to TUG2 #7 ~~and the IBER mode of the TU3 mode~~.

~~IBER1:~~

~~The IBER1 bit controls in band error reporting for tributary TU #1 in TUG2 #1 or TU3 in a TUG3. In TU3 mode, setting the IBER1 high causes in band error reporting information to be inserted in the G1 byte of the TU3. In non-TU3 modes, setting the IBER1 bit high causes in band error reporting information to be inserted in the V5 byte of tributary TU #1 of TUG2 #1. When the IBER1 bit is low, in band error reporting is disabled and the V5 byte of tributary TU #1 of TUG2 #1 or the G1 byte of the TU3 is not modified.~~

IBER1-IBER7:

The IBER1 to IBER7 bits control in band error reporting for tributary TU #1 in TUG2 #2 to TUG2 #7, respectively. Setting an IBER*x* bit high causes in band error reporting information to be inserted in the V5 byte of tributary TU #1 of the corresponding TUG2. When an IBER*x* bit is low, in band error reporting is disabled and the V5 byte of tributary TU #1 of the corresponding TUG2 is not modified.

3 FUNCTIONAL DISCREPANCIES

3.1 Outgoing V1 in Locked Mode Not Aligned to H4 Marker on OTMF Pin

3.1.1 Description

When the OTMF input is configured (OTMFH4 bit in Register 01H set to logic 1) to accept the H4 byte marker for the last frame in a tributary multiframe, the outgoing V1 signal on the LC1J1V1 pin in Locked Bus mode (LV1EN bit in Register 01H set to logic 0) is generated one frame late. The V1 signal incorrectly marks the second frame instead of the first frame in the tributary multiframe. The multiframe sequence is generated correctly in the H4 byte of the outgoing stream.

Note: If the outgoing V1 signal on the LC1J1V1 pin is not required by the downstream device, then this errata may be ignored.

3.1.2 Hardware Workaround

The workaround is implemented by configuring the OTMF input pin to accept the V1 marker (LV1EN bit in Register 01H set to logic 0) instead of the H4 marker. The external logic must also be configured to provide the V1 marker on the OTMF pin instead of the H4 marker. In this case, the outgoing V1 signal is generated correctly.

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