PRELIMINARY PRODUCT INFORMATION

NEC
ELECTRON DEVICE

BIPOLAR ANALOG INTEGRATED CIRCUIT
μPC1853

MATRIX SURROUND IC FOR I²C BUS

THe μPC1853 is a phase shift matrix surround IC. Only 2 speakers in front side can make implement wide sound expansion, and by adding rear speakers, rich three-dimensional sound can be obtained.
This IC can perform all controls such as mode change and volume control etc. through an I²C bus.

FEATURES

- Any control is possible through an I²C bus.
- Surround effect can be realized by only 2 speakers in front side.
- Volume and balance control circuits are incorporated.
- Tone (bass and treble) control circuits are incorporated.
- Output pin which can adjust levels only for low frequency sound is attached.
- Output pin which can adjust levels only for AV amplifier.

USE

- TV

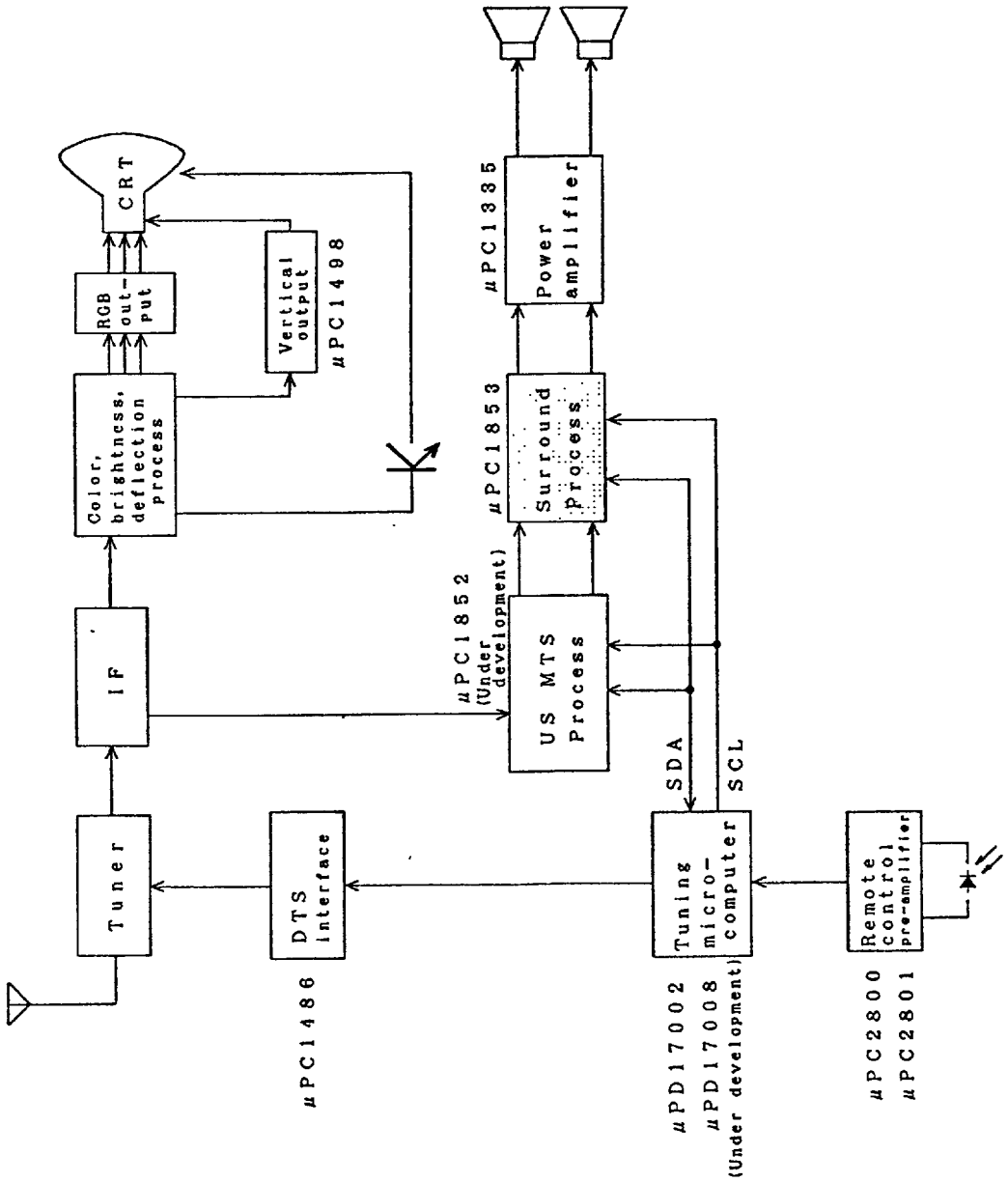
ORDER INFORMATION

Order name	Package	Quality level
μPC1853CT	30 pin shrink DIP (400 mil)	Standard (for general electronic equipment)

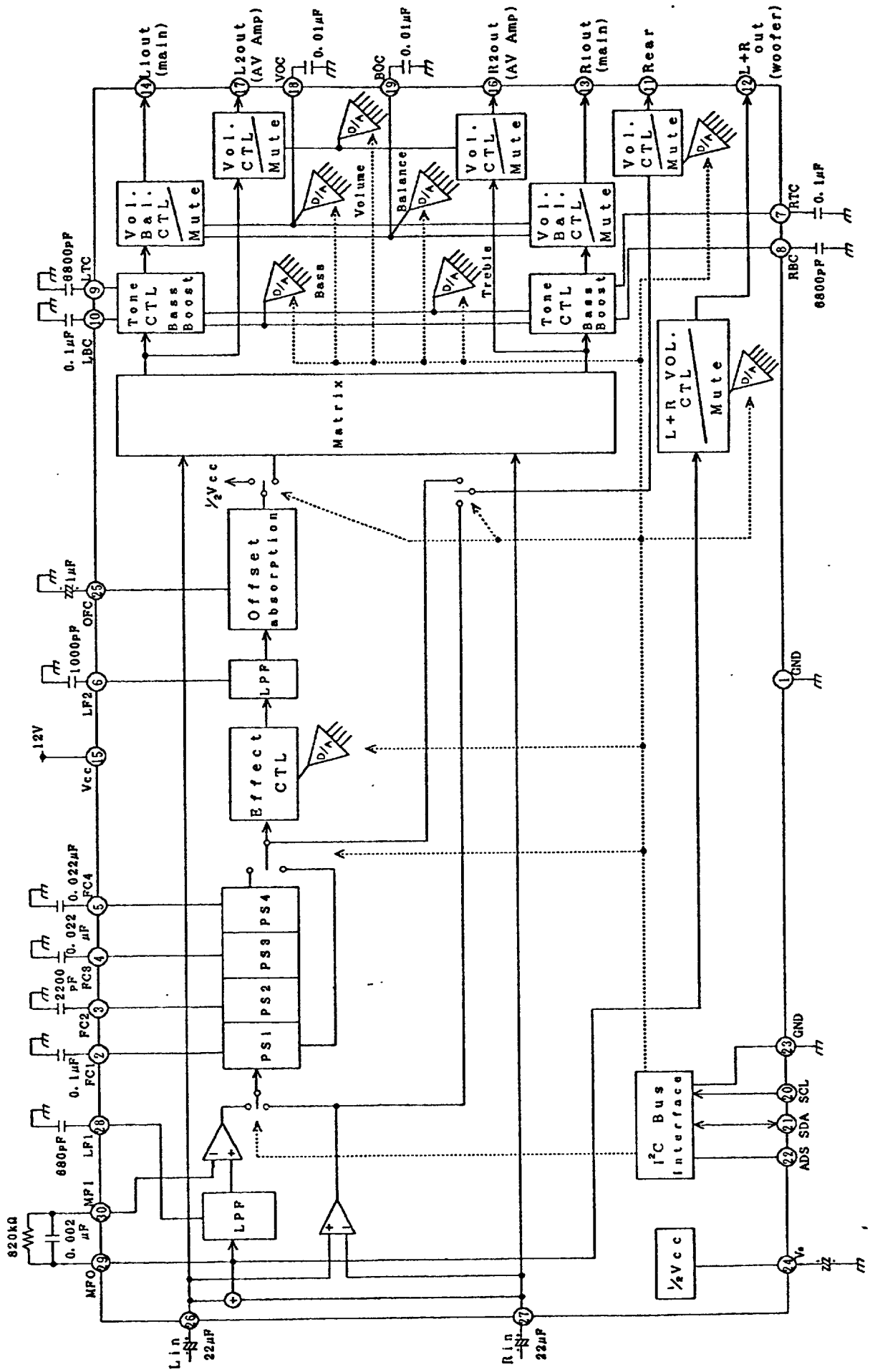
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) Published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

The information contained in this document is being issued in advanced of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.

SYSTEM BLOCK DIAGRAM (TV)



μPC1853 BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

Item	Symbol	Conditions	Ratings	Unit
Supply voltage	Vcc	No signal	14.0	V
Interface pin voltage	Vcont	20, 21 pin	Vcc + 0.2	V
Input signal voltage	Vin	26, 27 pin	Vcc	V
Operating temperature	Topt	Vcc = 12 V	-20 ~ +75	℃
Storage temperature	Tstg		-40 ~ +125	℃

RECOMMENDED OPERATING CONDITIONS

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	Vcc	No signal	10.8	12.0	13.2	V
Input signal voltage	Vin	26, 27 pin	—	1.4	8.2	V_{pp}
Interface pin voltage (H)	Vcont(H)	20, 21 pin	3.5		Vcc	V
Interface pin voltage (L)	Vcont(L)	20, 21 pin	0		1.5	V

ABOUT I²C BUS INTERFACE

The μPC1853 has serial bus function. This serial bus is a double wired bus developed by PHILIPS Corporation. It is composed of 2 wires, serial clock line (SCL) and serial data line (SDA).

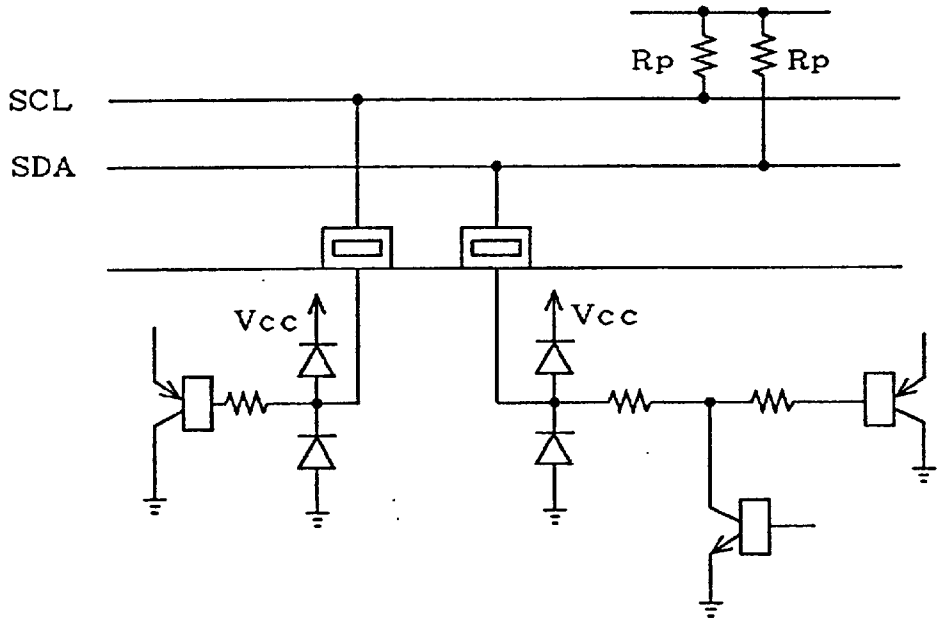
The μPC1853 has built-in I²C bus interface circuit, 9 rewritable registers (8 bits).

SCL (Serial Clock Line)

The master CPU outputs the serial clock to synchronize with the data. According to this clock, the μPC1853 takes in the serial data. Input level is compatible with CMOS.

SDA (Serial Data Line)

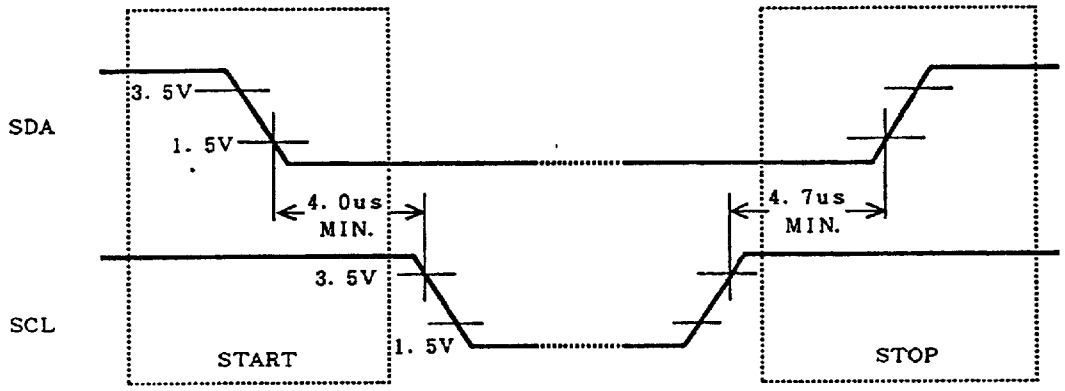
The master CPU outputs the data which is synchronized with the serial clock. The μPC1853 takes in this data according to the clock. Input level is compatible with CMOS.



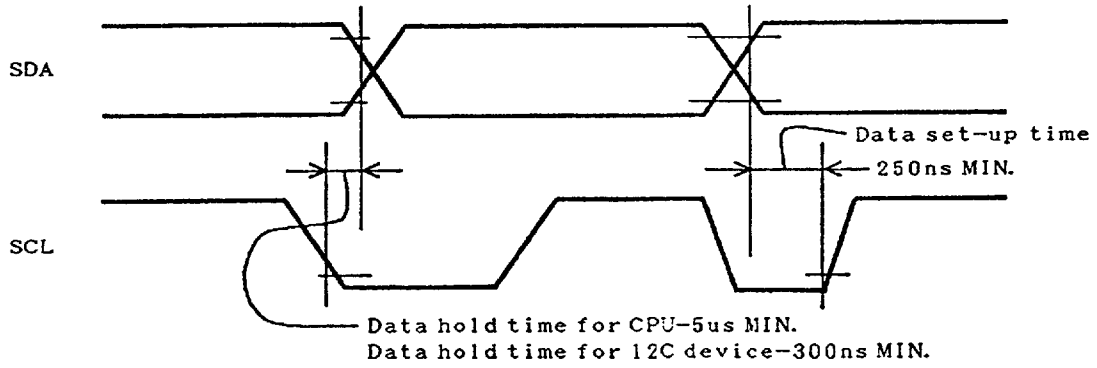
DATA TRANSFER

(1) Start Condition
Start condition is made by falling of SDA from "H" to "L" during SCL is "H" as shown in the following figure.
When this condition is received, the μPC1853 takes in the data synchronized with the clock after that.

(2) Stop Condition
Stop condition is made by rising of SDA from "L" to "H" during SCL is "H" as shown in the following figure.
When this condition is received, the μPC1853 stops to take in or output the data.



(3) Data Transfer
In case of data transfer, data changing should be executed during SCL is "L". When SCL is "H", be sure not to change the data.



DATA TRANSFER FORMAT

Data is composed of 8 bits unit, and 1 bit of acknowledge bit is always added after this 8 bits data. When the data is transferred, it should be MSB first which is transferred from MSB.

The 1 byte immediately after start condition specifies the chip address (slave address; note). This slave address is composed of 7 bits. The remaining 1 bit is read/write bit which specifies the direction of the data transferred after that.

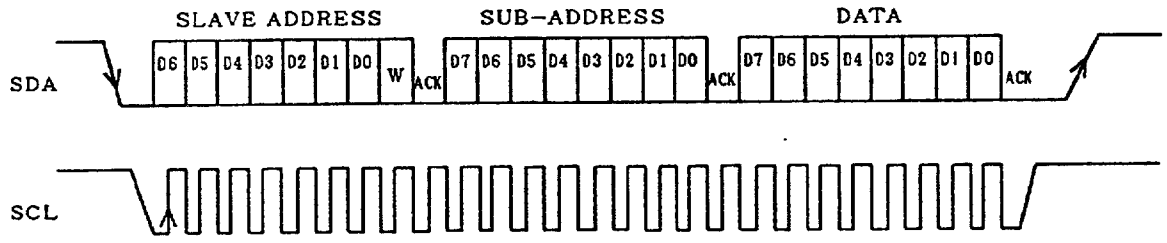
Read means to transfer the data from the μPC1853 to master CPU. Write means to transfer the data from master CPU to the μPC1853. In case of read mode, write "0" to read/write bit and in case of write mode, write "1" to the bit.

Note The slave address of the μPC1853 has been applied to PHILIPS Corporation at present.

In case of write mode, the byte following the slave address is subaddress byte of the μPC1853.

The μPC1853 has 9 subaddresses from SA_0 to SA_8, and each of them is composed of 8 bits. The data which is set to subaddress follows next to this subaddress byte.

The following is an example of data transfer in write mode.



The μPC1853 has auto increment function which increments the subaddress automatically in write mode. (Bit D0 of Subaddress 00H~07H is "1".)

By using this function, once the slave address and the subaddress are set, data can be transferred continuously to the subaddress after that. It is available for initializing, etc..

(1) 1 Byte Data Transfer

The following is the format in case of transferring 1 byte data.

S T A	SLAVE ADDRESS	W	A C K	SUB ADDRESS	A C K	DATA	A C K	S T P

STA : START
W : WRITE MODE
ACK : ACKNOWLEDGE
STP : STOP

(2) Serial Data Transfer

The following is the format in case that 9 bytes data is transferred at once by using auto increment function.

S T A	SLAVE ADDRESS	W	A C K	SUB ADDRESS	A C K	DATA1	A C K	DATA2	A C K	- - -	DATA9	A C K	S T P

STA : START
W : WRITE MODE
ACK : ACKNOWLEDGE
STP : STOP

Transfer "00H" after the start and the slave address like above figure. Transfer the data of SA_0 after the subaddress, and then transfer the data of SA_1, SA_2,..., SA_8 continuously without transferring the stop condition. Finally, transfer the stop condition and terminate.

The increment of the subaddress stops automatically when the subaddress comes to "07H" inside.

(3) Acknowledge

On I^2C bus, acknowledge bit is added to the 9th bit after data in order to judge whether data transfer is successful or not.

The master CPU judges it with acknowledge condition, "H" and "L".

When this acknowledge period is "L", it means success.

And when the condition is "H", it means failure of transfer or forced release of bus as NAK condition.

The NAK condition is when wrong slave address is transferred to slave IC or data transfer from slave side is finished.

EXPLANATION OF EACH COMMAND

1. SURROUND ON/OFF (BIT D7 OF SUBADDRESS 08H USED)

By controlling the bit D7 data of subaddress 08H, the switches whether indirect sound signal should be added or not is possible.

data "0".....Original signal is taken out directly (OFF mode).

data "1".....The signal passed through the phase shifter (indirect sound) is added to original signal. (surround mode).

2. MON/ST SWITCH (BIT D4 OF SUBADDRESS 08H USED)

By controlling the bit D4 data of subaddress 08H, the surround mode can be selected monaural mode or stereo mode.

data "0".....Stereo mode ; Stereo mode makes surround effect.

data "1".....Monaural mode ; Monaural mode makes output frequency characteristic in the form of comb, then produces simulated stereo.

3. SELECT STEPS OF PHASE SHIFTER (BIT D5 OF SUBADDRESS 08H USED)

By controlling the bit D5 data of subaddress 08H, the number of steps of phase shifters which turn the phase of indirect sound signal can be selected 1 or 4 steps.

data "0".....4 steps of phase shifter are used.

data "1".....1 step of phase shifter is used.

4. BOOST ON/OFF (BIT D6 OF SUBADDRESS 00H USED)

By controlling the bit D6 data of subaddress 00H, the switches whether low frequency boost should be on or off is possible.

data "0".....The low frequency boost is OFF.

data "1".....The low frequency boost is ON.

5. BOOST GAIN (BIT D5 OF SUBADDRESS 00H USED)

By controlling the bit D5 data of subaddress 00H, the boost gain can be selected 3 dB or 6 dB.

data "0".....The boost gain is 6 dB.

data "1".....The boost gain is 3 dB.

6. REAR OUTPUT SELECT (BIT D7 OF SUBADDRESS 00H USED)

By controlling the bit D7 data of subaddress 00H, the rear output can be selected L-R signal directly or ϕ(L-R) signal which is L-R signal through phase sifter.

data "0".....The rear output is L-R signal.

data "1".....The rear output is ϕ(L-R) signal.

7. MAIN OUTPUT VOLUME CONTROL (BIT D5 TO D0 OF SUBADDRESS 01H USED)

By controlling the bit D5 to D0 data of subaddress 01H, the output volume level can be controlled by 64 steps. The volume attenuation is -80 dB typ. (In the case of OFF mode, 1 kHz, 1.4 Vp-p input)

8. BALANCE CONTROL (BIT D5 TO D0 OF SUBADDRESS 02H USED)

By controlling the bit D5 to D0 data of subaddress 02H, balance of the left and right output can be adjusted by 64 steps.

The balance attenuation volume is -15 dB typ..

9. BASS CONTROL (BIT D5 TO D0 OF SUBADDRESS 03H USED)

By controlling the bit D5 to D0 data of subaddress 03H, the tone quality of the low tone side can be adjusted by 64 steps. The low area boost/cut volume are ±10 dB in 100 Hz. (If it is 0 dB in 1 kHz and in OFF mode).

10. TREBLE CONTROL (BIT D5 TO D0 OF SUBADDRESS 04H USED)

By controlling the bit D5 to D0 data of subaddress 04H, the tone quality of the high tone side can be adjusted by 64 steps. The high area boost/cut volume are ±10 dB in 10 kHz. (If it is 0 dB in 1 kHz and in OFF mode).

11. L+R OUTPUT VOLUME CONTROL (BIT D5 TO D0 OF SUBADDRESS 05H USHED)

By controlling the bit D5 to D0 data of subaddress 05H, L+R output sound volume can be adjusted in 64 levels. The volume attenuation is -80 dB typ. (In the case of 1 kHz, 1.4 Vp-p input)

12. AUDIO OUTPUT VOLUME CONTROL (BIT D5 TO D0 OF SUBADDRESS 06H USHED)

By controlling the bit D5 to D0 data of subaddress 06H, audio output sound volume can be adjusted in 64 levels. The volume attenuation is -80 dB typ. (In case of 1 kHz, 1.4 Vp-p input)

13. REAR OUTPUT VOLUME CONTROL (BIT D5 TO D0 OF SUBADDRESS 07H USHED)

By controlling the bit D5 to D0 data of subaddress 07H, rear output volume can be adjusted in 64 levels. The volume attenuation is -80 dB typ. (In case of 1 kHz, 1.4 Vp-p input)

14. EFFECT CONTROL (BIT D3 TO D0 OF SUBADDRESS 08H USED)

By controlling the bit D3 to D0 data of subaddress 08H, the volume of indirect sound signal (surround signal) added to original signal can be adjusted in 16 levels.

15. MAIN OUTPUT MUTE ON/OFF (BIT D1 OF SUBADDRESS 00H USED)

By controlling the bit D1 data of subaddress 00H, the switches whether main output mute should be on or off is possible.
data "0".....Main output mute is OFF.
data "1".....Main output mute is ON.

16. AUDIO OUTPUT MUTE ON/OFF (BIT D2 OF SUBADDRESS 00H USED)

By controlling the bit D2 data of subaddress 00H, the switches whether audio output mute should be on or off is possible.
data "0".....Audio output mute is OFF.
data "1".....Audio output mute is ON.

17. L+R OUTPUT MUTE ON/OFF (BIT D3 OF SUBADDRESS 00H USED)

By controlling the bit D3 data of subaddress 00H, the switches whether L+R output mute should be on or off is possible.
data "0".....Audio output mute is OFF.
data "1".....Audio output mute is ON.

18. REAR OUTPUT MUTE ON/OFF (BIT D4 OF SUBADDRESS 00H USED)

By controlling the bit D4 data of subaddress 00H, the switches whether rear output mute should be on or off is possible.
data "0".....Audio output mute is OFF.
data "1".....Audio output mute is ON.

19. AUDIO OUTPUT VOLUME LINKED WITH MAIN VOLUME/INDEPENDENTLY (BIT D0 OF SUBADDRESS 00H USED)

By controlling the bit D0 data of subaddress 00H, the switches whether audio output volume should be linked with main volume or independently is possible.
data "0".....Audio output volume can be controlled independently.
data "1".....Audio output volume can be linked with main volume.

20. AUTO INCREMENT ON/OFF (BIT D6 OF SUBADDRESS 01H TO 08H USED)

By controlling the bit D6 data of subaddress 01H to 08H, the switches whether auto increment should be on or off is possible.
data "0".....Auto increment is OFF.
data "1".....Auto increment is ON.

COMMAND LIST OF μPC1853

Sub-address	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
00H	Rear output select 0: φ (L-R) 1:L-R	Boost ON/OFF 0:OFF 1:ON	Boost Gain 0:6dB 1:3dB	Rear output mute 0:OFF 1:ON	L+R output mute 0:OFF 1:ON	Audio output mute 0:OFF 1:ON	Main output mute 0:OFF 1:ON	Audio output volume 0: independently 1: linked with main volume
01H	0	Auto increment 0:OFF 1:ON	Main output volume control					
02H	0	Auto increment 0:OFF 1:ON	Balance control					
03H	0	Auto increment 0:OFF 1:ON	Bass control					
04H	0	Auto increment 0:OFF 1:ON	Treble control					
05H	0	Auto increment 0:OFF 1:ON	L+R output volume control					
06H	0	Auto increment 0:OFF 1:ON	Audio output volume control					
07H	0	Auto increment 0:OFF 1:ON	Rear output volume control					
08H	Surround ON/OFF 0:OFF 1:ON	Effect control auto increment 0:OFF 1:ON	Number of steps of phase shifters 0:4 steps 1:1 step	MON/ST select 0:ST 1:MONO	Effect control			

GND :GROUND(DIGITAL, ANALOG) 1, 23 PIN
FC1 :CAPACITOR1 FOR PHASE SHIFTER 2 PIN
FC2 :CAPACITOR2 FOR PHASE SHIFTER 3 PIN
FC3 :CAPACITOR3 FOR PHASE SHIFTER 4 PIN
FC4 :CAPACITOR4 FOR PHASE SHIFTER 5 PIN
LF2 :LOW PASS FILTER2 6 PIN
RTC :R TREBLE CAPACITOR 7 PIN
RBC :R BASS CAPACITOR 8 PIN
LTC :L TREBLE CAPACITOR 9 PIN
LBC :L BASS CAPACITOR 10 PIN
VCC :POWER SUPPLY 15 PIN
VOC :VOLUME OFFSET CAPACITOR 18 PIN
BOC :BALANCE OFFSET CAPACITOR 19 PIN
SCL :SERIAL CLOCK LINE 20 PIN
SDA :SERIAL DATA 21 PIN
ADS :ADDRESS SELECT 22 PIN
VB :BIAS VOLTAGE 24 PIN
OFC :CAPACITOR OF OFFSET ABSORPTION 25 PIN
LIN :L INPUT 26 PIN
RIN :R INPUT 27 PIN
LF1 :LOW PASS FILTER1 28 PIN
MFO :MONAURAL FILTER OUTPUT 29 PIN
MFI :MONAURAL FILTER INPUT 30 PIN