

TC74LVX86F, TC74LVX86FN, TC74LVX86FT

QUAD EXCLUSIVE OR GATE

The TC74LVX86 is a high speed CMOS EXCLUSIVE OR GATE fabricated with silicon gate C²MOS technology. Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

This device is suitable for low voltage and battery operated systems.

The internal circuit includes an output buffer, which provides high noise immunity and stable output.

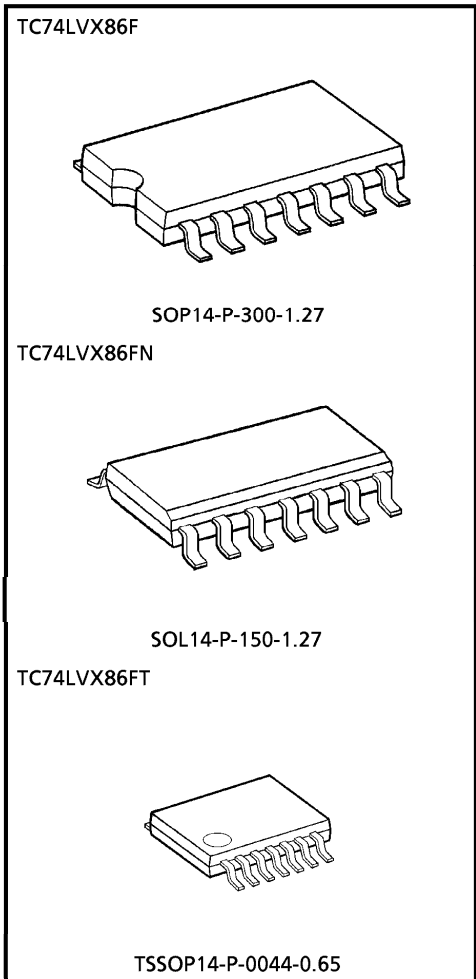
An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage.

This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

FEATURES

- High speed : $t_{pd} = 5.8ns$ (Typ.) ($V_{CC} = 3.3V$)
- Low power dissipation : $I_{CC} = 2\mu A$ (Max.) ($T_a = 25^\circ C$)
- Input voltage level : $V_{IL} = 0.8V$ (Max.) ($V_{CC} = 3V$)
 $V_{IH} = 2.0V$ (Min.) ($V_{CC} = 3V$)
- Power down protection is provided on all inputs.
- Balanced propagation delays : $t_{pLH} \approx t_{pHL}$
- Low noise : $V_{OLP} = 0.5V$ (Max.)
- Pin and function compatible with 74HC86

(Note) The JEDEC SOP (FN) is not available in Japan.



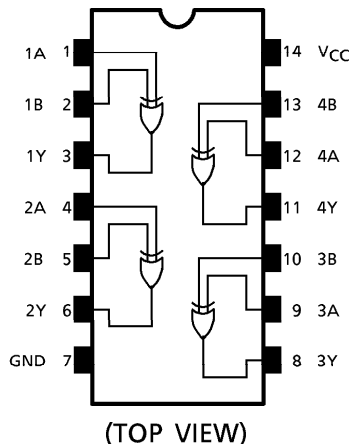
Weight

SOP14-P-300-1.27	: 0.18g (Typ.)
SOL14-P-150-1.27	: 0.12g (Typ.)
TSSOP14-P-0044-0.65	: 0.06g (Typ.)

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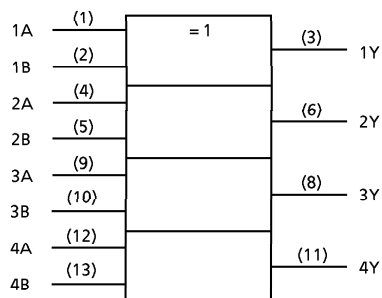
PIN ASSIGNMENT



TRUTH TABLE

INPUTS		OUTPUTS
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

IEC LOGIC SYMBOL



MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage Range	V _{CC}	-0.5~7.0	V
DC Input Voltage	V _{IN}	-0.5~7.0	V
DC Output Voltage	V _{OUT}	-0.5~V _{CC} +0.5	V
Input Diode Current	I _{IK}	-20	mA
Output Diode Current	I _{OK}	±20	mA
DC Output Current	I _{OUT}	±25	mA
DC V _{CC} /Ground Current	I _{CC}	±50	mA
Power Dissipation	P _D	180	mW
Storage Temperature	T _{stg}	-65~150	°C

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- The information contained herein is subject to change without notice.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	-40~85	°C
Input Rise And Fall Time	dt/dv	0~100	ns/V

ELECTRICAL CHARACTERISTICS

DC characteristics

PARAMETER	SYM-BOL	TEST CONDITION	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40\sim 85^\circ\text{C}$		UNIT				
				MIN.	TYP.	MAX.	MIN.	MAX.					
Input Voltage	"H" Level		V_{IH}	2.0	1.5	—	—	1.5	—	V			
				3.0	2.0	—	—	2.0	—				
				3.6	2.4	—	—	2.4	—				
	"L" Level			V_{IL}	2.0	—	—	0.5	—		0.5		
					3.0	—	—	0.8	—		0.8		
					3.6	—	—	0.8	—		0.8		
Output Voltage	"H" Level	$V_{IN} = V_{IH}$ or V_{IL}	V_{OH}		$I_{OH} = -50\mu\text{A}$	2.0	1.9	2.0	—	1.9	—	V	
					$I_{OH} = -50\mu\text{A}$	3.0	2.9	3.0	—	2.9	—		
					$I_{OH} = -4\text{mA}$	3.0	2.58	—	—	2.48	—		
	"L" Level			$V_{IN} = V_{IH}$ or V_{IL}	V_{OL}	$I_{OL} = 50\mu\text{A}$	2.0	—	0.0	0.1	—		0.1
						$I_{OL} = 50\mu\text{A}$	3.0	—	0.0	0.1	—		0.1
						$I_{OL} = 4\text{mA}$	3.0	—	—	0.36	—		0.44
Input Leakage Current	I_{IN}	$V_{IN} = 5.5\text{V}$ or GND	3.6			—	—	± 0.1	—	± 1.0	μA		
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND	3.6			—	—	2.0	—	20.0	μA		

AC characteristics (Input $t_r = t_f = 3\text{ns}$)

PARAMETER	SYM-BOL	TEST CONDITION			Ta = 25°C			Ta = -40~85°C		UNIT
			VCC (V)	CL (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t _{pLH}		2.7	15	—	7.5	14.5	1.0	17.5	ns
				50	—	10.0	18.0	1.0	21.0	
	3.3 ± 0.3		15	—	5.8	9.3	1.0	11.0		
			50	—	8.3	12.8	1.0	14.5		
Output To Output Skew	t _{osLH}	(Note 1)	2.7	50	—	—	1.5	—	1.5	ns
	t _{osHL}			3.3 ± 0.3	50	—	—	1.5	—	
Input Capacitance	C _{IN}	(Note 2)			—	4	10	—	10	pF
Power Dissipation Capacitance	C _{PD}	(Note 3)			—	18	—	—	—	pF

(Note 1) Parameter guaranteed by design.

$$(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$$

(Note 2) Parameter guaranteed by design.

(Note 3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

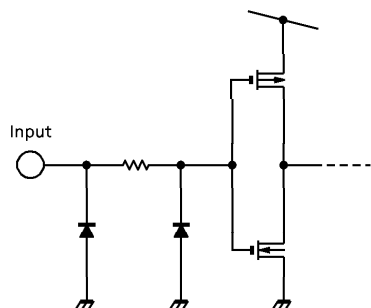
Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr.}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Gate)}$$

Noise characteristics (Ta = 25°C, Input $t_r = t_f = 3\text{ns}$, C_L = 50pF)

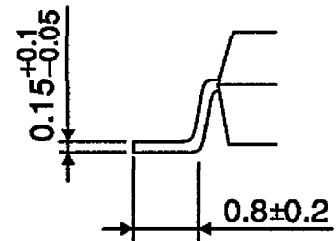
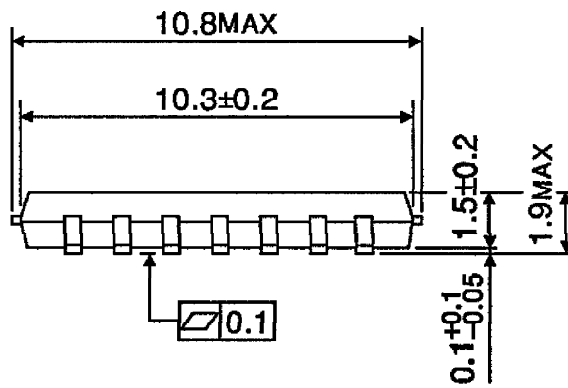
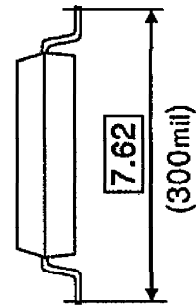
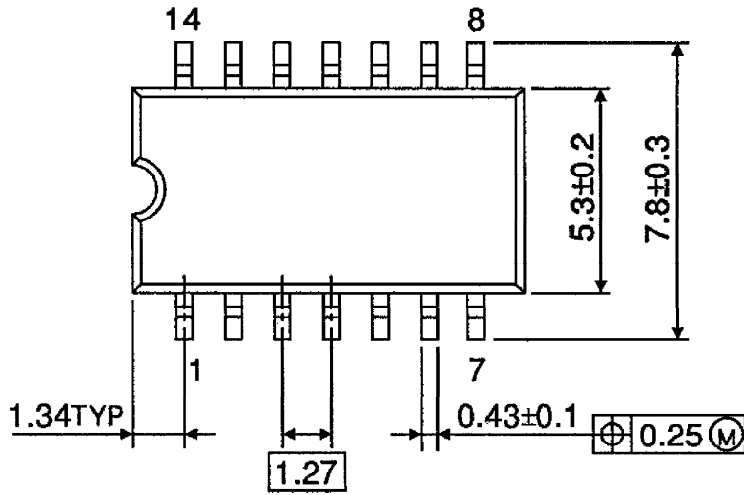
PARAMETER	SYMBOL	TEST CONDITION	VCC (V)	TYP.	LIMIT	UNIT
Quiet Output Maximum Dynamic V _{OL}	V _{OLP}		3.3	0.3	0.5	V
Quiet Output Minimum Dynamic V _{OL}	V _{OLV}		3.3	-0.3	-0.5	V
Minimum High Level Dynamic Input Voltage	V _{IHD}		3.3	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V _{ILD}		3.3	—	0.8	V

INPUT EQUIVALENT CIRCUIT



OUTLINE DRAWING
SOP14-P-300-1.27

Unit : mm

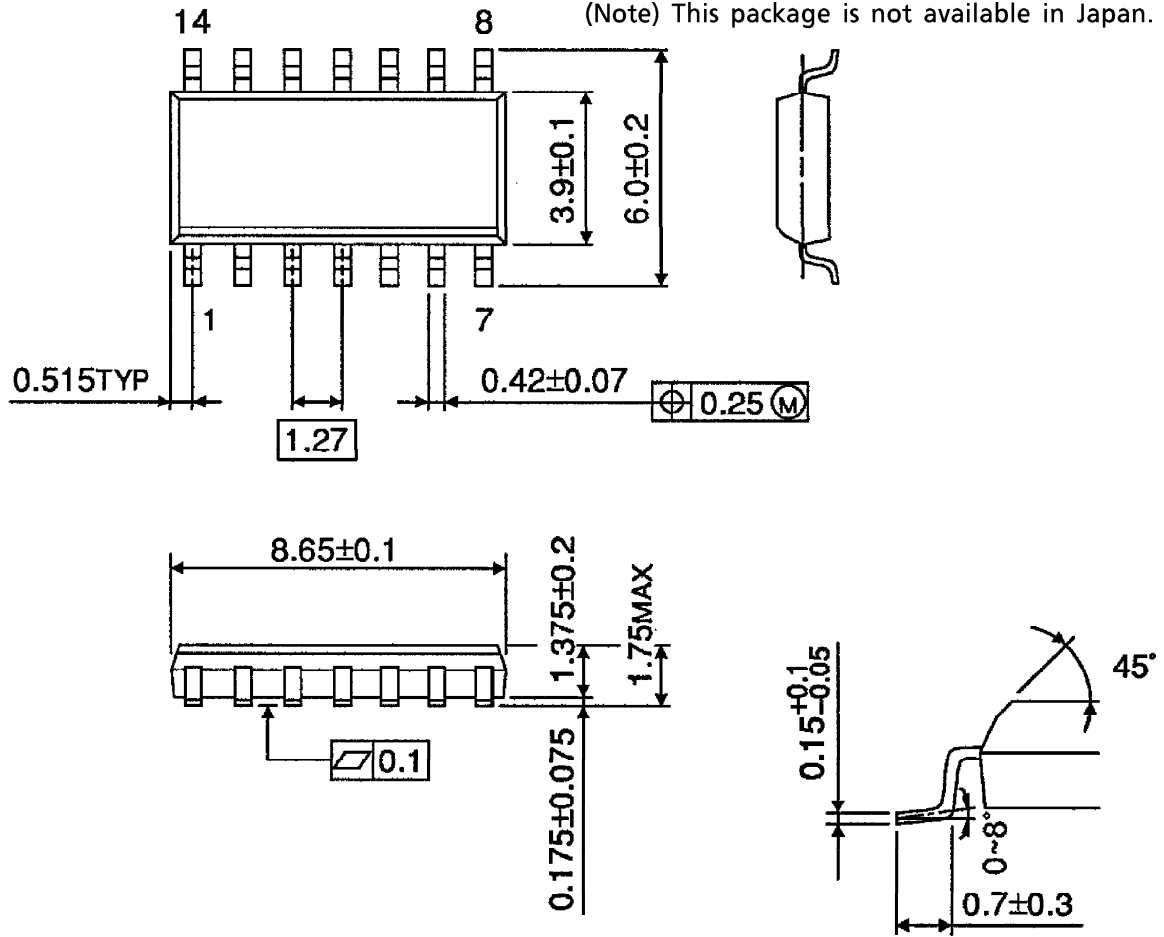


Weight : 0.18g (Typ.)

OUTLINE DRAWING
SOL14-P-150-1.27

Unit : mm

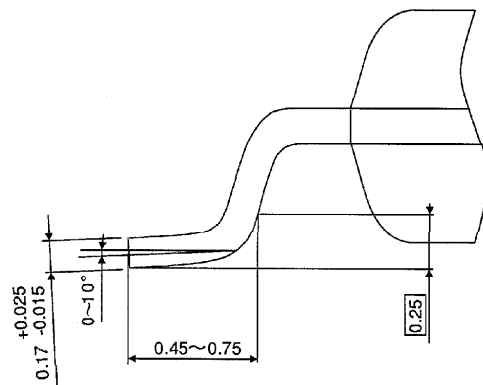
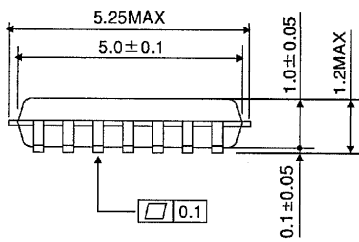
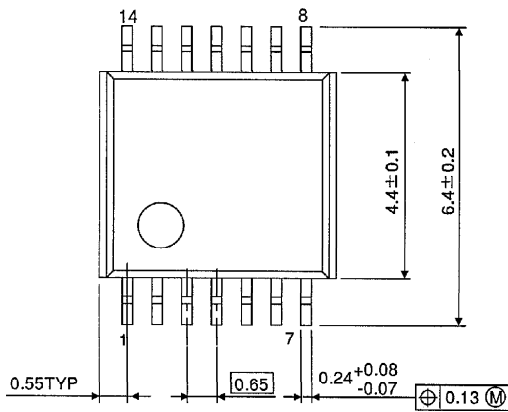
(Note) This package is not available in Japan.



Weight : 0.12g (Typ.)

OUTLINE DRAWING
TSSOP14-P-0044-0.65

Unit : mm



Weight : 0.06g (Typ.)