

## Features

- High power added efficiency
- Excellent ACP and ALT
- Three quiescent current states
- CMOS compatible state logic inputs
- Internally matched input and output
- Low leakage current
- Single +3.0 V operation

## Benefits

- Extended battery operating time
- Low current consumption
- Very small 6 × 6 mm package
- Few external components
- Fully ESD protected

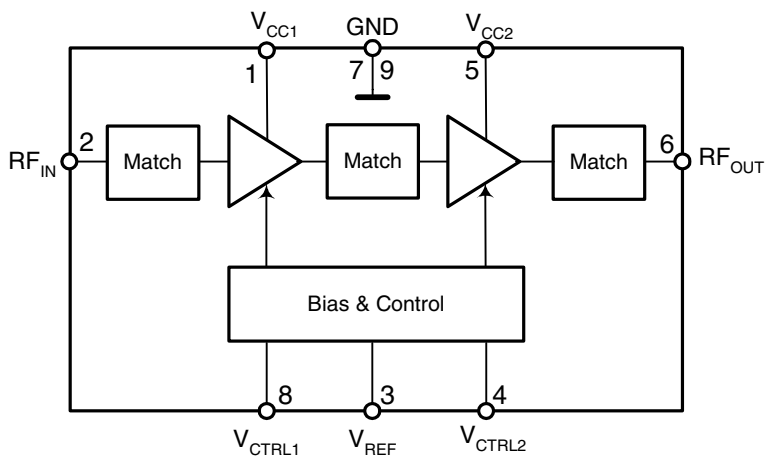
## Description

The T0370 is a 6 mm × 6 mm 3-V CDMA/AMPS cell-band power-amplifier module designed for use in mobile phones. The module incorporates a SiGe HBT two-stage CDMA / AMPS power-amplifier die. The module is 50-Ohm matched on the input and output allowing the device to be used with minimal external circuitry. Its RF performance meets the requirements for products designed to the IS-95A and B and IS-98 standards.

The T0370 gives excellent RF performance with low current consumption resulting in longer talk times in portable applications. The module features three quiescent current states to minimize current consumption for each output power level. The module has a small 6 mm × 6 mm footprint to allow use in compact phone design.

## Block Diagram

Figure 1.



## Ordering Information

Extended Type Number	Package	Remarks
T0370		6 x 6 mm housing



## 3-V CDMA/AMPS Power-Amplifier Module

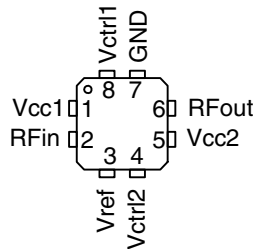
## T0370

Rev. A3, 13-Dec-01



## Pin Configuration

Figure 2. Pinning



## Pin Description

Pin	Symbol	Function
1	Vcc1	Collector supply for input stage
2	RF IN	RF input. The RF circuit is DC grounded internally, 50 ohm RF impedance.
3	Vref	Input for regulated supply for setting bias
4	Vctrl2	CMOS compatible logic level used to set bias
5	Vcc2	Collector supply for output stage
6	RF OUT	RF output. The RF circuit is DC blocked internally, 50 ohm RF impedance
7	GND	Ground
8	Vctrl1	CMOS compatible logic level used to set bias
Paddle	GND	Device Ground and heat sink, requires good thermal path

## Product Description

The T0370 is a two-stage SiGe HBT power-amplifier module in a cascade configuration intended for use in CDMA/AMPS cellular-band handsets.

## Operation

The operation modes of the T0370 are determined based on the setting of  $V_{CTRL2}$ , and  $V_{REF}$ . The truth table below defines the operating mode. In addition, please refer to the test circuit above and the section on determining the input and output matching circuits below.

Operating Mode	$V_{CTRL1}$	$V_{CTRL2}$	$V_{REF}$
High power	High	High	> 2.7 VDC
Mid power	High	Low	> 2.7 VDC
Low power	Low	Low	> 2.7 VDC
Off	0 V	0 V	0 VDC

## Application

The application circuit for the T0370 is very simple since most of the critical components are included inside the module. There are several important considerations when using the module in a phone design.

First of all, it is important that the source impedance of the  $V_{CC}$  power supply is very low. This is because the high current demand during the modulation peaks of the CDMA waveform can introduce voltage ripple at the symbol rate that will introduce additional intermodulation distortion or adjacent channel power distortion at the output of the power amplifier. If the power amplifier has a quiescent current of 100 mA and a peak current demand in excess of 1 A, it is possible to see 900 mA change in the current required from  $V_{CC}$  as the modulated signal moves from one extreme to the other. If the power supply source impedance is 1  $\Omega$ , the resulting voltage ripple would be 0.9 V which would cause the amplifier to fail in ACP requirements. Generally, the power supply source impedance should be kept as low as possible, preferably below 0.1 ohms total. Most battery technologies used in cellular telephones will support a low source impedance, but it may be necessary to supplement this in some designs with a low ESR capacitor. Ceramic or tantalum capacitors of approximately 10 micro-farads work well for this requirement.

The application circuit includes 100 nF capacitors at each of the PA control lines and  $V_{CC}$  lines to ensure proper RF bypassing. Depending on the phone board layout and circuit bypassing in other areas of the phone, some of these components may not be necessary. There are a number of VCO signals and IF signals used in a given phone design, so it is important to protect the PA module from interfering signals and to limit any interference coming from the PA itself. Care should be taken when removing any of the RF bypassing components.

One final area of concern is with excessive bypassing. If too large a value of bypassing capacitor is used on any of the control lines, it could reduce the frequency response of that control line to the point where a specification failure could occur. Please be sure that the logic lines and regulated supply lines driving the power amplifier control lines are adequate to supply peak current requirements of the bypassing capacitors chosen on the control lines.

## Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage, no RF applied	$V_{CC1}, V_{CC2}$	- 0.5 to + 6.0	VDC
Power supply voltage, RF applied	$V_{CC1}, V_{CC2}$	- 0.5 to + 5.0	VDC
Bias reference voltages and bias control voltages (Pins 3, 4, and 8 respectively)	$V_{REF}, V_{Ctrl1}, V_{Ctrl2}$	-0.5 to + 5.0	VDC
Power dissipation	$P_{DISS}$	2.5	W
Case temperature, survival	$T_C$	-40 to +100	°C
Storage temperature	$T_{stg}$	-40 to +150	°C
DC blocked RF output	$RF_{OUT}$	-20 to +20	VDC
DC grounded RF input ( no DC voltages)	$RF_{IN}$	0 to 0	VDC

Note: The part may not survive all maximums applied simultaneously.

## Thermal Resistance

Parameter	Symbol	Value	Unit
Junction-ambient	$R_{thJA}$	t.b.d.	K/W

## Operating Range

Parameter	Symbol	Value	Unit
Supply voltage	$V_{CC1}, V_{CC2}$	3.1 to 4.2	V
Recommended operating temperature	$T_c$	-30 to +85	°C

## Electrical Characteristics

$V_{CC1, CC2} = 3.4$  VDC,  $V_{REF} = 2.85$  VDC,  $V_{ctrl1, ctrl2} = 2.0$  VDC,  $R_F = 836$  MHz,  $T_{case} = 25^\circ\text{C}$ ,  
Min./Max. limits are at  $+25^\circ\text{C}$  case temperature, unless otherwise specified

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
<b>1</b>	<b>CDMA mode</b>								
1.1	Frequency		2	f	824		849	MHz	
1.2	Output power	P <sub>out</sub>	6	P <sub>out</sub>		28		dBm	
1.3	Large signal gain, high-gain mode	P <sub>out</sub> = +28 dBm, $V_{CTRL1,2} = \text{high}$	2, 6	G <sub>H</sub>	26	29.0		dB	A
1.4	Large signal gain, mid-gain mode	P <sub>out</sub> = +15 dBm, $V_{CTRL1} = \text{high}$ , $V_{CTRL2} = \text{low}$	2, 6	G <sub>M</sub>		28.0		dB	A
1.5	Large signal gain, low-gain mode	P <sub>out</sub> = 0 dBm, $V_{CTRL1,2} = \text{low}$	2, 6	G <sub>L</sub>		21		dB	A
1.6	Gain variation vs. temperature	-30 to +85°C	2, 6	ΔG		+/-1.4		dB	C
1.7	Quiescent current, high gain	$V_{CTRL1,2} = \text{high}$	1, 5	I <sub>CQ_hi</sub>		112		mA	A
1.8	Quiescent current, mid gain	$V_{CTRL1} = \text{high}$ , $V_{CTRL2} = \text{low}$	1, 5	I <sub>CQ_mid</sub>		65		mA	A
1.9	Quiescent current, low gain	$V_{CTRL1,2} = \text{low}$	1, 5	I <sub>CQ_low</sub>		25		mA	A
1.10	Output power (high)	ACPR = -49dBc, IS-95/98 standard, $V_{CTRL1,2} = \text{high}$	6			28		dBm	C
1.11	Output power (mid)	ACPR = -49dBc, IS-95/98 standard, $V_{CTRL1} = \text{high}$ , $V_{CTRL2} = \text{low}$	6			12		dBm	C
1.12	Output power (low)	ACPR = -49dBc, IS-95/98 standard, $V_{CTRL1,2} = \text{low}$	6			-0.5		dBm	C
1.13	Power added efficiency	P <sub>out</sub> = +28 dBm	6	PAE		35.0		%	A
1.14	Adjacent channel power	P <sub>out</sub> = +28 dBm, IS-95/98 standard, $V_{CTRL1,2} = \text{high}$	6	ACP		50...52		dBc	A

\*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

## Electrical Characteristics

$V_{CC1, CC2} = 3.4$  VDC,  $V_{REF} = 2.85$  VDC,  $V_{ctrl1, ctrl2} = 2.0$  VDC,  $RF = 836$  MHz,  $T_{case} = 25^{\circ}C$ ,

Min./Max. limits are at  $+25^{\circ}C$  case temperature, unless otherwise specified

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1.15	Alternate channel power	$P_{out} = +28$ dBm, IS-95/98 standard, $V_{CTRL1,2} = high$	6	ALT		-57		dBc	A
1.16	Noise power in Rx band	$P_{out} = +28$ dBm, RBW = 30 kHz IS-95/98 standard, $V_{CTRL1,2} = high$	6	$P_{noise,Rx}$		-94		dBm	C
1.17	Input VSWR	Both $I_{CQ\_hi}$ & $I_{CQ\_mid}$	2	$S_{11}$		1.6 : 1			A
1.18	Second harmonic	$P_{out} = +28$ dBm, IS-95/98 standard, $V_{CTRL1,2} = high$	6	2f		-35		dBc	A
1.19	Third harmonic	$P_{out} = +28$ dBm, IS-95/98 standard, $V_{CTRL1,2} = high$	6	3f		-45		dBc	A
1.20	Supply voltage		1, 5	$V_{CC}$	3.1	3.4	4.2	VDC	D
1.21	Reference voltage		3	$V_{ref}$	2.8	2.85	2.9	VDC	D
1.22	Bias current	$V_{CTRL1,2} = high$	3	$I_{Bias}$		10		mA	A
1.23	$V_{REF}$ current, $I_{CQ\_mid}$	Mid-power mode, $V_{CTRL1} = high$ , $V_{CTRL2} = low$				5		mA	
1.24	$V_{REF}$ current, $I_{CQ\_lo}$	Mid-power mode, $V_{CTRL1,2} = low$				2		mA	
1.25	Leakage current	$V_{CTRL1,2} = low$ , $V_{REF} = 0$ VDC				10		$\mu A$	
1.26	Logic current	At $V_{CTRL1,2}$	4, 8	$I_{CTRL1,2}$		49		$\mu A$	A
1.27	Control voltage	High Low	4, 8	$V_{CTRL1,2}$ $V_{CTRL1,2}$	1.7 0	2.0 0.25	4.5 0.5	VDC VDC	D
1.28	Ruggedness	No damage, $P_{OUT} = 28$ dBm, IS-95/98 standard, $V_{CTRL1,2} = high$	6				10 : 1		C
1.29	Stability	No oscillations, $P_{OUT} = 28$ dBm, IS-95/98 standard, $V_{CTRL1,2} = high$	6				10 : 1		A
<b>2</b>	<b>AMPS mode</b>								
2.1	Output power (saturated)	$P_{in} = +3.7$ dBm $V_{ctrl1,2} = high$	6	$P_{out}$		31.5		dBm	A
2.2	Small signal gain		6	$G_{AMPS}$		28		dB	A

\*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter



## Electrical Characteristics

$V_{CC1, CC2} = 3.4$  VDC,  $V_{REF} = 2.85$  VDC,  $V_{ctrl1, ctrl2} = 2.0$  VDC, RF = 836 MHz,  $T_{case} = 25^{\circ}C$ ,

Min./Max. limits are at  $+25^{\circ}C$  case temperature, unless otherwise specified

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
2.3	Power added efficiency	Pout = +31.5 dBm	6	PAE		51.4		%	A
2.4	Noise power in Rx band	Pout = +31.5 dBm, RBW = 30 KHz	6	$P_{Noise,Rx}$		-94		dBm	C
2.5	Input VSWR	All Operating Pout and $V_{CC1}, V_{CC2}$	2	$S_{11}$		1.6 : 1			A
2.6	Second harmonic	Pout = +31.5 dBm	6			-32.5		dBc	A
2.7	Third harmonic	Pout = +31.5 dBm	6			-42.5		dBc	A
2.8	Supply current	Pout = +31.5 dBm	1, 5	$I_{CC}$		783		mA	A

\*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

## Typical Performance, CDMA High Power Mode

Test conditions:  $V_{CC1} = 3.4$  VDC,  $V_{CC2} = 3.4$  VDC,  $V_{CTRL1} = V_{CTRL2} = 2.0$  V,  $V_{ref} = 2.85$  VDC,  $P_{out} = 28$  dBm,  $T_{case} = 25^{\circ}C$

Figure 3.

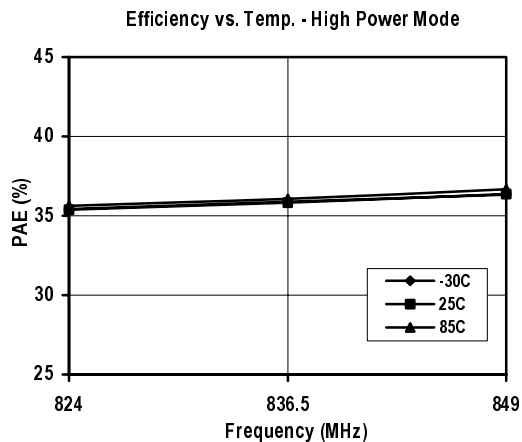


Figure 4.

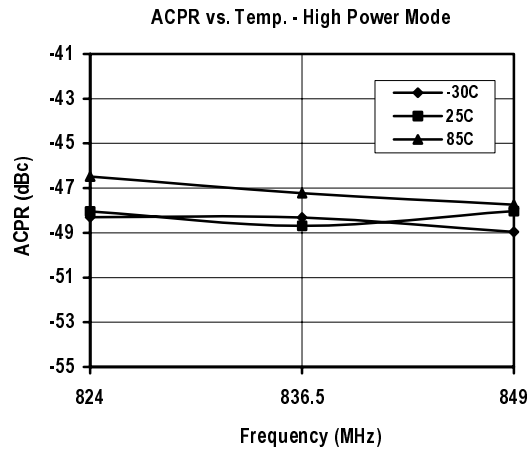


Figure 5.

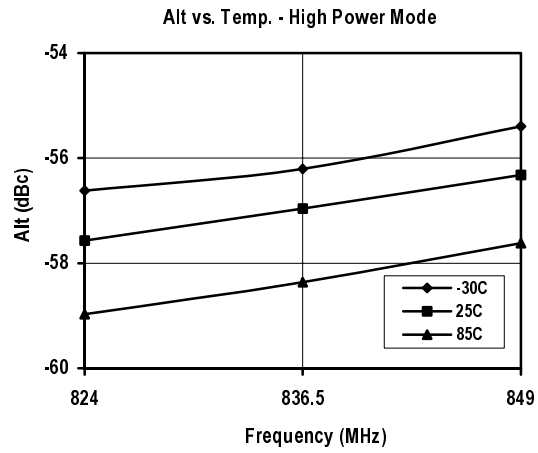


Figure 6.

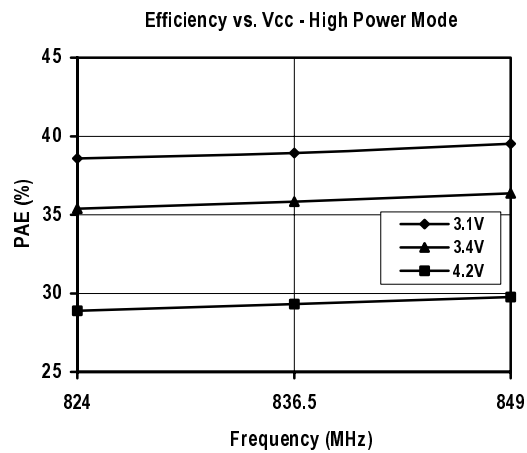


Figure 7.

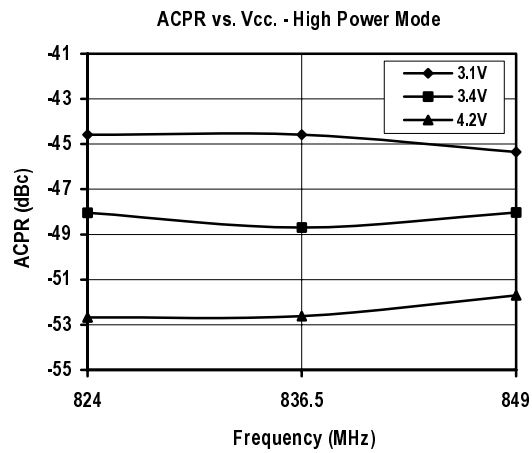


Figure 8.

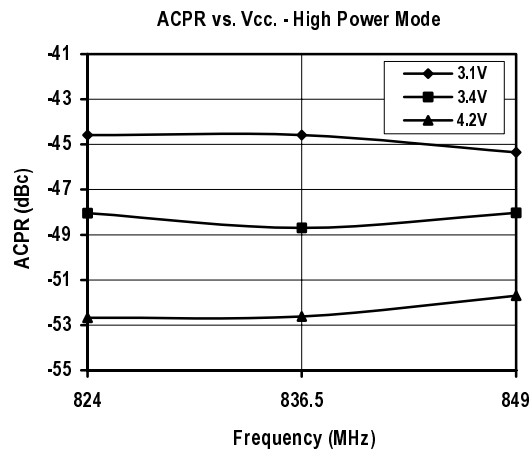


Figure 9.

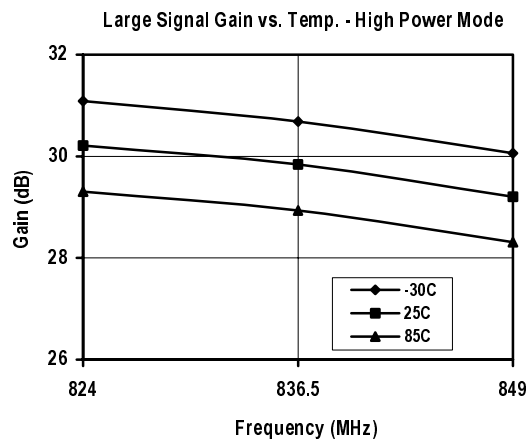




Figure 10.

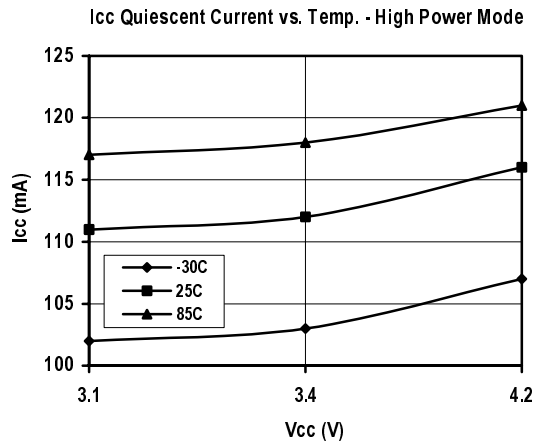
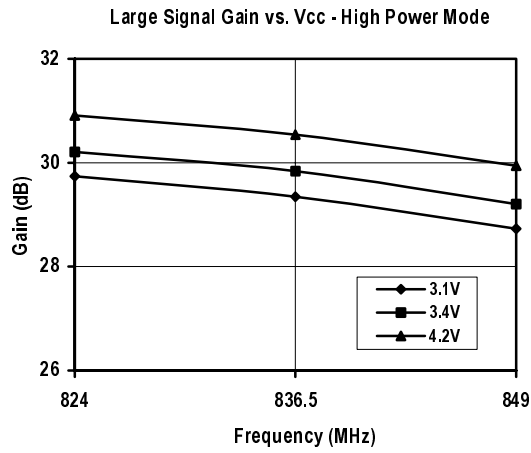


Figure 11.



### Typical Performance, CDMA Mid Power Mode

Test conditions:  $V_{CC1} = V_{CC2} = 3.4$  VDC,  $V_{CTRL1} = 1.7$  VDC,  $V_{CTRL2} = 0.5$  VDC,  $V_{ref} = 2.85$  VDC,  $P_{out} = 12$  dBm,  $T_{case} = 25^{\circ}\text{C}$

Figure 12.

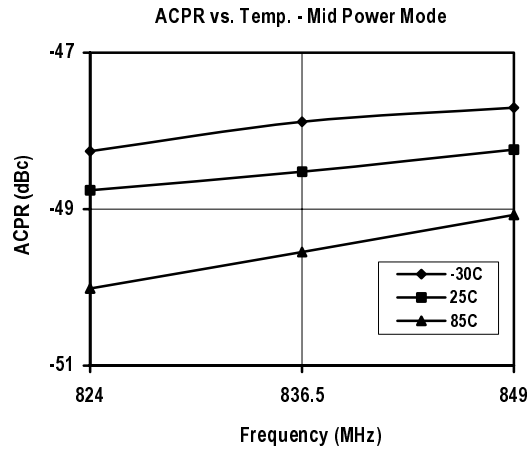


Figure 13.

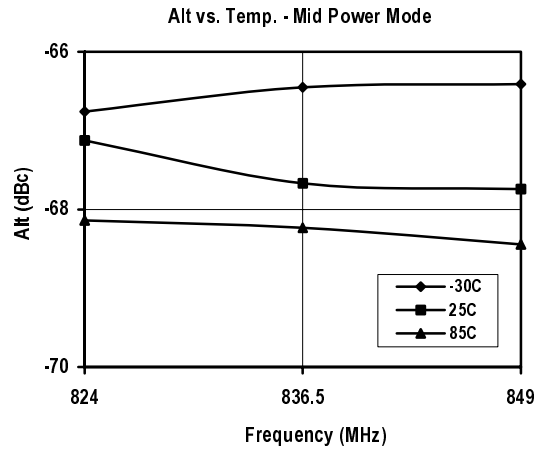


Figure 14.

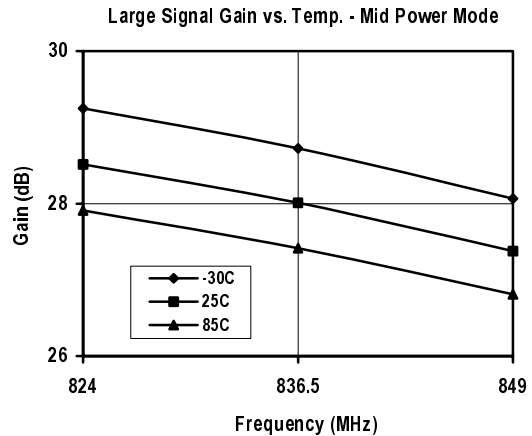


Figure 15.

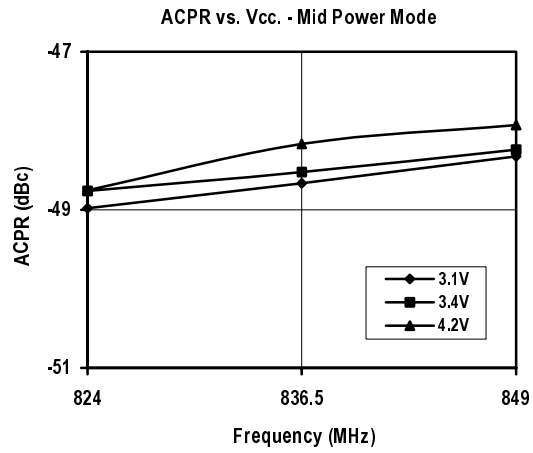


Figure 16.

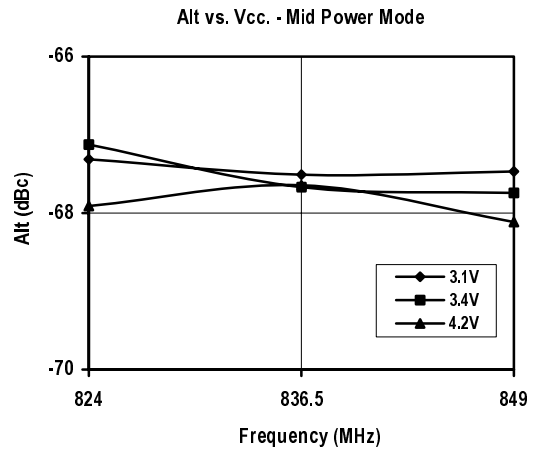


Figure 17.

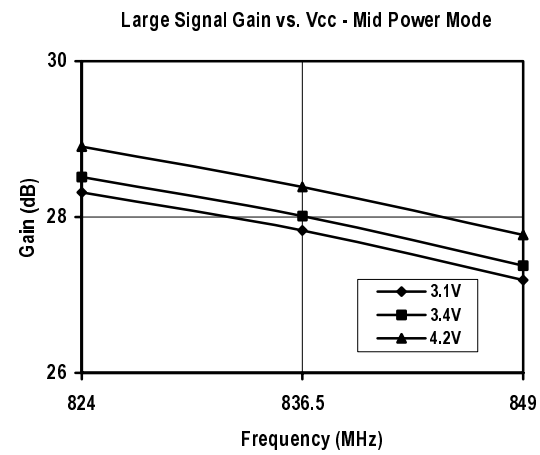
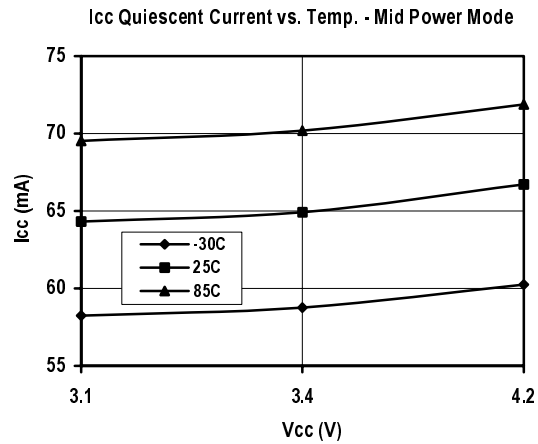


Figure 18.



### Typical Performance, CDMA Low Power Mode

Test conditions:  $V_{CC1} = V_{CC2} = 3.4$  VDC,  $V_{CTRL1} = 0.5$  VDC,  $V_{CTRL2} = 0.5$  V,  $V_{ref} = 2.85$  VDC,  $P_{out} = -0.5$  dBm,  $T_{case} = 25^{\circ}C$

Figure 19.

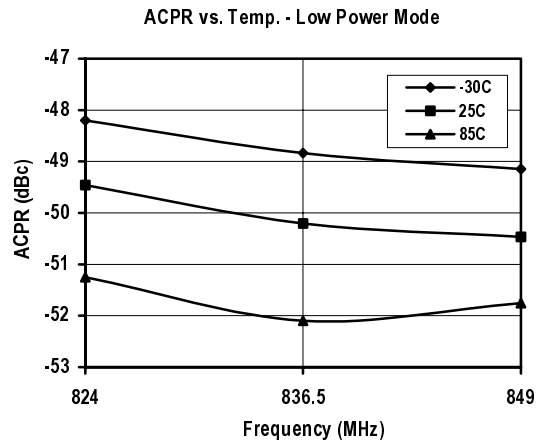


Figure 20.

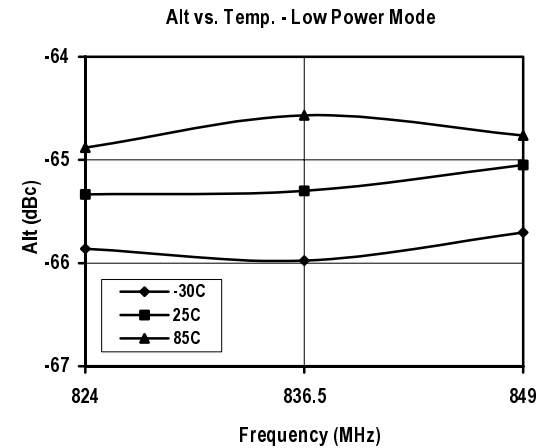


Figure 21.

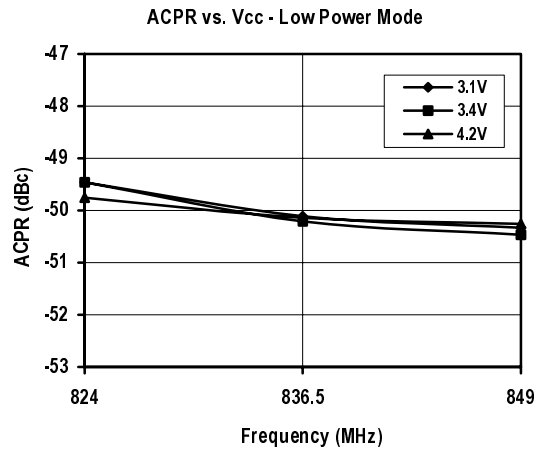


Figure 22.

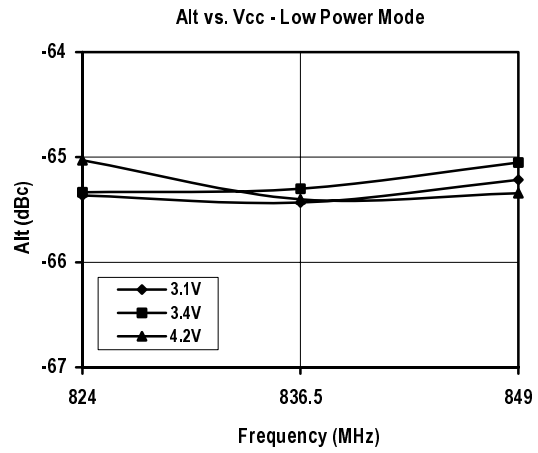


Figure 23.

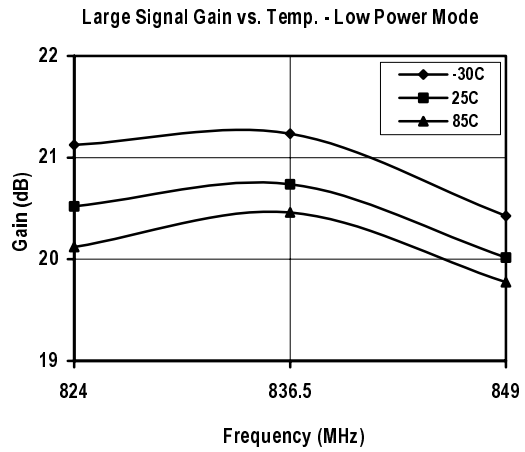


Figure 24.

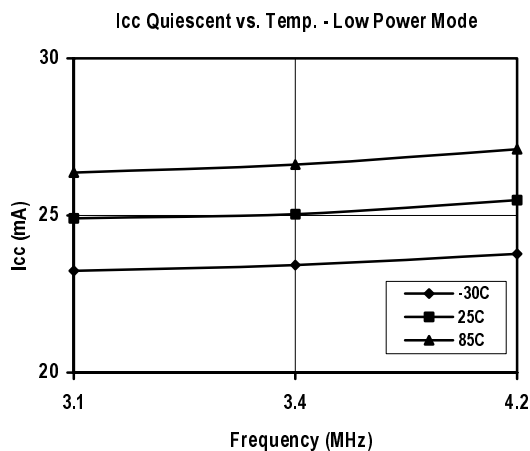
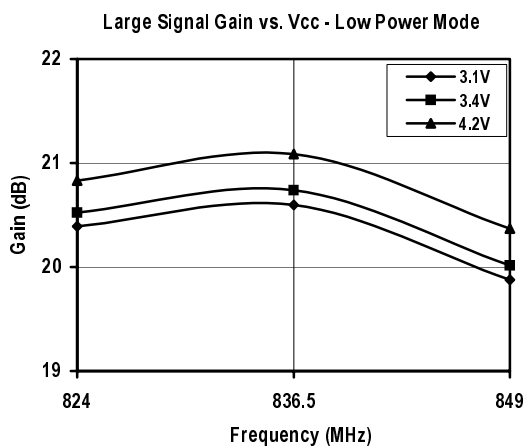


Figure 25.



### Typical Performance, AMPS Mode

Test conditions:  $V_{CC1} = V_{CC2} = 3.4$  VDC,  $V_{CTRL1} = 1.7$  VDC,  $V_{CTRL2} = 1.7$  V,  $V_{ref} = 2.85$  VDC,  $P_{in} = 5$  dBm,  $T_{case} = 25^{\circ}C$

Figure 26.

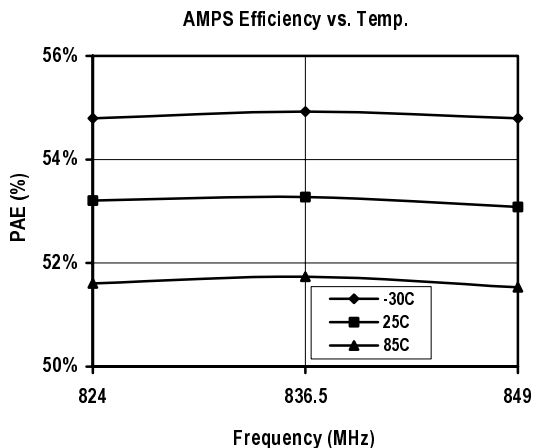


Figure 27.

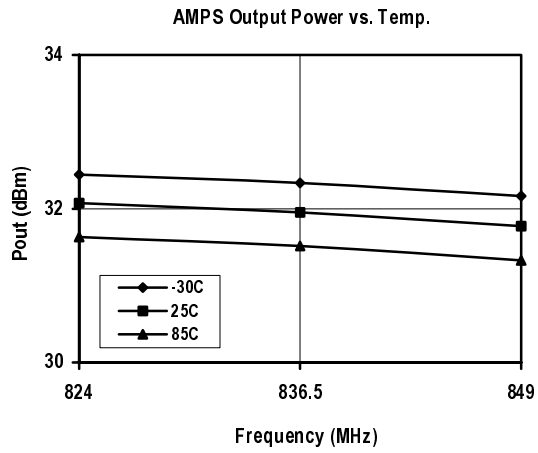


Figure 28.

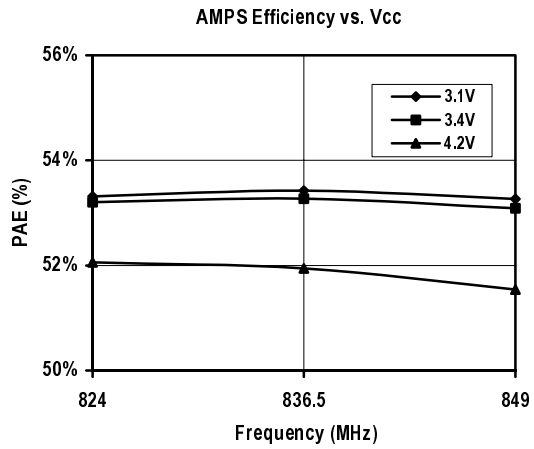
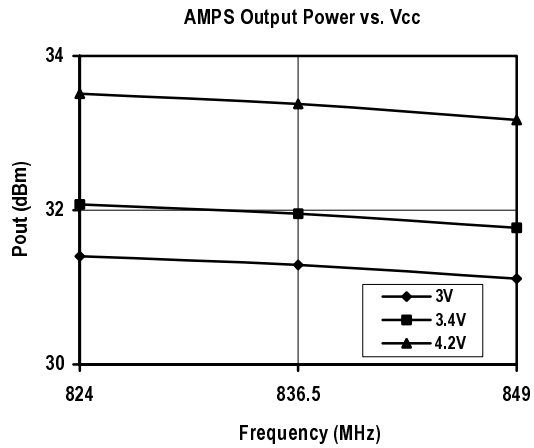


Figure 29.

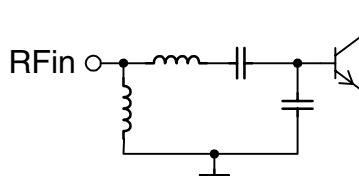


## PA Quiescent Current as a Function of CMOS Logic Signals Vctrl1 and Vctrl2

Digital Bias State	Vctrl1	Vctrl2	Icq
High power mode / AMPS mode	High	High	112 mA
Medium power mode	High	Low	65 mA
Low power mode	Low	Low	25 mA

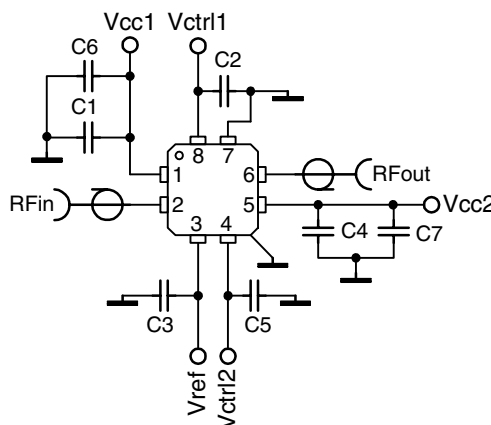
## Equivalent Circuits on Pins

Figure 30. RF input



## Schematic of Demo Board

Figure 31.



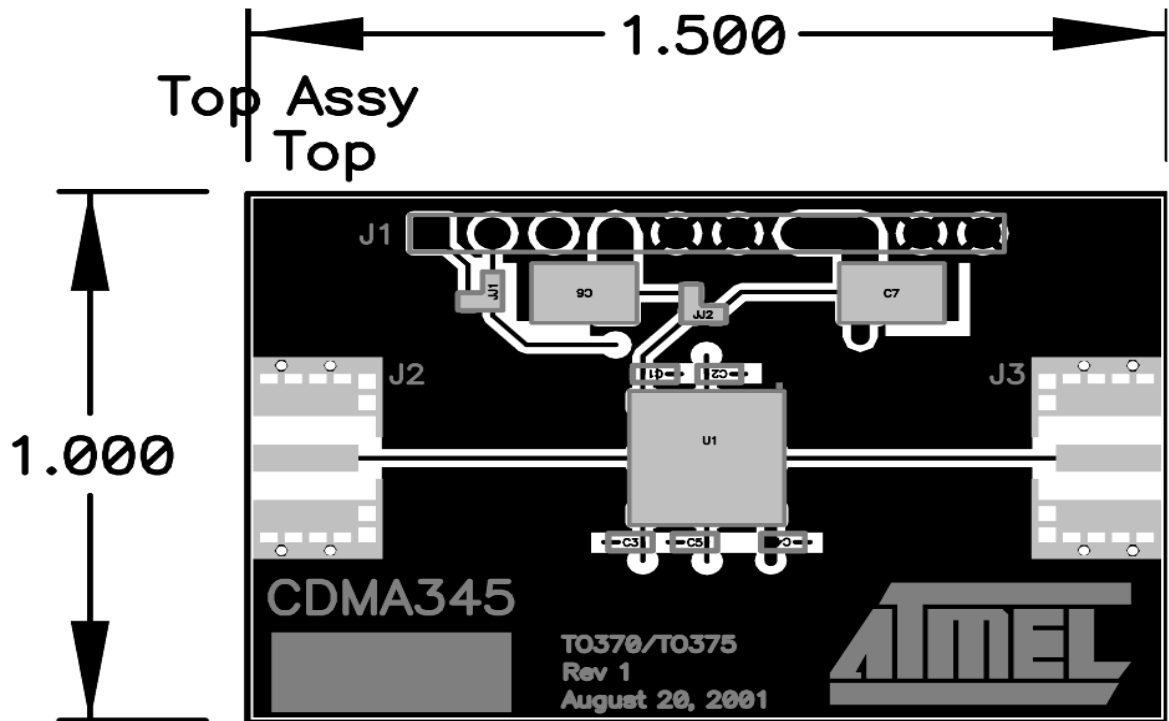
## Bill of Materials of Demo Board

Component	Reference	Vendor	Part Number / Remark	Value	Size / Package
PA Module	IC1	Atmel-WM	T0370		8 pin 6 mm square
RF Connector	J2, J3				
Capacitor	C1, C2, C3, C4, C5			100 nF	0402
Capacitor	C6, C7			10 $\mu$ F	1210 <sup>1)</sup>
Note: 1. may vary do to printed circuit board layout and material					



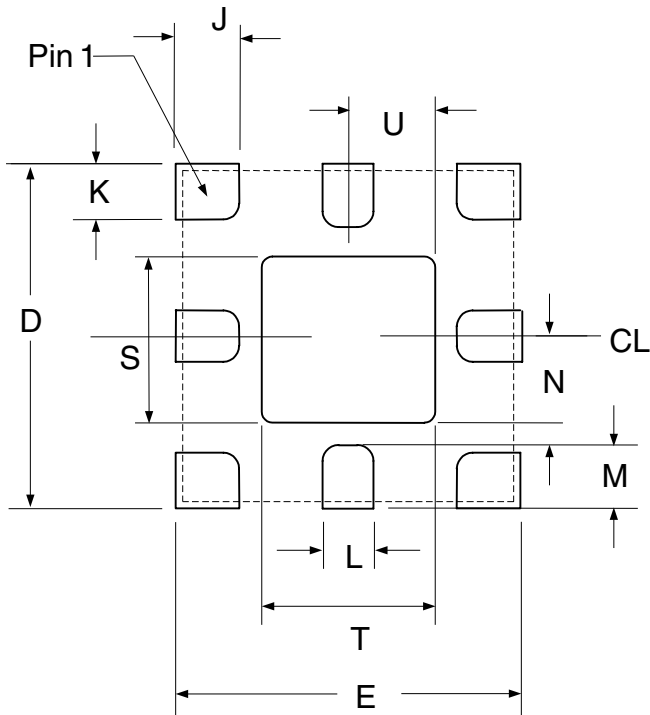
## Layout of Demo Board

Figure 32. Dimensions in inches



## Recommended PCB Layout Footprint for 8-Pin Module Plastic Package

Figure 33.

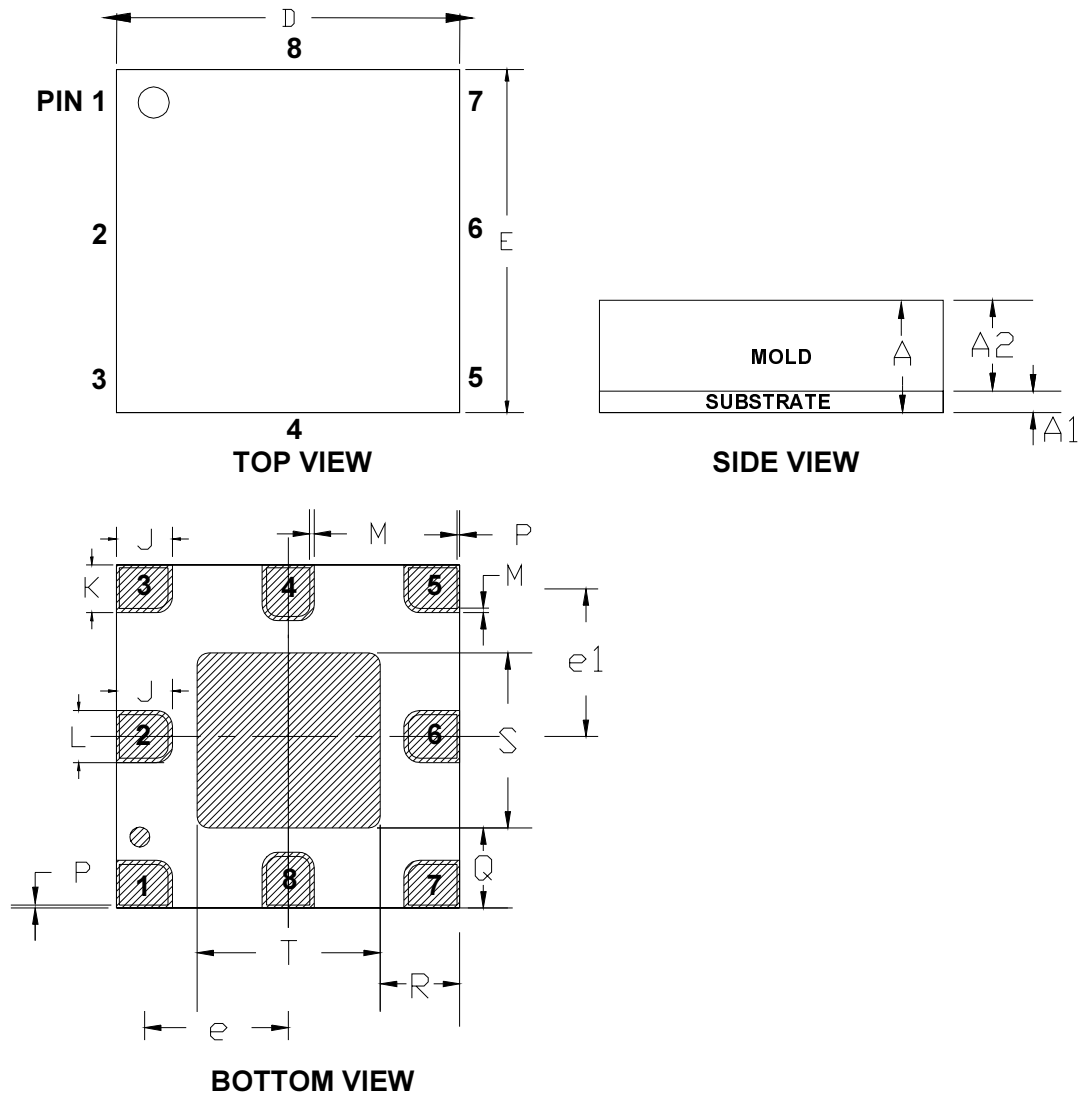


Dimensions	mm	in
D	6.35	0.250
E	6.35	0.250
J	1.17	0.046
K	1.03	0.040
L	0.95	0.037
M	1.17	0.046
N	1.60	0.063
S	3.06	0.120
T	3.20	0.126
U	1.60	0.063

Note: Only ground signal traces are allowed directly under the package.

## Package Information

Figure 34. Dimensions in mm



Designation	Description	Dimension	Note
A	OVERALL HEIGHT	1.42 +/-0.09 mm	
A1	SUBSTRATE THICKNESS	0.32 +/-0.05 mm	
A2	MOLD THICKNESS	1.10 +/-0.05 mm	
D	PACKAGE LENGTH	6.0 +/-0.1 mm	
E	PACKAGE WIDTH	6.0 +/-0.1 mm	
J	TERMINAL SOLDER MASK OPENING LENGTH (FOR ALL TERMINALS)	0.975 +/-0.035 mm	
K	TERMINAL SOLDER MASK OPENING WIDTH FOR TERMINAL 1, 3, 5, 7	0.835 +/-0.035 mm	
L	TERMINAL SOLDER MASK OPENING WIDTH FOR TERMINAL 2, 4, 6, 8	0.91 +/-0.035 mm	



Designation	Description	Dimension		Note
M	DISTANCE BETWEEN METAL PAD AND SOLDER MASK	0.075	+/-0.02 mm	
P	DISTANCE BETWEEN METAL PAD AND PACKAGE EDGE	0.05	+/-0.02 mm	
T	GND SOLDER MASK OPENING LENGTH	3.2	+/-0.1 mm	
S	GND SOLDER MASK OPENING WIDTH	3.06	+/-0.1 mm	
R	DISTANCE BETWEEN MASK OPENING AND PACKAGE EDGE	1.39	+/-0.2 mm	
Q	DISTANCE BETWEEN MASK OPENING AND PACKAGE EDGE	1.40	+/-0.2 mm	
E	TERMINAL PITCH FOR TERMINAL 3-4-5 AND 7-8-1	2.513	mm	
e1	TERMINAL PITCH FOR TERMINAL 1-2-3 AND 5-6-7	2.583	mm	

## Ozone Depleting Substances Policy Statement

It is the policy of **Atmel Germany GmbH** to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

**Atmel Germany GmbH** has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

**Atmel Germany GmbH** can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.





## Atmel Sales Offices

### **France**

3, Avenue du Centre  
78054 St.-Quentin-en-Yvelines  
Cedex  
Tel: +33 1 30 60 70 00  
Fax: +33 1 30 60 71 11

### **Germany**

Erfurter Strasse 31  
85386 Eching  
Tel: +49 89 319 70 0  
Fax: +49 89 319 46 21

Kruppstrasse 6  
45128 Essen  
Tel: +49 201 247 30 0  
Fax: +49 201 247 30 47

Theresienstrasse 2  
74072 Heilbronn  
Tel: +49 7131 67 36 36  
Fax: +49 7131 67 31 63

### **Italy**

Via Grosio, 10/8  
20151 Milano  
Tel: +39 02 38 03 71  
Fax: +39 02 38 03 72 34

### **Spain**

Principe de Vergara, 112  
28002 Madrid  
Tel: +34 91 564 51 81  
Fax: +34 91 562 75 14

### **Sweden**

Kavallerivaegen 24, Rissne  
17402 Sundbyberg  
Tel: +46 8 587 48 800  
Fax: +46 8 587 48 850

### **United Kingdom**

Easthampstead Road  
Bracknell  
Berkshire RG12 1LX  
Tel: +44 1344 707 300  
Fax: +44 1344 427 371

### **USA Western**

2325 Orchard Parkway  
San Jose, California 95131  
Tel: +1 408 441 0311  
Fax: +1 408 436 4200

### **USA Eastern**

1465 Route 31, Fifth floor  
Annandale  
New Jersey 08801  
Tel: +1 908 848 5208  
Fax: +1 908 848 5232

### **Hong Kong**

Room #1219,  
Chinachem Golden Plaza  
77 Mody Road, Tsimhatsui East  
East Kowloon, Hong Kong  
Tel: +852 23 789 789  
Fax: +852 23 755 733

### **Korea**

25-4, Yoido-Dong, Suite 605,  
Singsong Bldg.  
Youngdeungpo-Ku  
150-010 Seoul  
Tel: +822 785 1136  
Fax: +822 785 1137

### **Rep. of Singapore**

Keppel Building #03-00  
25 Tampines Street 92,  
Singapore 528877  
Tel: +65 260 8223  
Fax: +65 787 9819

### **Taiwan, R.O.C.**

8F-2, 266 Sec.1 Wen Hwa 2 Rd.  
Lin Kou Hsiang,  
244 Taipei Hsien  
Tel: +886 2 2609 5581  
Fax: +886 2 2600 2735

### **Japan**

Tonetsushinkawa Bldg.  
1-24-8 Shinkawa Chuo Ku  
Tokyo 104-0033  
Tel: +81 3 3523 3551  
Fax: +81 3 3523 7581

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### **Web Site**

<http://www.atmel-wm.com>

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Data sheets can also be retrieved from the Internet: <http://www.atmel-wm.com>