SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

STV0042 / STV0056

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SUMMARY **Page**

1 - INTRODUCTION

The purpose of this application note is to provide the user with the most important informations relevant to the hardware and software environment of the STV0042 and the STV0056 circuits. In this introduction part, we would like to mention that the STV0042/STV0056 circuits features very specific FM demodulators, consequently we would advice to pay a specific attention to the relevant chapters.

Conventions

In this note, when the explanations are commun to both STV0042 and STV0056 circuits : the circuits are called STV42/56 and when pin numbers are given, they are relevant to the STV0056 (ex : Pin 15 means Pin 15 of STV0056 (corresponding to Pin 12 of STV0042)).

When the explanations are relevant to only one circuit, the entire circuit reference is mentionned (ex : STV0042). When external components reference are given in this note, they are relevant to the STV0056 application circuit (page 31).

When speaking about software :

- R : stands for register - ex : R06 ⇒ Register 06
- B : stands for bit - ex : R06 B1 ⇒ Register 06 Bit1

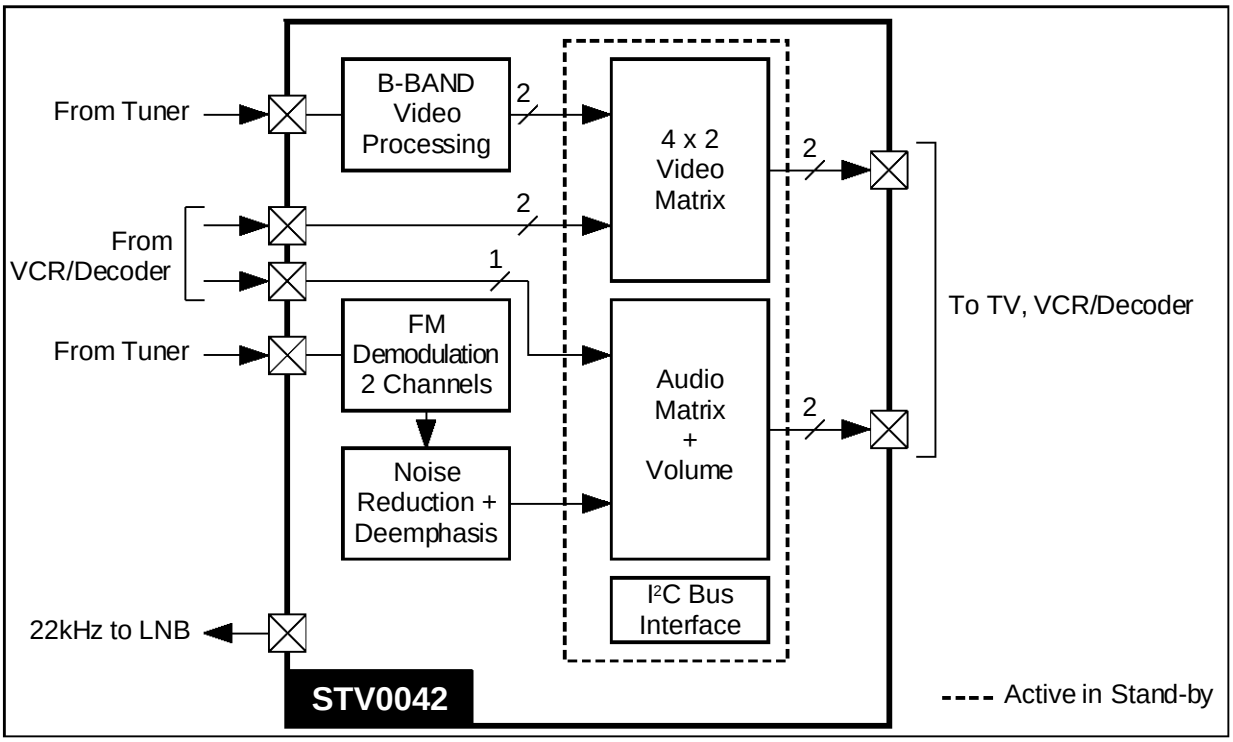
Other conventions :

- R05 B0-5 ⇒ Register 05 from Bit 0 to Bit 5
- R06 B2 B4 ⇒ Register 05 Bit 2 and Bit 4
- R05 B0-5 = 35 ; it means no attention is paid to Bit 6 and Bit 7. 35 is the hexadecimal value given by the 5 first bits.

2 - GENERAL BLOCK DIAGRAMS (differences between STV0042 and STV0056)

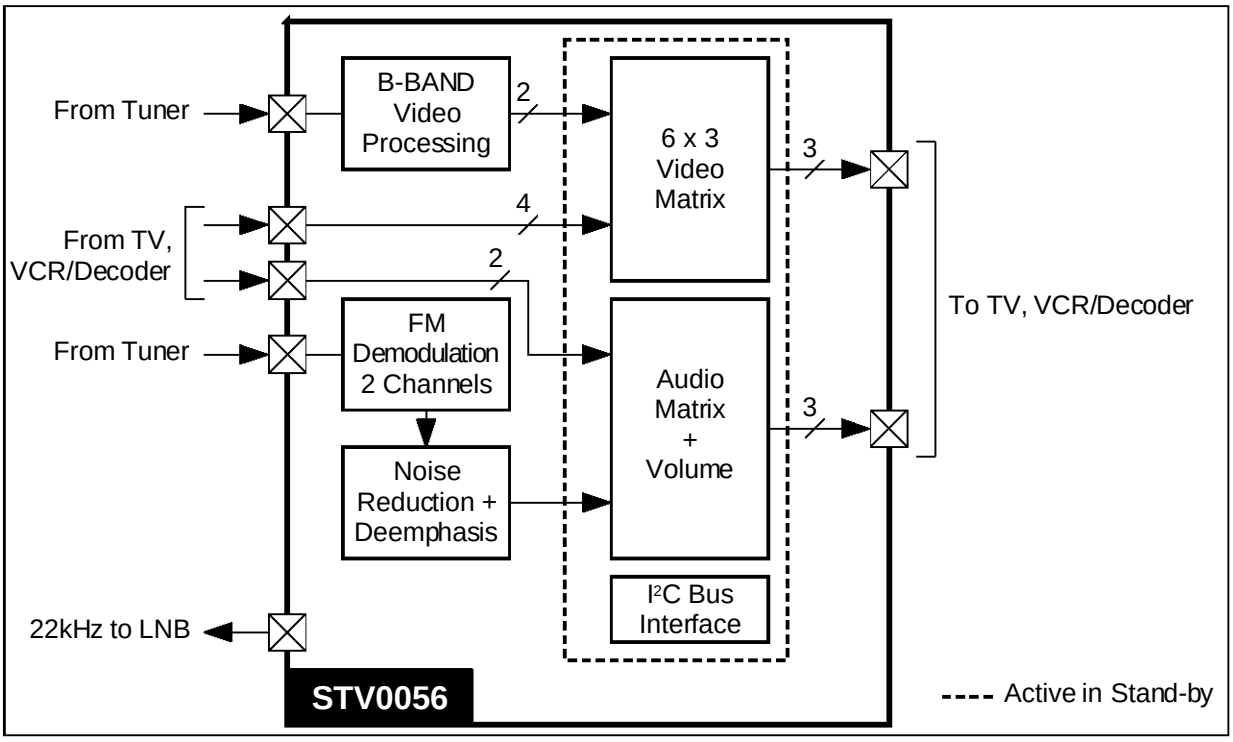
The general block diagram of the STV0042 and STV0056 circuits are given in Figure 1 and 2 respectively.

Figure 1 : STV0042 General Block Diagram



2 - GENERAL BLOCK DIAGRAMS (differences between STV0042 and STV0056) (continued)

Figure 2 : STV0056 General Block Diagram



Both circuits contain the following main functions :

Video :
- a baseband video processing block,
- a video switching matrix,

Audio :
- 2 independant FM demodulators,
- an audio processing part containing (audio de-emphasis, noise reduction),
- an audio switching matrix with a volume control output,

Others :
- an I^2C bus decoder,
- a 22kHz tone generator for LNB control.

When the circuit is in stand-by (R4 B3 = high), all the functions are turned-off except for the I^2C bus interface and the audio and video matrix. With such a configuration, it is still possible to allow signals to go through the satellite receiver while having a lower power consumption.

Differences between STV0042 and STV0056

		STV0042	STV0056	Comments
Video	Clamped Video Inputs	2	4	
	Clamped Video Outputs	2	3	See Note 1
Audio	Audio De-emphasis	50/75µs	50/75µs and J17	
	Audio Noise Reduction	L + R	Panda	See Note 2
	Auxillary Inputs	1	2	
	Auxillary Outputs	1	2	
Others	I^2C Addresses	06	06 or 46	See Note 3
	Digital I/O	No	1	
	22kHz Tone Generator	Pin 13	Pin 16 or/and Pin 29	

Notes : 1. One of STV0056 video output feature a DC level output (black level adjust)

2. With the STV0042 the input signal which is used to control the noise reduction circuit is (L + R). With the STV0056, there are 2 independants noise reduction circuits, one for left, one for right.

3. With the STV0056, the I^2C bus address can be selected by connecting the HA pin either to V_{DD} or to GND.

3 - APPLICATION NOTES

3.1 - Video Processing

Figure 3 and Figure 4 respectively give the architecture of the video processing part of the STV0042 and STV0056 circuits.

Figure 3 : STV0042 Video Processing Block Diagram

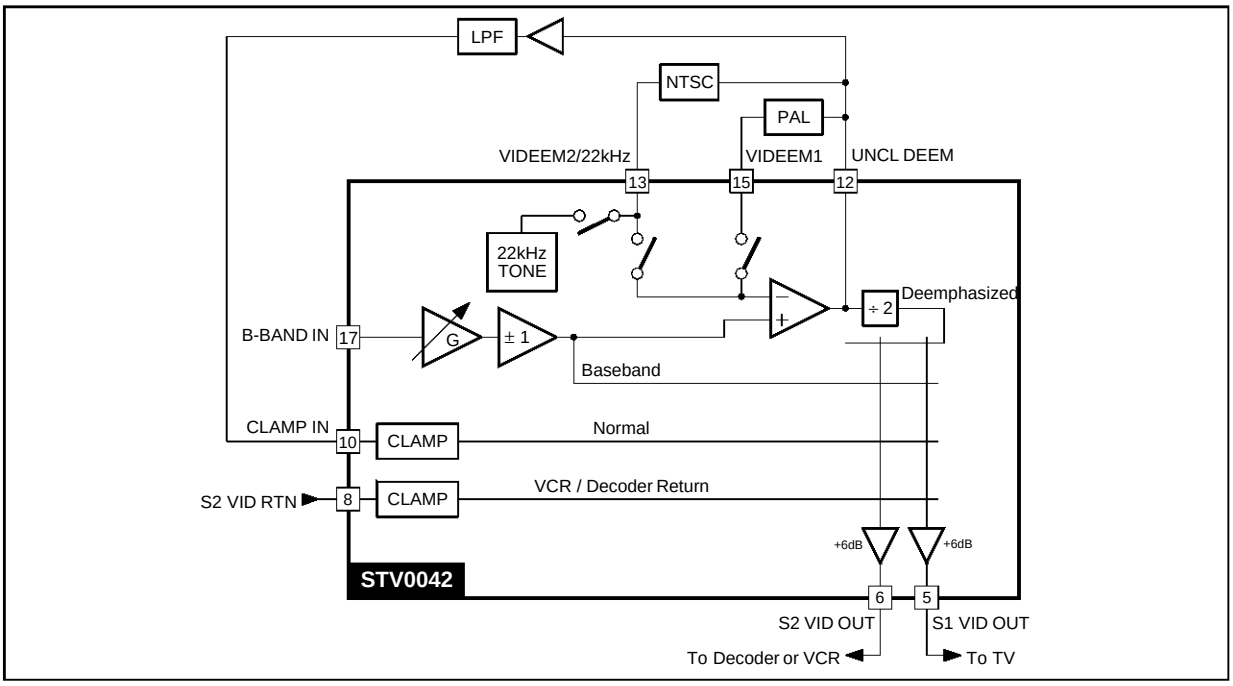
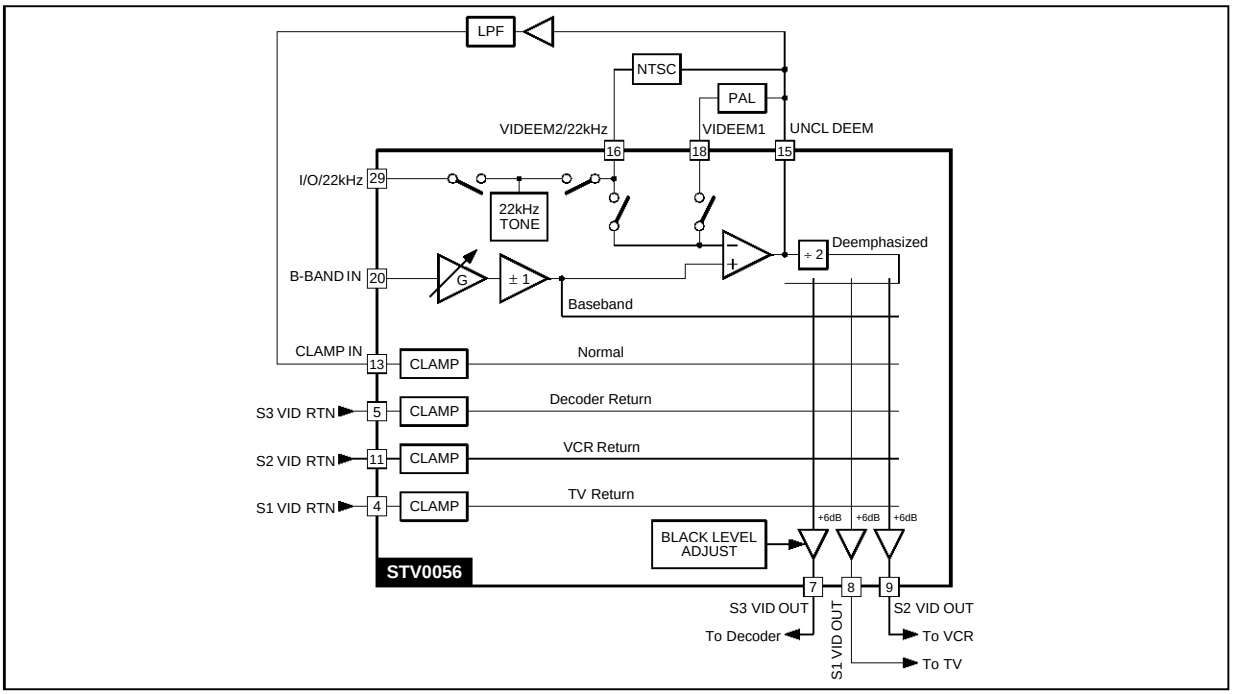


Figure 4 : STV0056 Video Processing Block Diagram



Basically those block diagrams contain two mains parts : the baseband video processing an a switching matrix.

3 - APPLICATION NOTES (continued)

3.1.1 - Breaking down the Baseband Video Processing Function

3.1.1.1 - Input Stage

This wide band input stage has a programmable gain (R1 B0-5).

The gain value is selected to get a $1V_{PP}$ signal at the output (loaded with 75Ω).

Taking into account all the different gains of the video channel (externbal and internal buffers, low pass filters), it corresponds to a $0.4V_{PP}$ signal at the input of the de-emphasis amplifier (synchro top to peak white (not taking into account the pre-emphasis spikes)).

$$G_{Input\ Stage} = \frac{0.4\ V_{PP}}{V_{T\pm W}}$$

$V_{T\text{-}W}$: the synchro top to peak white amplitude of the signal delivered by the tuner.

3.1.1.2 - Video Polarity Inverter

To comply with both positive video (Ku bands) and negative video (C-band) ; a programmable inverter is implemented in the STV42/56 to recover good video phase.

3.1.1.3 - Video De-emphasis + External Low Pass Filter

The video de-emphasis function is realized with a non-inverting amplifier (see Figure 5).

Dimensionning the External Components

The required video de-emphasis law is :

$$F = K \cdot \frac{1 + \frac{f}{f_2}}{1 + \frac{f}{f_1}} \quad f : \text{frequency} \quad (1)$$

in 625 lines systems : $f_2 = 1.56MHz$, $f_1 = 312kHz$
in 525 lines systems : $f_2 = 0.875MHz$, $f_1 = 187kHz$

The AC gain of the structure can be calculated as follow :

$$G_{AC} = 1 + \frac{z_2}{z_1} = 1 + \frac{R_9}{R\,(R_9\,C_{12}\,p + 1)} \quad (2)$$

p : Laplace operator (p : $j2\pi f$ in the frequency field)
R : R11//R10
$|1/C2p| << R11$ for video frequencies

With some calculations, the relation (2) can be presented with the same shape as (1) :

$$(2) \Leftrightarrow (1 + \frac{R_9}{R}) \frac{\left(1 + \frac{R_9\,C_{12}\,p}{(1 + \frac{R_9}{R})}\right)}{(R_9\,C_{12}\,p + 1)} = G_{AC} \quad (3)$$

Comparing (1) and (3)

$$\frac{f_2}{f_1} = 1 + \frac{R_9}{R} \quad (4)$$

$$\text{and } f_1 = \frac{1}{2\,\pi\,R_9\,C_{12}} \quad (5)$$

Additionnaly the DC output voltage of the de-emphasis amplifier is choosen in the range of 3.5 to 4.0V.

This range offers two advantages :

- limits the current consumption when hybrid type of low pass filters are choosen, as suggested in our typical application diagrams (TDK SEL 5618 filter)

$$I_{OUT\ DC} = \frac{V_{OUT\ DC}}{R_{15} + R_{16}}$$

- When the low pass filter is built with discrete components (L and C), there is generally the need for a group delay compensation circuit (see Figure 5) which implements a transistor Q. In such a case, to offer the widest swing, the voltage at the emitter V_E should be :

$$V_E \approx \frac{V_{DD}}{4} \approx 3V, \quad V_E \approx (V_{OUT\ DC} - 0.7V)$$

The DC output voltage of the de-emphasis amplifier is :

$$V_{OUT\ DC} = V_{IN\ DC} \cdot \left(1 + \frac{R_9}{R_{10}}\right) \approx 3.7V \quad (6)$$

with $V_{IN\ DC} = 2.45V$

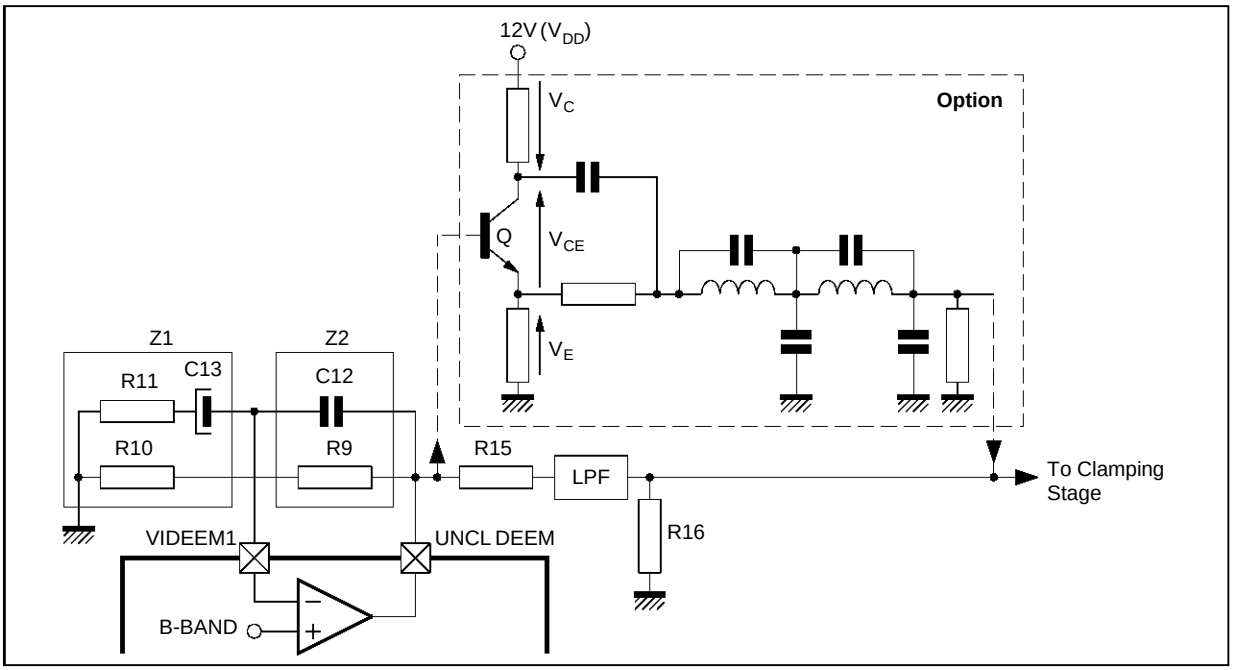
Using relations (4), (5), (6), it is possible to determine all the component values.

- 625 lines systems : (VIDEEM1 Pin)
  R_9 = 5.1kΩ (choosen value)
  ⇒ C_{12} = 100pF, R_{10} = 10kΩ, R_{11} = 1.5kΩ, $C_{13} \geq 10\mu F$
- 525 lines systems (see the PAL/NTSC typical application diagram, Pin VIDEEM2)
  R_{14} = 5.6kΩ (choosen value)
  ⇒ C_{14} = 100pF, R_{13} = 10kΩ, R_{12} = 1.5kΩ, $C_{15} \geq 10\mu F$

Remark :
In order not to be to sensitive to potential crosstalk with the 22kHz tone signal which can be generated from Pin VIDEEM2/22kHz, it is possible to lower the impedance of the de-emphasis network ; for exemple by choosing $R_9 \approx 2.2k\Omega$. In this case, it is required to add a resistor (≈ 2.7kΩ) between the UNCL.DEEM Pin and ground. With $R_9 < 2.2k\Omega$, the power consumption of the de-emphasis amplifier becomes important.

3 - APPLICATION NOTES (continued)

Figure 5 : Video De-emphasis Amplifier



3.1.2 - Breaking down the Video Matrix Section

3.1.2.1 - Clamp Stage

All the video inputs of the video matrix feature the same clamp stage. The purpose of the clamp stage is to reject the energy dispersal ramp and to ensure a stable DC level at all video outputs (easier interface with decoder or text insertion circuits).
The coupling capacitor value is only critical for the rejection of the energy dispersal ramp (C11 in the application diagram).
The principle of the clamp stage is : DC alignment of the synchronization top bottom level. The coupling capacitor C_{11} is charged with a high current I_2 when the input level is lower than 2.7V and is permanently discharged by a small I_1 current (see Figure 6).

Dimensionning the Coupling Capacitor C_{11}

C_{11} is dimensionned for the largest ramp amplitude A_R which can be measured at the output of the low pass filter :

$$A_{R\ max.} = \frac{A \cdot G \cdot G_{DEEM}}{2}$$

A : amplitude of the ramp at the tuner output
G : gain of the input stage
GDEEM : gain of the de-emphasis amplifier (at 25 or 30Hz)

This worst case of the ramp produces a positive or negative voltage offset Δ at each line :

$$\Delta = \frac{A_{Rmax.}}{312.5}\ (625\ lines)\ \text{or}\ \Delta = \frac{A_{Rmax.}}{262.5}\ (525\ lines)$$

To reject the Slope :
The I_1 current must produce a negative ramp in C_{11} which compensate the positive ramp of the energy dispersal sawtooth :

$$C_{11} \leq \frac{I_{1\ Min.}}{\Delta_{Max.}} \cdot T \qquad (1)$$

Additionnaly the I_2 current of the circuit is choosen to produces enough charge during the synchro pulse of the negative slopes of the energy dispersal ramp.

$$I_{2\ Min.} \geq \frac{C_{11} \cdot \Delta + I_1 \cdot T}{T_S} \qquad (2)$$

Results :
For a worst case of a 4MHz pp ramp added to a 16MHz/V channel

$$A_{RMax.} = 1.25V_{PP} \Rightarrow \Delta_{Max.} = 4.0mV$$

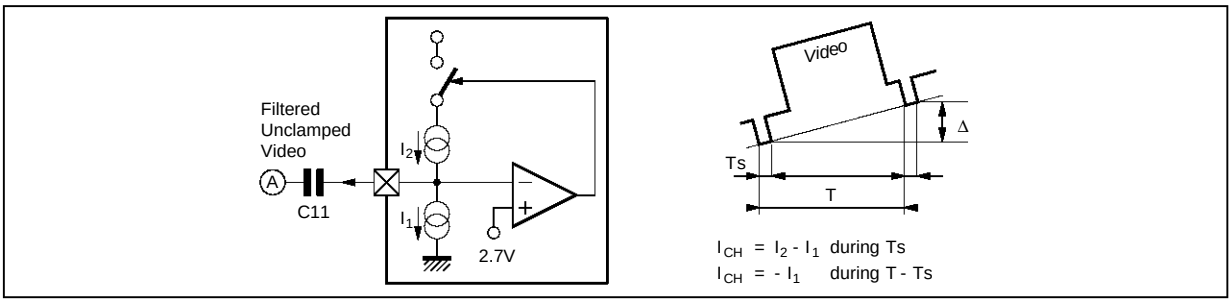
$$(1) \Rightarrow C_{11} \leq \frac{0.5\mu A}{4mV},\ C_{11} \approx 8.2nF$$

(2) $\Rightarrow$ Required $I_{2\ Min.} > 28\mu A$,
Actual $I_{2\ Min.} = 40\mu A$
(specification of STV42/56)

Remarks :
- It is important not to use a too small C_{11} value. A low C_{11} value would induce a degradation of the TILT parameter (parasitic slope on the clamped video). Additionnaly, in case of built-in Videocrypt receiver, a parasitic slope would produce a voltage offset at the "cut and rotate" point.
- For a good operation, the DC impedance of point **A** (see Figure 6) must be as low as possible.

3 - APPLICATION NOTES (continued)

Figure 6 : Video Input Clamp Function



3.1.2.2 - Switching Matrix

This switching matrix is simply an array of CMOS switches which is driven by registers. All configurations are possible. Any output can be connected to any input. An input can be connected to several outputs.

3.1.2.3 - Output Stages

Each video output has a 6dB output gain, and the internal final stage is a emitter follower structure pulled down with a 1.3mA current source.

The output voltage amplitude is $2V_{PP}$, and the synchro bottom level is clamped at 1.3V typically.

In the application, an external current amplifier (75Ω driver) is required.

Remarks :

- The S3VIDOUT of the STV0056 features a black level adjust (corresponding to a DC level adjust). This function may be used to more simply interface with built-in Videocrypt decoder.
- When the high 2 low power mode is selected, the output impedance becomes high (≈ 23kΩ typ.), and the DC output levels drops to low values (< 0.2V) consequently the external 75Ω driver is also turned (power saving).

3.2 - FM Demodulation

3.2.1 - Hardware Description

This chapter is relevant to :

- the input filter,
- a study of the FM demodulator which is integrated in the STV42/56 circuits (including the external components needed at Pins DET L/R, AMPLOCK L/R, CPUMP L/R, AGC L/R).

3.2.1.1 - Input Filter (C25, R18, R17, L4, C24, C23)

The FM demodulator integrated in the STV42/56 circuit have a good rejection of the video signal (due to the selective AGC stage see paragraph 3.2.1.2). However, to get a good audio signal to noise ratio, it is preferable to attenuate the video signal spectrum with an input filter.

The filter proposed in the typical application (see Figure 7) contains a high pass cell (C_{25}, R_{18}, $f_C \approx 1.5$MHz) and a chroma trap (R_{17}, L_4, C_{24}).

C_{23} is required for capacitive coupling with the FM IN Pin (C_{23} value is not critical).

The center frequency of the chroma trap is about 4.4MHz for PAL/SECAM application and 3.58MHz in case of NTSC application (Remark : In case of PAL/NTSC application, a double trap may be required.)

It is recommanded to directly connect the input filter to the tuner baseband output, because at this stage the video signal is still emphazed (giving a natural 14dB attenuation of the lower part of the video spectrum where most of the energy is concentrated.

3.2.1.2 - FM Demodulators

The block diagram of the FM demodulation part is given in Figure 8. This block diagram contains 2 independants FM demodulators able to process all types of mono and stereo sound, including :

- mono signals with deviation from ± 30kHz up to ± 400kHz (remark the spec mentions : ± 19.5kHz to ± 592kHz, in order to cover all possible dispersions).
- Stereo pair featuring a frequency spacing different from 180kHz (between left and right sub-carriers).

Each FM demodulator section contains 2 parts :

- an automatically gain controlled input stage
- a PLL demodulator

The only common point to both FM demodulators is the frequency synthesis circuit : SYNTHESIZER.

The structure of the FM demodulators which is different from conventional solutions have been selected for the two following reasons :

- no need for costly selective filters (LC or ceramic),
- to have a variable bandwidth (to accomodate all type of deviations).

3 - APPLICATION NOTES (continued)

Figure 7 : FM Demodulation, Video Signal Rejection Filter

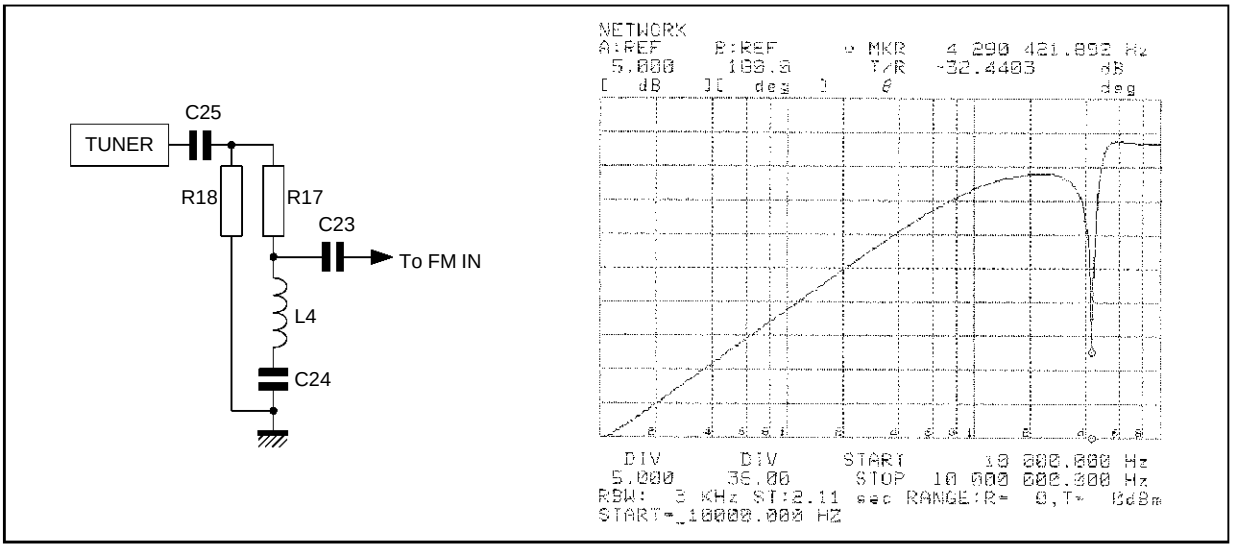
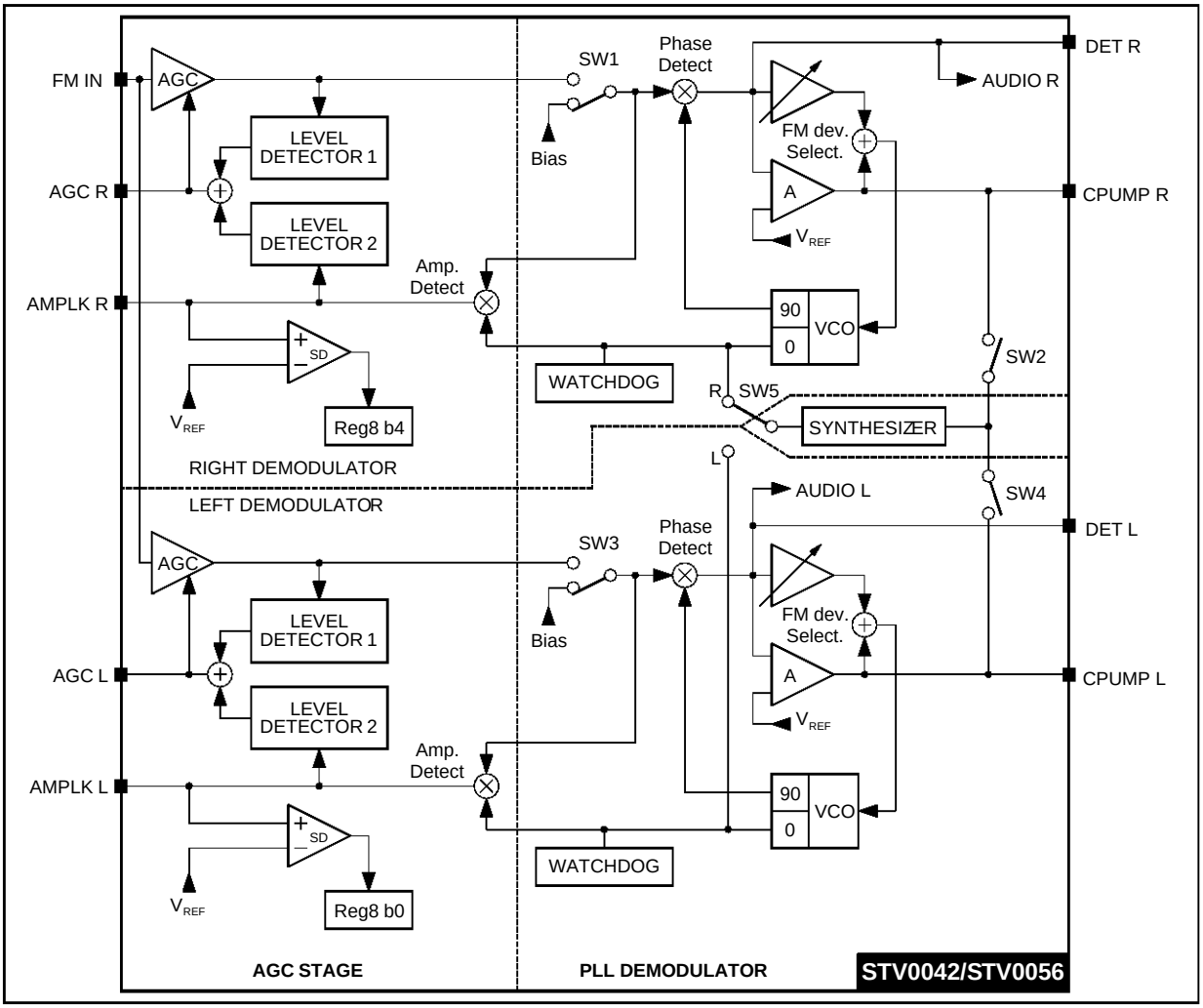


Figure 8 : FM Demodulation Block Diagram



3 - APPLICATION NOTES (continued)

a) Principle of the FM Demodulators

To properly operate the FM demodulators require to go through different operating modes before to produce the demodulated signal. The required sequence is described in the software part (Section 3.2.2.1).

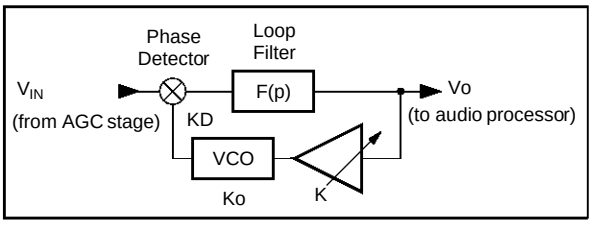
Because there is no selective filter (LC or ceramic) which sets the operating frequency (ex : 10.7MHz), the demodulation of the STV42/56 circuit directly operates at the subcarrier frequency (ex : f_{VCO} = 7.02MHz when demodulating the 7.02MHz subcarrier). This first point explains why each VCO can be driven by the Synthesizer.

- SW2 closed and SW5 to R to drive the right VCO
- SW4 closed and SW5 to L to drive the left VCO

During the Demodulation :

When the FM demodulator is in demodulation, it operates like any PLL demodulator and its block diagram can be simplified (as Figure 9).

Figure 9



F(p) : the transfert function of the external loop filter which is connected at DET Pin.

KD : the phase detector gain (in V/radians).

KO : slope of the voltage controlled oscillator (VCO) in (radians/volts or Hz/volts).

K : is a programmable coefficient related to the register 05 bits 0 to 5.

In Annex 1 a more detailed study of this PLL structure is provided. Out of this detailed study the key results are :

$$KO : 460kHz/V \Leftrightarrow 2.89 \cdot 10^6 \text{ radians/V (typ.)}$$

$$KD \approx DETH \cdot \frac{R_{33}}{R_{36}} \text{ (for left channel)} \quad (0)$$

DETH is a parameter given in the specification.

$$\text{Lock range} = \omega_L = KO \cdot K \cdot KD \quad (1)$$

$$\text{DC gain} = \frac{V_{O\,PP}}{(\text{deviation})_{PP}} = \frac{1}{K \cdot KO} \quad (2)$$

Remarks about those relations :

- The relations (1) shows that a programmable K coefficient corresponds to a programmable bandwidth (FM deviation selection, table in Page 26 of the specification dated June 1995).
- In the satellite receiver applications it is asked to have a required audio level for a full deviation signal (ex : $1V_{RMS}$ on the scart output at full deviation). Refering to relation (2), it means that the K · KO products must remain constant for all deviations.
  Consequently to compensate the dispersion of the VCO slope KO, the STV42/56 FM deviation selection table offers many steps, so that there is always a selection which guarantees :
  K · KO = constant ± small dispersion
  The method to select the optimum K factor is described in Section 3.2.2.3
- Additionnally, in relation (1), it can be noticed that a constant (K · KO) product gives a more stable lock range.

b) Breaking Down the PLL Demodulator Section

(explanation for left channel and refered to Fig. 8)

- *Phase Detector :*
  This part converts the phase difference between the wanted subcarrier and the VCO signal (with 90° phase log) into a current I_{PD}. In the calculation KD is given in Volt per Radians, because a current to voltage conversion is done by the resistor R_{33} connected between Pin DET and V_{REF}.
- *The Loop Filter :*
  It is made of external components connected between DET Pin and V_{REF}.
- *The VCO :*
  The voltage controlled oscillator typically has a 460kHz/volt slope. It is driven by the SYNTHESIZER during the frequency synthesis sequence and by the demodulated signal during the demodulation.
  The VCO part features a first output with 90° phase lag compared with the subcarrier, this output is used for phase detection ; the second output is in phase with the subcarrier and is used for synchronous amplitude detection (see AGC stage).
- *The Watchdog :*
  It is used to measure the VCO frequency. This function is used to check if the VCO frequency has reached the wanted subcarrier frequency during the frequency synthesis. This operation is also usefull to monitor the VCO frequency during demodulation (preventing it from shifting away when operating under abnormal conditions). The watchdog is a 1/1000 divider (clocked by a 10kHz reference frequency) consequently its averages the VCO frequency over a 100ms period (equivalent to 10Hz) ; this long period makes the results independant from the audio modulating signal.

3 - APPLICATION NOTES (continued)

- *FM Deviation Selection :*
  This part is a programmable attenuator driven by R5 B0-5.
- *SW3-SW4-SW5 :*
  Those switches are used to drive the VCO either by the Synthesizer or by the wanted subcarrier.
  During the synthesis SW4 is closed, SW5 is set to L, and SW3 is connected to bias (in order not to have parasitic drives coming from the phase detector).
  Those switches are driven by the R06 B2 B4 (left), R06 B2 B5 (right).
- *Amplifier A and CPUMP Pin :*
  During the demodulation, the DC voltage corresponding to the VCO center frequency is memorized in a large capacitor (about 10µF) connected at CPUMP Pins.
  To prevent the VCO from slow frequency shifts which could be generated by current leakages, the PLL demodulator has a DC loop which is closed by a voltage to current amplifier A.
  The output current capability of this amplifier is low (max. ± 2µA) in order not to disturb the AC operation of the amplifier.

c) Why an AGC Input Stage

When no selective filter (LC or ceramic) is used, the sum of all the subcarriers is input in the phase detector of the PLL demodulator.

Consequently a linear type of phase detector is necessary (to avoid intermodulations) ; but this type of phase detector features a gain which is proportionnal to the amplitude (As) of the subcarrier to be demodulated.

$$KD = \alpha \cdot As \quad (3)$$

Refering to the relation (1), the lock range of the PLL demodulator :

$$\omega_L = KO \cdot K \cdot KD = KO \cdot K \cdot \alpha \cdot As$$

Consequently in order to have a stable lock range, it is important to maintain a constant amplitude of the wanted subcarrier ; then an automatically gain controlled stage is required.

d) Breaking Down the AGC Stage

- The AGC amplifier is controlled by two level detectors, and offers a 40dB gain range.
- The first control loop built with the AGC stage and the level detector 1, is always active (during the synthesis and the demodulation). This loop guarantees that the amplitude (As) of the wanted subcarrier does not take too small or too high values. In doing so, the first capture is easier when starting to demodulate.
- The second loop made of : the amplitude detector, level detector 2 and the AGC stage, is active only during demodulation (SW3 connected to AGC amplifier).
  When operating, thanks to the higher current capability of level detector 2, the second loop controls the AGC amplifier.
  After the PLL capture, the amplitude detector receives all the subcarriers on one input and the VCO signal at the other input. Due to the PLL the VCO signal is synchronous with the wanted subcarrier ; consequently the average DC signal which can be measured at AMPLOCK Pin only depends on the amplitude of the wanted subcarrier (regardless the amplitude and the number of the other subcarriers).
  Finally with this second loop the amplitude of the wanted subcarrier is constant at the input of the phase detector.
  An external RD filter is used on the AMPLOCK Pin to reject all the AC components of the amplitude detector output signal.
- SD comparator : This Subcarrier Detector comparator switches to high when the AMPLOCK voltage exceeds a fixed threshold. In doing so it detects wether a subcarrier is present at the wanted frequency.

e) Synthesizer

This function is shared between both FM demodulators. For this reason, when demodulating a stereo pair, two successive frequency synthesis sequences are required.

The synthesizer used a conventional PLL solution, in which the VCO signal frequency is divided by a programmable N factor, and the frequency divided signal is compared in phase with a precise frequency reference (10kHz) derived from the crystal oscillator). The output of the phase detector is a current which charges or discharges the external CPUMP capacitor, so that the VCO frequency converges to the required frequency. The average charge current (when f_{VCO} is quite different from the wanted frequency) is about 60µA. Consequently the tuning speed is about

$$\frac{\Delta f_{VCO}}{\Delta t} \approx 10.5\text{MHz/second } (C_{41} = 10\mu F)$$

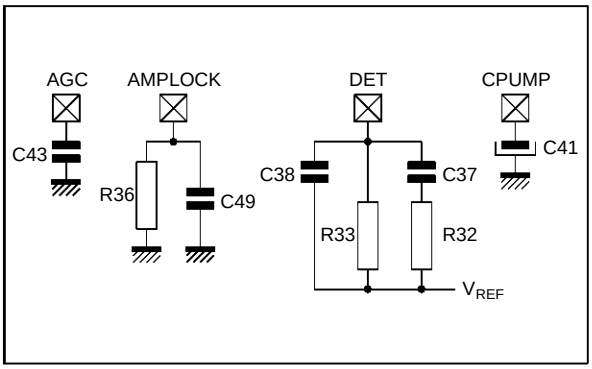
Important Remark :
Due to its loop gain the frequency synthesizer has a ± 10kHz accuracy.

3 - APPLICATION NOTES (continued)

f) Dimensioning the External Components
(DET, AMPLOCK, AGC, CPUMP Pins)

Example : Left channel (see Figure 10).

Figure 10 : Left Channel, FM Demodulator External Components



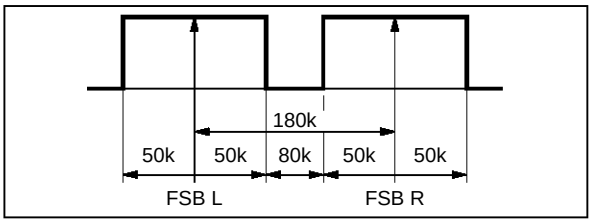
- AMPLOCK, AGC Pins :
  Due to the AGC loop, the amplitude As of the wanted subcarrier at the phase detector input is inversely proportionnal to the external resistor connected to AMPPLOCK.

$$(As)_{PP} \approx \pi \cdot DETH \cdot \frac{11k\Omega}{R_{36}}$$

  In order to maintain the phase detector in a linear operation (even in case of a high number of subcarrier : 10 subcarriers), we recommand (As) not to exeed 0.25V_{PP}.
  For R_{36} = 560kΩ, $AS_{PP} \approx 0.19\ V_{PP}$.
  The C_{49} capacitor associated with R_{36} realizes a filter which rejects all the AC components. For a good operation, the roll-off frequency of this filter is lower than the audio spectrum for C_{49} = 100nF, $f_C \approx 2.8$MHz.
  The value of the AGC capacitor C_{43} is not very critical, 100nF has been selected for component standardization. However it is recommanded to have $C_{43} < 1\mu F$ for a good stability of the loop.
- CPUMP Pin :
  Choosing the CPUMP capacitor value results from a compromisze. The smaller is CPUMP the shorter is the duration of the frequency synthesis, but a too small value of CPUMP induces a too fast response of the DC compensating loop (risk of distorsion in the low frequency audio signals).
  $C_{41} = 10\mu F$ is a good compromise.
- DET Pins :
  following is a simplified method to calculate the components.

The most severe case is : "narrow band stereo pair" when simultaneously are required a good quality sound and a precise control of the capture range (due to the low frequency spacing : 180kHz (80kHz dynamically)).

Figure 11 : Stereo Pair, Frequency Spacing and Coverage



Theoretical request : $\omega_L > 50$kHz, $\omega_C < 80$kHz.
Actually a more severe compromise is required.

- $\omega_L > 70$kHz. A first margin is required to compensate the phase lag which appears in case of high frequency slew rates (case of audio sibilance). In practice, a further margin is given to compensate the dispersion of the phase detector gain, eventually :

$$90kHz \leq \omega_L \text{ typ.} \leq 100kHz$$

- ω_C will be choosen as low as possible to also compensate potential level imbalance between left and right subcarriers (2 to 3dB max. could be measured on some broadcasted channels).

The STV42/56 circuits have been optimized to get a 1V_{PP} at the DET Pin (full deviation).

Refering to realation (2) :

$$K \cdot KO = \frac{100kHz}{1V_{PP}}_{PP} = 100kHz/V$$

choosing ω_L = 100kHz in (1) :

$$KD = \frac{\omega_L}{K \cdot KO} \approx 1V/rd$$

using relation (0) :

$$R_{33} = \frac{KD}{DETH} \cdot R_{36} \approx 180k\Omega,$$

$$DETH = 3.1V, R_{36} = 560k\Omega$$

To calculate the other components C_{37}, R_{32}, would lead to complex mathematics. A first estimate can be done using the relations given in Annex 1.
Some experiments and calculations have given R_{32} = 82kΩ and C_{37} = 22pF, corresponding capture range is about 52kHz.
An additionnal capacitor C_{38} is recommanded to give a further reduction to the capture range ($C_{38} \approx$ 15 to 22pF).

3 - APPLICATION NOTES (continued)

3.2.2 - Software Description

To properly use the FM demodulators of the STV42/56, specific software routines need to be implemented.

This section describes three software routines :
- FM demodulation,
- PLL monitoring,
- PLL gain auto calibration.

Remark :
In this section some solutions are given, but the software engineer may improve them for his application.

3.2.2.1 - FM Demodulation Software Routine

As far as the FM demodulation is concerned, there are two main cases : mono and stereo pair.
In case of mono subcarriers, it is suggested to have both left and right demodulators demodulating the same wanted sub-carrier (in doing so, signals can be surely provided to the decoders).
In case of stereo pair, naturally the two demodulators work on different subcarriers.

Description (Flow Chart in Figure 12)

With the STV0042/STV0056 circuits, for each channel, three steps are required to acheive a FM demodulation :
- 1st step :To set the demodulation parameters :
  - A : FM deviation selection,
  - B : Subcarrier frequency selection.
- 2nd step : To implement a waiting loop to check the actual VCO frequency.
- 3rd step :To close the demodulation phase locked loop (PLL).

Refering to the FM demodulation block diagram (see Figure 8), the frequency synthesis block is common to both channels (left and right) ; consequently two complete sequences have to be done one after the other when demodulating stereo pairs.
For clarity, the explanations are based on the following example : stereo pair 7.02MHz/L 7.20MHz/R, deviation ±50kHz max.

1st Step (left) :
SETTING THE DEMODULATION PARAMETERS

A. The FM deviation is selected by loading R5 with the appropriate value (see Table 1).

Table 1 : Register 5 (FM Deviation Selection)

4	3	2	1	0	Selected Nominal Carrier Modulation	
					Bit 5 = 0	**Bit 5 = 1**
0	0	0	0	0	Do not use	cal : do not use = 0.3373V offset on VCO
0	0	0	0	1	Do not use	cal : do not use = 0.3053V offset on VCO
0	0	0	1	0	Do not use	cal : do not use = 0.2763V offset on VCO
0	**0**	**0**	**1**	**1**	Cal. set. (2V)	**calibration setting (1V offset on VCO)**
0	0	1	0	0	592kHz	296kHz modulation
0	0	1	0	1	534kHz	267kHz modulation
0	0	1	1	0	484kHz	242kHz
0	0	1	1	1	436kHz	218kHz
0	1	0	0	0	396kHz	198kHz
0	1	0	0	1	358kHz	179kHz
0	1	0	1	0	322kHz	161kHz
0	1	0	1	1	292kHz	146kHz
0	1	1	0	0	266kHz	133kHz
0	1	1	0	1	240kHz	120kHz
0	1	1	1	0	218kHz	109kHz
0	1	1	1	1	196kHz	98.3kHz
1	0	0	0	0	179kHz	89.7kHz
1	0	0	0	1	161kHz	80.9kHz
1	0	0	1	0	146kHz	73.1kHz
1	0	0	1	1	122kHz	66.0kHz
1	0	1	0	0	120kHz	60.0kHz
1	**0**	**1**	**0**	**1**	109kHz	**54.4kHz = default power up state**
1	0	1	1	0	98kHz	49.1kHz
1	0	1	1	1	89kHz	44.3kHz
1	1	0	0	0	78kHz	39.8kHz
1	1	0	0	1	71kHz	35.9kHz
1	1	0	1	0	65kHz	32.4kHz
1	1	0	1	1	58kHz	29.1kHz
1	1	1	0	0	53kHz	26.7kHz
1	1	1	0	1	48.6kHz	24.3kHz
1	1	1	1	0	43.8kHz	21.9kHz
1	1	1	1	1	39.6kHz	19.7kHz

Corresponding bandwidth can be calculated as follows :
Bw ≈ 2 (FM deviation + audio bandwidth)
Bw ≈ 2 (value given in table + audio bandwidth)

In the example : ± 50kHz

R5	Bits	7	6	5	4	3	2	1	0
		X	X	1	1	0	1	1	0

3 - APPLICATION NOTES (continued)

B. The subcarrier frequency is selected by launching a frequency synthesis (the VCO is driven to the wanted frequency). This operation requires two actions :

- To connect the VCO to the frequency synthesis loop. Refering to the FM demodulator block diagram (see Figure 8) :
  - SW4 closed ⇒ R6 B2 = H
  - SW3 to bias ⇒ R6 B4 = L
  - SW2 to bias ⇒ R6 B3 = L
  - SW1 opened ⇒ R6 B5 = L
- To load R7 and R6 B6 B7 with the value corresponding to the left channel frequency. This 10 bits value is calculated as follows :
  Subcarrier frequency = coded value x 10kHz
  (10kHz is the minimum step of the frequency synthesis function)
  Considering that the tunning range is comprised between 5 to 10MHz, the coded value is a number between 500 and 1000 (2^{10} = 1024) then 10 bits are required.
  Example :
  7.02MHz = 702 x 10kHz
  702 ⇒ 1010 1111 10 ⇒ AF + 10
  R7 is loaded with AF and R6 B6 : L, R6 B7 : H.

The Table 2 gives the setting for the most common subcarrier frequencies.

2nd Step (left) :
VCO Frequency Checking (VCO)

This second step is actually a waiting loop in which the actual running frequency of the VCO is measured.
To exit of this loop is allowed when : Subcarrier Frequency - 20kHz ≤ Measured Frequency ≤ Subcarrier Frequency + 20kHz (± 10kHz is the maximum dispersion of the frequency synthesis function).
In practice, R8 B2 B3 and R9 are read and compared to the value loaded in R6 B6 B7 and R7 ±2 bits.

3rd Step (left)

The FM demodulation can be started by connecting the VCO to the phase locked loop (PLL).

In practice :
- SW3 closed ⇒ R6 B4 = H
- SW4 opened ⇒ R6 B2 = L

After this sequence of 3 steps for left channel, a similar sequence is needed for the right channel.

Note :
In the sequence for the right, there is no need to again select the FM deviation (once is enough for the pair).

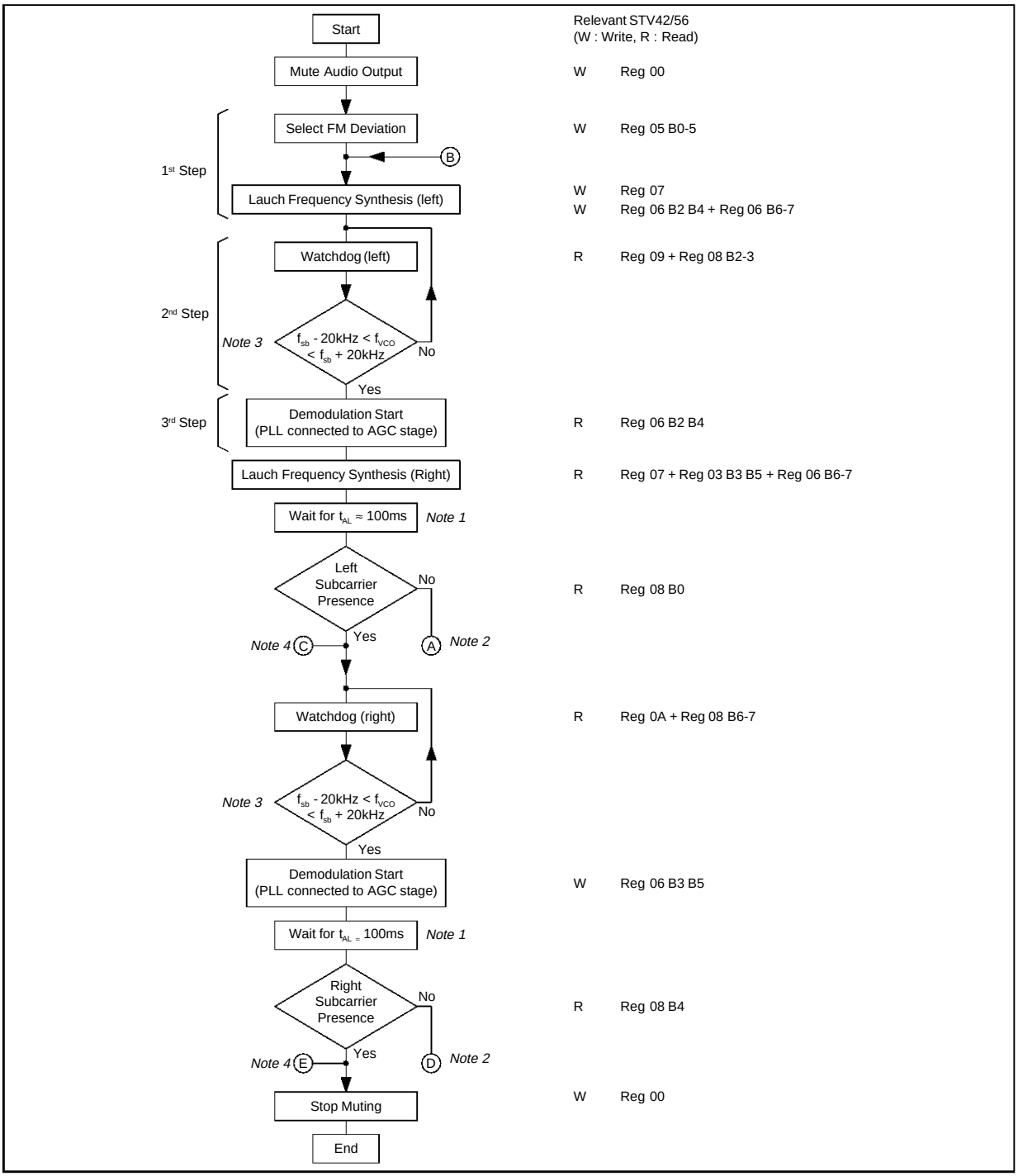
General Remark
Before to enable the demodulated signal to the audio output, it is recommanded to keep the audio muting and to check whether a subcarrier is present at the wanted frequency. Such an information is available in R8 B0 and R8 B4 which can be read.

Table 2 : Frequency Synthesis Register Setting for the Most Common Subcarrier Frequencies

Subcarrier Frequency (MHz)	Register 7 (Hex)	Register 6	
		Bit 7	Bit 6
5.58	8B	1	0
5.76	90	0	0
5.8	91	0	0
5.94	94	1	0
6.2	9B	0	0
6.3	9D	1	0
6.4	A0	0	0
6.48	A2	0	0
6.5	A2	1	0
6.6	A5	0	0
6.65	A6	0	1
6.8	AA	0	0
6.85	AB	0	1
7.02	AF	1	0
7.20	B4	0	0
7.25	B5	0	1
7.38	B8	1	0
7.56	BD	0	0
7.74	C1	1	0
7.85	C4	0	1
7.92	C6	0	0
8.2	CD	0	0
8.65	D8	0	1

3 - APPLICATION NOTES (continued)

Figure 12 : FM Demodulation Software routine Flow Chart



Notes : 1. t_{AL} must be longer than the setting time of the voltage at AMPLOCK Pins. t_{AL} can be reduced by decreasing the AMPLOCK capacitor.

2. In points **A** and **D** different strategies may be adopted (up to the software engineer).
   Suggestion : to return to **B** point and to have a second trial. If this second trial is not successfull, to run till end ; in this case a randoom noise is output and the end user is warned about the subcarrier "abscence".

3. The frequency synthesis has a ± 10kHz accuracy. But in order to give some more margin ± 20kHz tolerance may be used (this tolerance remains lower than the capture range of the PLL).

4. In point **C**, two different strategies may be adapted :
   - either to keep muted the output till the MCU runs till **E** point,
   - or to output the left sound on both outputs untill the MCU runs to **E** point, and real stereo sound is output after **E** point.

3 - APPLICATION NOTES (continued)

3.2.2.2 - PPL Monitoring Software Routine

During the demodulation, the VCO is locked on the wouted subcarrier frequency. If for any reason the subcarrier desappears (signal drop out, unreliable cable connection to the parabola ...) the VCO is no larger locked on a fixed frequency, it may drift away and may lock on unwanted subcarriers when the RF signal appears again.
To prevent the application from tese problems, it is recommanded to implement PLL monitoring routine.

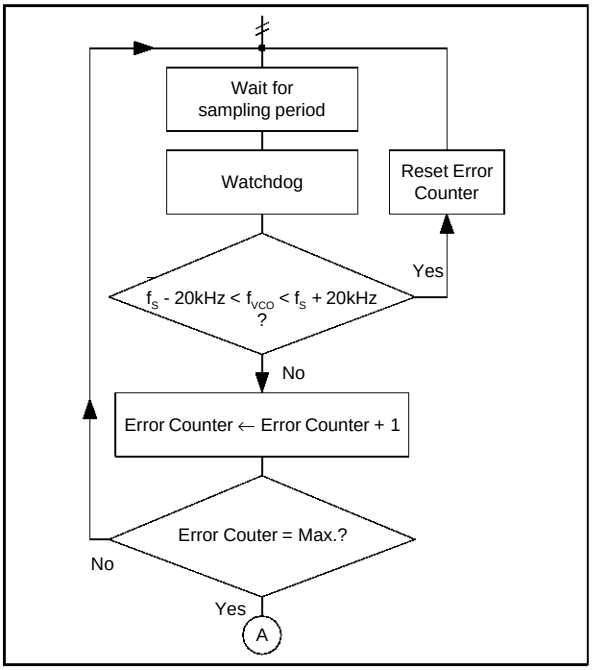
Description

To regularly and permanently check the VCO frequency (using) the watchdog). The sampling period may be in the range of 200ms to 500ms.
When an error is detected, the demodulation is not imediatly stopped but an error counter is initialized. If at the next sampling of the watchdog, there is a new error, the error counter is incremented.
The demodulation is stopped when the error counter reaches a fixed value (for instance 4 or 5).
If one sampling of the watchdog gives a good esult before the error counter reaches the limit, the error counter is reset.

Flow Chart

This function has no real start sequence, because it permanently operates (see Figure 13).
In Point A, it is suggested to restart the FM demodulation sequence.

Figure 13 : PLL Monitoring Routine : Flow Chart



3.2.2.3 - PLL Calibration Function

a - Reason for the Calibration

In order to have a good and stable quality of the sound, it is important to precisely control the PLL bandwidth (stable lock and capture ranges of the PLL).

Refering to the general theory of the PLLs, the lock range can be calculated as following (also valid for the STV42/56 circuits) :

$$\omega_L = KO \cdot K \cdot KD \quad (1)$$

where :

KO : the VCO slope (in rd/V or kHz/V),
KD : the phase detector gain (in V per Rd),
K : a constant (in the case of STV42/56, this parameter is programmable in order to accomodate different FM deviations : Reg 5 B0-5).

In the case of the STV42/56, most of the dispersions come from the KO (VCO slope), in theory dispersions as high as ± 30 to ± 40% could be expected. In order to compensate this problems the STV42/56 circuits feature many PLL gain positions (K factor).
In order to find the optimum K factor (Reg 5 B0-5) there are two methods :

a.1 - To implement a test in the assembly line

This test can be described as following :
- A full deviation FM signal is input to the STV42/56 circuit.
- The STV42/56 is set to demodulation.
- The peak-to-peak signal is measured on the DET Pins or on the scart outputs (in this later case no de-emphasis and no noise reduction are preferable).
- Then with either an automatic system or with the help of an operator, the optimum K parameter is selected to get a $1V_{PP}$ signal on the DET Pins or $2V_{PP}$ at the scart outputs.
- The result of this test is memorized in the EEPROM of the receiver (remark : to save time the test can be done for only one deviation and its result can be used for all deviations accomodated by the receiver).

a.2 - To use the auto-calibration function of the STV42/56 circuits

This second method will actually be a software routine which is embeded in the microcontroller software.

This second method has two advantages :
- no need for test in the assembly line (time saving, equipment saving),
- the receiver can auto-calibrate during its life, then compensating drifts related to time and temperature.

3 - APPLICATION NOTES (continued)

b - Principle of the Auto-calibration Function (see Figures 14 and 15)

The purpose of the auto-calibration function is to automatically measure the slope of the VCO of the PLL. This can be done with the STV42/56 circuits when using the following software routine :

1st step : To implement a synthesis to bring the VCO to a known frequency (F_o) (ex : 7.02MHz).

2nd step : To use a frequency watchdog sequence to check whether the VCO has reached the wanted F_o frequency.

3rd step : To generate a well known voltage increase ΔV in the drive of the VCO (this function can be done with the autocalibration setting of the STV42/56 circuits (Reg 05 loaded with value 03 or 23)).
ΔV = 1V for Reg 05 : 23
ΔV = 2V for Reg 05 : 03

4th step : After a well known delay, the new frequency (Fe) reached by the VCO is measured with the frequency watchdog function.
Remark : The delay to be given must be higher than sampling period of the watchdog (100ms). And since the internal timing of the watchdog is not known, we think that the optimum delay is 200ms.

With all above steps, the VCO slope can be calculated as follows : $KO \approx \frac{F_e \pm F_o}{\Delta V}$

Figure 14 : PLL Demodulator, Auto-calibration Function

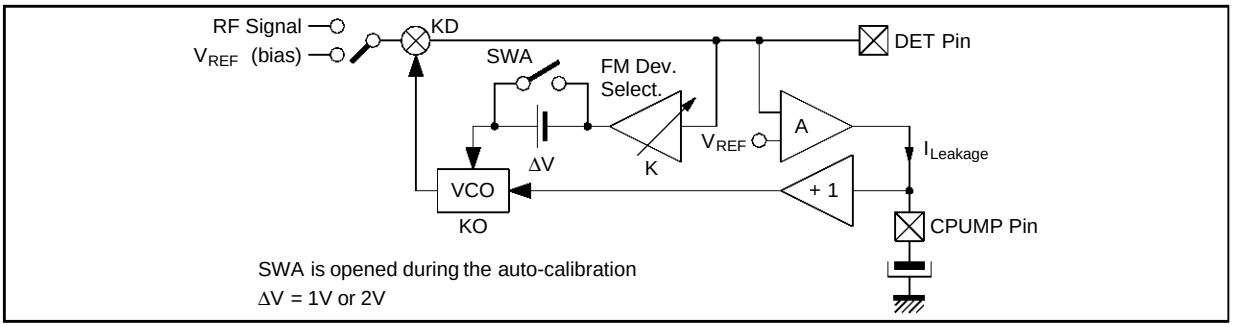
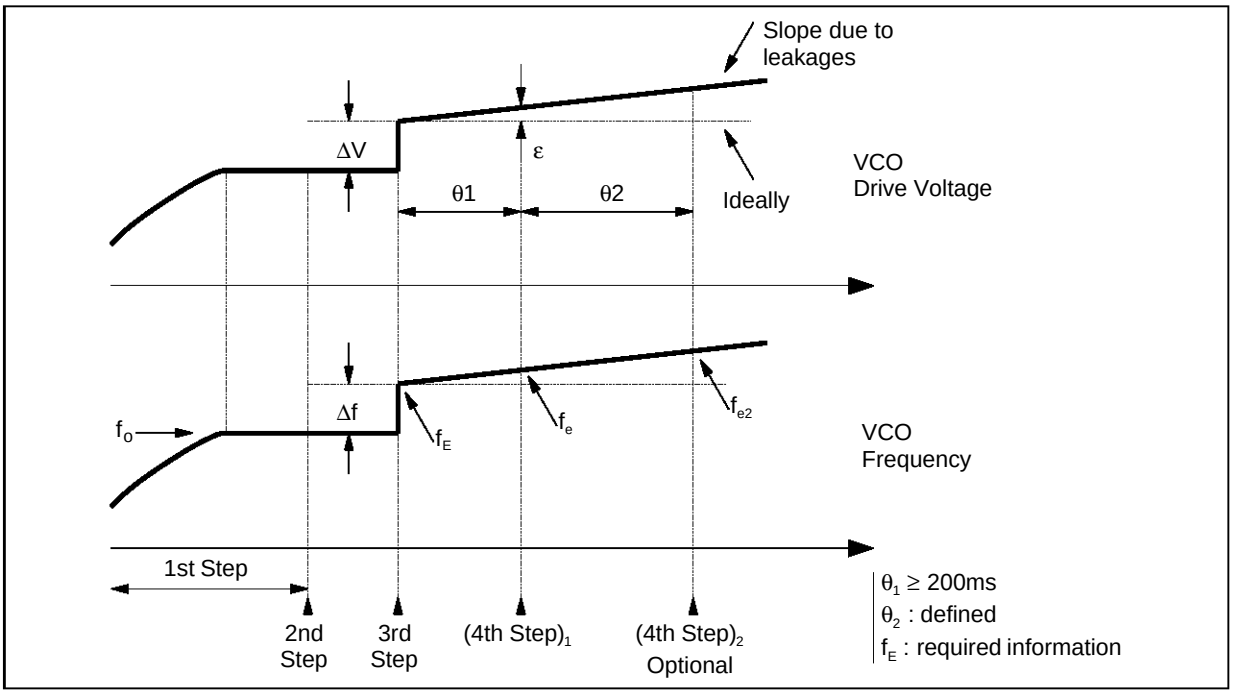


Figure 15 : Auto-calibration Timing, Diagram of the Potential Drifts



3 - APPLICATION NOTES (continued)

c - How to Use the Results of the Auto-calibration Routine

Let us keep in mind that the final objective is to get a PLL gain or a lock range as close as possible to its optimum value.

Coming back to relation (1) :

$$\omega_L = KO_{Typ.} \cdot K_{table} \cdot KD = KO_{act} \cdot K_{corrected} \cdot K$$

$KO_{Typ.}$: is the VCO slope when there is no dispersion.
K_{table} : is the required coefficient (Reg 05 b0-5), when KO has no dispersion.
KO_{act} : the actual measured value (with the auto-calibration).
$K_{corrected}$: the coefficient that will be set after the auto-calibration.

How to select the optimum setting in the FM deviation table (Reg 05 B0-5)

In the FM deviation table of the STV42/56 circuits, each step produces a 11% increase :

$$K_{N+1}/K_N = 1.11$$

Consequenctly the maximum allowed dispersion α of the slope KO before a correction is necessary, is the dispersion which respects the following relation :

$$(1+ \alpha) = (1 - \alpha) \cdot 1.11 \Rightarrow \alpha = 5.26\%$$

Repeting the same idea, it is possible to build a table of the required correction versus the dispersion of the VCO slope. Proposed table :

In this table R is the ratio : $KO_{act} / KO_{Typ.}$

$R_{Min.}$	$\leq R \leq$	$R_{Max.}$	Required correction
------		0.692	- 4
0.692		0.768	- 3
0.768		0.853	- 2
0.853		0.947	- 1
0.947		1.0526	No correction
1.0526		1.168	+ 1
1.168		1.297	+ 2
1.297		1.44	+ 3
1.44		------	+ 4

+ 1 means : for a given deviation, + 1 is added to the typical value which is loaded in Reg 05 (example for $\pm$ 50kHz, typical value is 36h and the corrected value is 37h).

Remark : In general the correction will not exceed $\pm$ 2.

In practice

In practice the microcontroller which are used in the satellite receivers seldom have advancd arithmetic processing functions (such as division). So, we propose to compare the actual result (F_e - F_o) to its expected typical value δ_{th}.

$\delta_{th} = \Delta V \cdot KO_{Typ.}$
ΔV : 1V for Reg 05:23h and 2V for Reg 05:03h
$KO_{Typ.}$: 460kHz/V

To select the corection to be implemented, a table similar to the above described one can be used. The selection range of this new table is :

$$\delta_{th} \cdot R_{Min.} \leq F_e - F_O \leq \delta_{th} \cdot R_{Max.}$$

d - Additionnal Advices about the Auto-calibration Function

d.1 - When to implement the auto-calibration function ?

It is suggested to implement the auto-calibration function when the end-user turns-off the satellite receiver (remote control command or front panel command).

This position of the auto-calibration function offers two advantages :

- The receiver is auto-calibrated when the part is already warmed-up. In this way potential drift related to temperature are taken into account.
- The auto-calibration is done when the end-user no longer wishes to use the receiver, consequently the duration of the auto-calibration routine (about 1s) is no longer an inconvenience.

d.2 - To minimize the errors coming from voltage offsets

There are two settings of Reg 05, 03 and 23 which can be used for the auto-calibration, but in preactice we suggest to use Reg 05 : 03 because it produces a higher voltage increase in the VCO drive. In such a case the offset voltages have relatively less influence.

d.3 - Compensation of the drifts appearing on CPUMP (see Figure 15)

To be efficient, the auto-calibration routine must be as precise as possible.
For this reason we would suggest to compensate some errors which may happen during the auto-calibration routine.
More precisely, it has been noticed that small leakage currents produce a drift of the CPUMP voltage which also drives the VCO. Consequently, because of the required delay between the 3rd and 4th steps of the auto-calibration routine, a small error ε may be induced in the drive voltage of the VCO.

Suggestion :
To repeat twice the 4th step (frequency watchdog). The first time about 200ms after the 3rd step. The second time after a well known duration after the first time.
Assuming that the drift is linear, it is possible to correct the first reading.

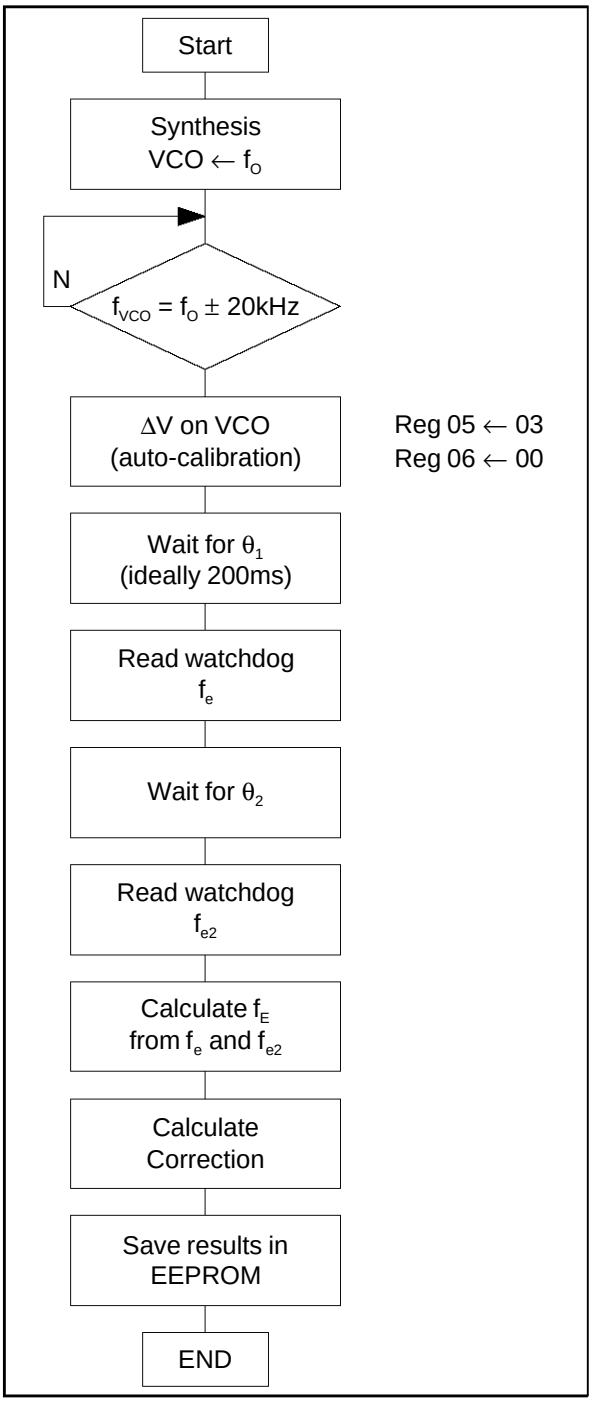
Additionnaly to minimize the leakage currents which would induce a drift of the CPUMP voltage, it is suggested not to connect the PLL circuit to the incoming RF signal, but to keep the phase detector input to bias (ex: if left channel is calibrated Reg 06 B2 = L and Reg 06 B4 = L).

3 - APPLICATION NOTES (continued)

e - Suggested Flow Chart

Following is a suggestion which has not been tested in SGS-THOMSON laboratory yet.

Figure 16 : Auto-Calibration Flow Chart



3.3 - Audio Processing

Figure 17 and Figure 18 give the architecture of the audio processing part of the STV42/56 circuits.

The main functions of the audio processing part are :

- the audio noise reduction system (ANRS),
- the audio de-emphasis,
- the volume control with the mono stereo switch,
- a switching array,
- input/output buffers.

3.3.1 - Audio Noise Reduction (ANRS)

About the ANRS, there is a main difference between the STV0042 and the STV0056.

In the STV0042, the input signal of the ANRS is the sum of left and right (L + R) (see Figure 19). Whereas, the STV0056 has two independant ANRS (one for left and one for right) (see Figure 20). For this reason, it is recommanded to use STV0056 when "Panda" qualification is targeted.

Additionnally, as far as the ANRS input is concerned, the STV0056 offers two options (K4) ; either the decoder return or the FM demodulator output. The decoder return has been implemented provisionnaly, but so far, the second output is required : FM demodulator output.

3.3.1.1 - Principle

The basic idea of the ANRS is to controlled the bandwidth of the output gm amplifier versus the amplitude of the demodulated audio signal coming from the FM demodulator.

To do so, the ANRS implements three main functions :

- An external band pass filter which rejects the undesired signal components which remains at the output of the FM demodulator.
- The filtered signal is rectified, so that the DC voltage at Pin PKOUT is an image of the audio signal amplitude.
  More precisely :
  $(V_{PKOUT} - V_{REF}) = k \cdot A$ = control signal
  with K = proportionnality coefficient
  and A = amplitude of the audio signal
- The output stage is an amplifier whose transconductance is a function of the control signal
  gm = f(control) = f (K . A)

3 - APPLICATION NOTES (continued)

Figure 17 : STV0042 Audio Processing Block Diagram (Channel Left)

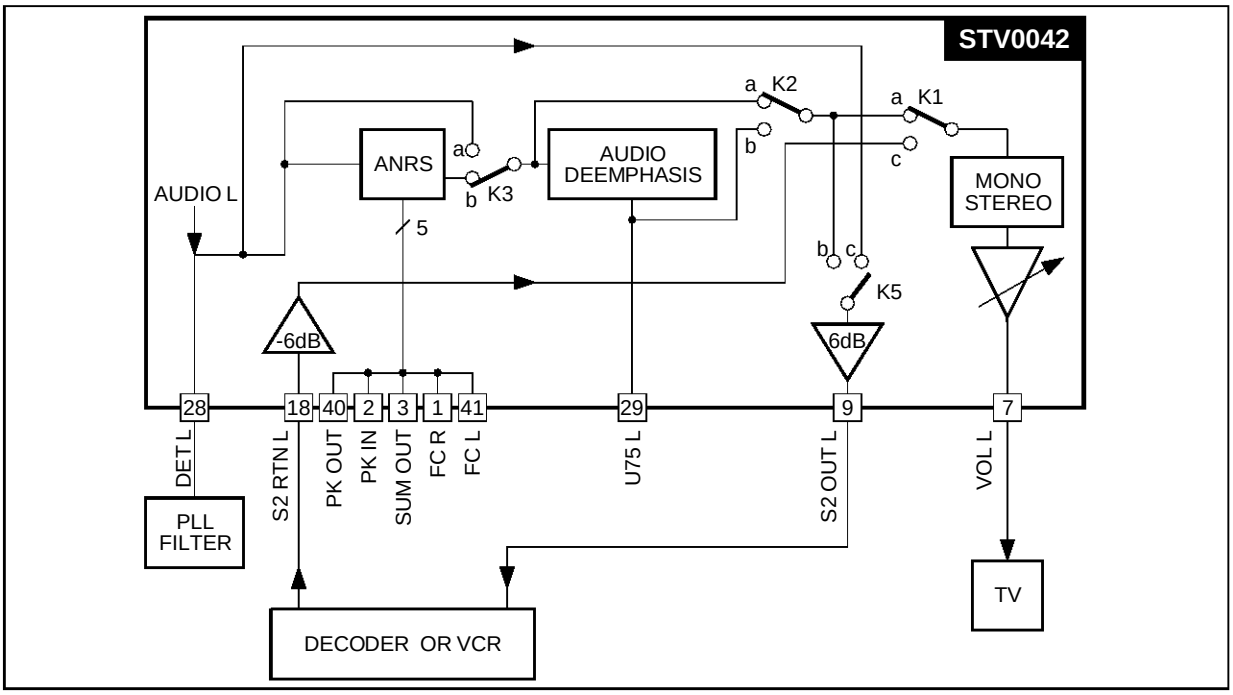
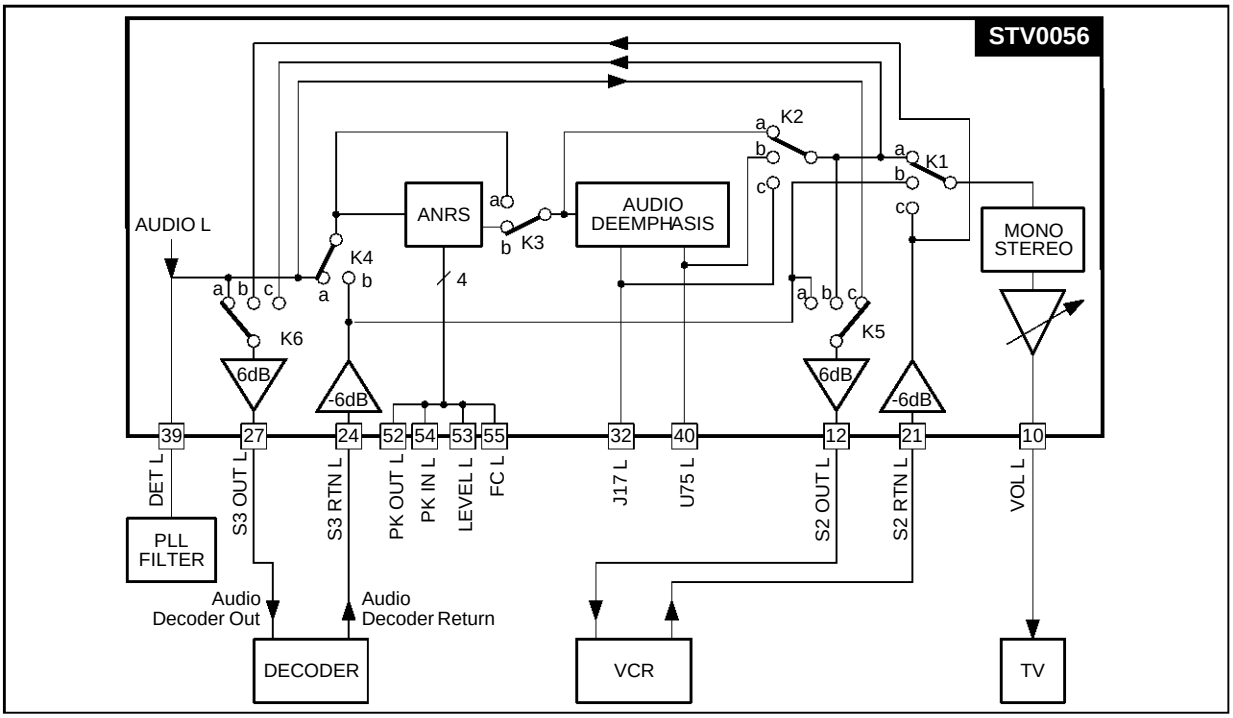


Figure 18 : STV0056 Audio Processing Block Diagram (Channel Left)



3 - APPLICATION NOTES (continued)

Figure 19 : STV0042 ANRS Block Diagram

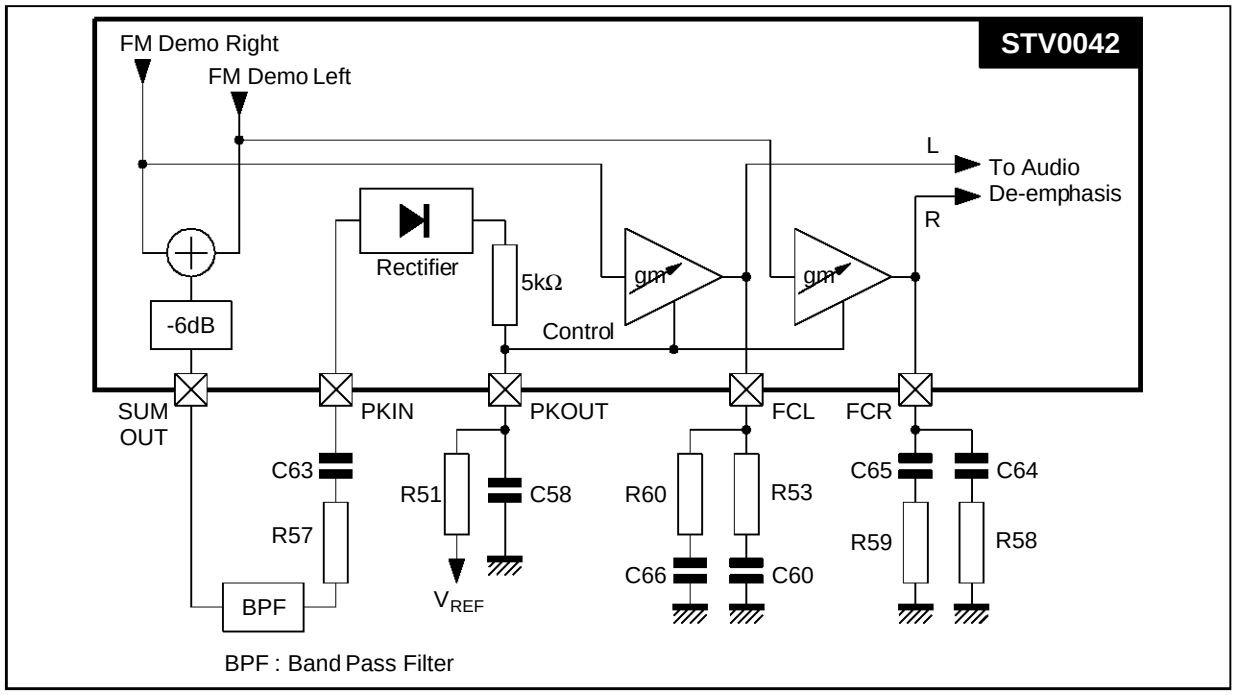
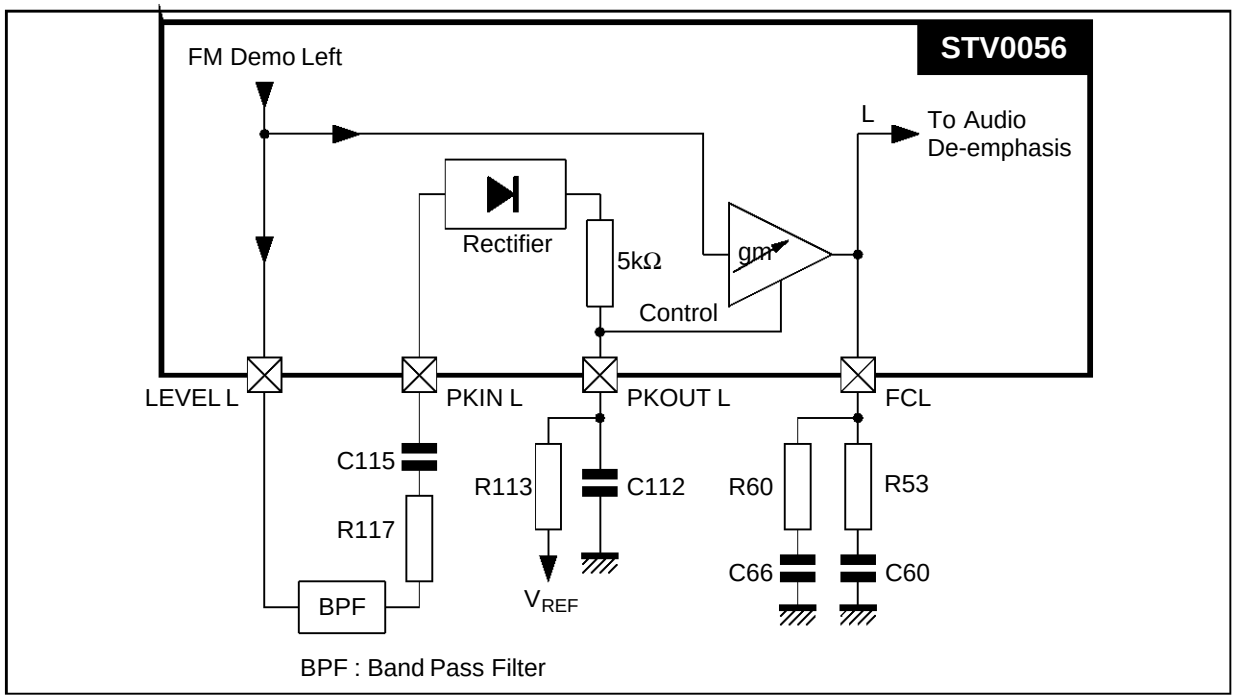


Figure 20 : STV0056 ANRS Block Diagram



3 - APPLICATION NOTES (continued)

3.3.1.2 - Dimensioning the External Components

a) The Band Pass Filter : BPF

The output signal of the FM demodulator contains different components :

- The desired demodulated signal,
- beat signal of the unwanted subcarriers with the VCO frequency,
- beat signal of the attenuated video with the VCO frequency (attenuated video : the input filter C_{25}, R_{18}, R_{17}, L_4, C_{24} does not totally reject the video).

The amplitude of the beat signals cannot be neglected when the desired audio signal has low amplitudes. Consequently, it is necessary to filter the signal before the rectifier.

For a better efficiency a 12dB/octave filter (order 2) is prefered.

The suggested solution (Figure 21) is a simple, low-cost, active filter (using a Sallen and Key structure).

Main characteristics :

$Z_{IN} \geq$ few kΩ, $Z_O \leq 100\Omega$, Bandwidth ≥ 15kHz, Attenuation at 80kHz ≈ 25dB, Peaking ≈ 1.3dB

A small peaking has been prefered to provide a small correction of the frequency response of the complete ANRS.

b) Input and Output Circuitry of the Rectifier (R_{117}, C_{115}, C_{112}, R_{113})

C_{115} is necessary because the rectifier requires a capacitive coupling with the BPF. C_{115} value is not critical ($C \geq 220nF$).

R_{117} value combined with an internal 68kΩ resistor, gives the gain of the rectifier :

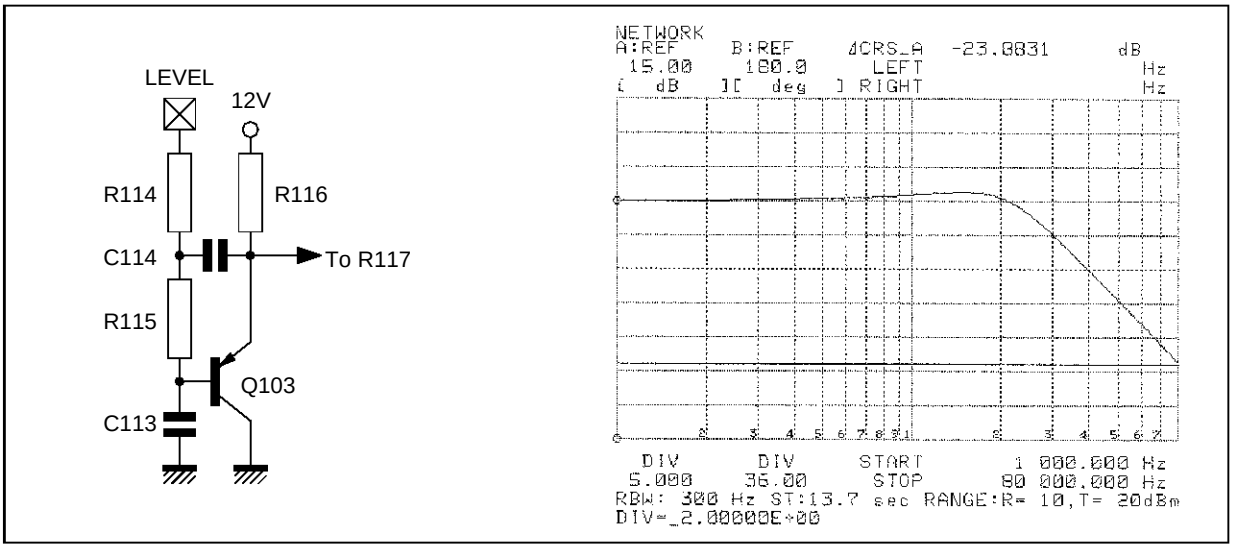
$$(V_{PKOUT} - V_{REF}) = K \cdot A$$
$$\text{with } K \approx \pm \frac{68k\Omega}{R_{117}}$$

C_{112} : Combined with an internal 5kΩ resistor, the C_{112} capacitor produces a time constant which is optimized in order to have the lowest overshoot as possible on the rising edge of the 2Hz/4 ÷ 1 burst pattern used in the PANDA qualification.

Once C_{112} is fixed, R_{113} is choosen to produce a delay time constant which compensates the envelop appearing at the beginning of the low amplitude session of the 2Hz/4 ÷ 1 burst pattern used in the PANDA qualification. Good compromise with $R_{113} = 560k\Omega$.

Remark : The Rectifier is not a full wave one, it works with negative halfwaves.

Figure 21 : Example of Simple Band Pass Filter

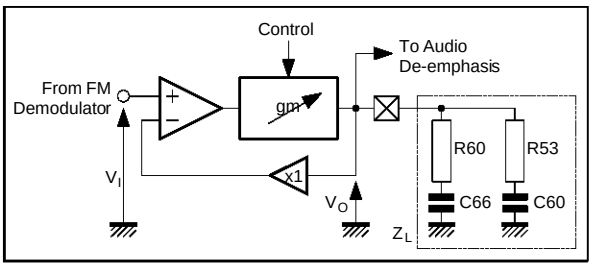


3 - APPLICATION NOTES (continued)

c) Load of the Output Amplifiers
(R_{60}, C_{66}, R_{53}, C_{60})

Looking at more in details, the output amplifier can be described as given in Figure 22.

Figure 22 : ANRS Output Amplifier Structure



with such a structure : $\frac{V_O}{V_I} = \frac{\pm gm\ Z_L}{1 + gm\ Z_L}$ (1)

In order to simplify the calculations, it can be noticed that the R60 C66 filter only operates at very low frequencies, and assuming that $R_{60} >> R_{53}$, the impedance Z_L can be reduced to (R_{53} + C_{60}).
With such assumptions

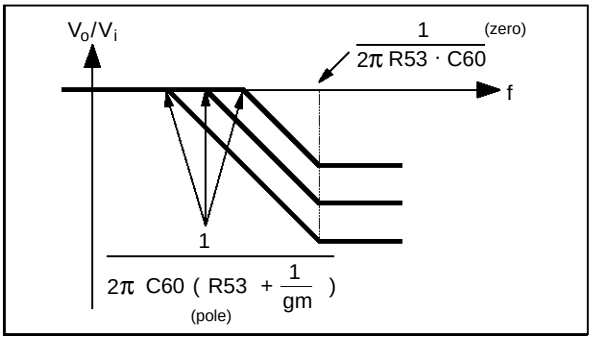
$$\frac{V_O}{V_I} = \frac{R_{53} \cdot C_{60} \cdot p + 1}{\left(R_{53} + \frac{1}{gm}\right) \cdot C_{60} \cdot p + 1}$$

p : Laplace operator (p = j2πf in the frequency field)

gm = f(control)

Conclusion :
The output stage of the ANRS behaves as a filter having a fixed zero and a variable pole (depending on the audio level) (see Figure 23).

Figure 23 : ANRS Output Amplifier, General Frequency Response



The ANRS is used in combination with the 75µs de-emphasis ; consequently the (zero) frequency is choosen to compensate the de-emphasis

$\Rightarrow R_{53} \cdot C_{60} \approx 75\mu s$

The value of R53 is optimized in order to get the flatest frequency response as possible at levels (PPL - 18dB) and (PPL - 28dB) of the PANDA qualification (PPL : standing for peak program level which is equivalent to full deviation ± 50kHz)

In summary :
- $R_{53} \cdot C_{60} \approx 75\mu s$
- R_{53} and R_{117} optimized to get flat frequency response with (PPL-18dB) and (PPL-28dB).

R_{60} C_{66} Filter : Without this filter, when the audio signal is very low ($V_{PKOUT} \approx V_{REF}$) or when there is no signal, the 1/gm value reaches very high values (several MΩ) ; under those conditions the FC Pins have a very impedance and become a noise pick-up. With the R_{60} C_{66} filter, the maximum impedance which can be reached by the FC Pins is clipped to the value of R_{60} ; the S/N ratio is greatly improved. C_{66} is not actual ($C_{66} \geq 10nF$).

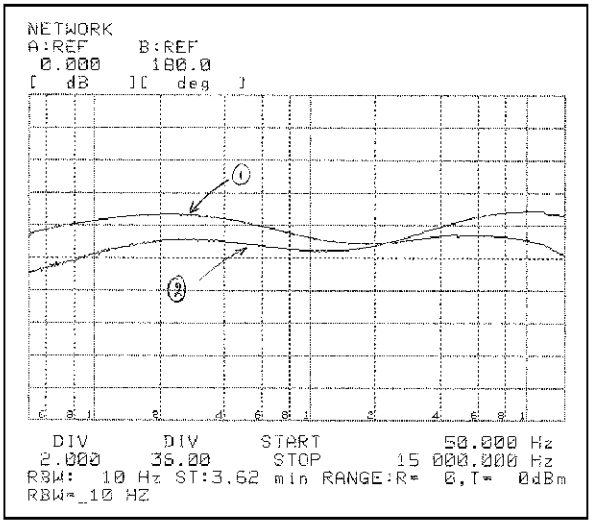
3.3.1.3 - Results with PANDA Encoder

Refering to the STV0056 specification.

a) Distorsion is lower than 1% at PPL
b) Crosstalk is typically lower than 60dB in stereo at 1kHz
c) Signal to noise ratio unweighted
(output level : 0.77V_{RMS})
S/N = 67dB typ.
S/N ⇒ 74dB typ. (with 400HzHPF)
d) Frequency Response at (PPL - 18dB) and (PPL - 28dB) (see Figure 24)
e) Compander Gain Tracking

Input Level	400Hz	10kHz	Limits
PPL	18dB	16dB	23/17dB
PPL - 10dB	11.4dB	8.4dB	23/17dB
PPL - 20dB	0	0	Reference
PPL - 30dB	-11.1dB	-8.8dB	-13/-7dB
PPL - 40dB	-20dB	-17.8dB	-23/-17dB
PPL - 50dB	-29.4dB	-27.4dB	-34/-26dB
PPL - 60dB	-37dB	-36dB	-47/-33dB

Figure 24 : ① : PPL - 18dB . ② : PPL - 28dB



3 - APPLICATION NOTES (continued)

3.3.2 - Audio De-emphasis

The audio de-emphasis functions are simply realized with transconductance amplifiers loaded by external loads whose impedance follow the required de-emphasis laws (see Figure 25).

With such structures :

$V_{OUT} = V_{IN} \cdot gm \cdot Z_L$ (1)

Z_L : Output Impedance (external circuit)

3.3.2.1 - Dimensioning the External Components

a) J7 De-emphasis (STV0056 only)

Using relation (1) :

$$\frac{V_{O17}}{V_I} = \frac{R_{107} \cdot C_{108} \cdot p + 1}{(R_{106} + R_{107}) \cdot C_{108} \cdot p + 1}$$

p : Laplace operator ($p = j2\pi f$ in the frequency field)

The DC gain of the J17 de-emphasis is dimensionned in order to comply with the scart recommandations : $V_{OUT\ scart} = 1V_{RMS}$ 3dB at full deviation. Taking into account the 6dB gain of the scart drivers.

$$V_{O17} = \frac{V_{OUT\ scart}}{2} = 0.5\ V_{RMS} \Leftrightarrow 1.41\ V_{PP}$$

$$\left(\frac{V_{O17}}{V_I}\right)_{DC} = gm \cdot R_{106}$$

with $gm = \frac{1}{10.8k\Omega}$ (integrated characteristics)

$V_I = 0.44\ V_{PP}$ (at low frequencies of a J17 pre-emphazed signal)

$\Rightarrow R_{106} \approx 34.7k\Omega \Rightarrow R_{106} = 36k\Omega$ (2)

As far as AC characteristics are concerned :

(3) $\frac{1}{2\pi R_{107} \cdot C_{108}} \approx 4135Hz$
(zero of the J17 curve)

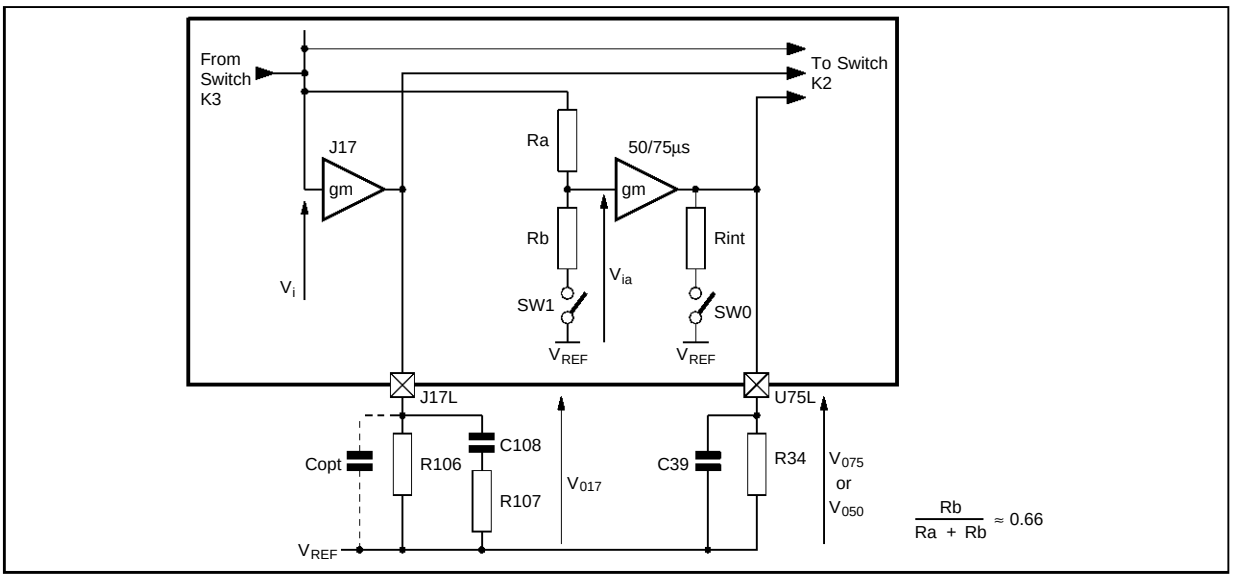
(4) $\frac{1}{2\pi (R_{106} + R_{107}) \cdot Cp} \approx 477Hz$
(pole of the J17 curve)

Combining (2) (3) (4) :
$R_{107} = 4.69k\Omega \Rightarrow R_{107} = 4.7k\Omega$
$C_{108} = 8.19nF \Rightarrow C_{108} = 8.2nF$

Remark about J17

1) Due to the zero of the J17 law, the high frequency signals contained in the input signal are not completely attenuated. This explains why the beat frequency produced inside the PLL section remains present at the scart output when J17 is selected.
   If the user prefers to give a further attenuate to the high frequency signals, optionnally C_{OP} can be used (C_{OPT} is choosen to produce a additional pole at about 20kHz). In theory $C_{OPT} \approx 1.9nF$ (1.5nF can be also selected for standardization of values).
2) Under certain conditions it is possible to implement both J17 and 50/75µs with STV0042 (please refer to "Application options" Chapter 4.2).

Figure 25 : Audio De-emphasis Solution



3 - APPLICATION NOTES (continued)

b) 75µs De-emphasis

When the 75µs de-emphasis is selected, SW1 is closed and SW0 is opened.

The de-emphasis amplifier is only loaded by the external C_{39} R_{34} filter, and with SWI the input level is attenuated in order to have similar output levels for both 75 and 50µs de-emphasis.

DC gain :
$V_{O75} = V_{ia} \cdot gm \cdot R_{39}$
with
$V_{O75} = 1.41\ V_{PP} \Rightarrow R34 \approx 25.4k\Omega \Rightarrow 27k\Omega$
$gm = 1/10.8k\Omega$
$V_{ia} = 0.66\ V_I$
$V_I = 0.905\ V_{PP}$

AC characteristics :
$R_{34}\ C_{34} \approx 75\mu s \Rightarrow C_{39} = 2.7nF$

c) 50µs De-emphasis

When 50µs de-emphasis is selected, SW1 is opened and SW0 closed.

The load of the de-emphasis amplifier corresponds to the external filter in parallel with an internal resistor R_{IN}.

This configuration would give a lower DC gain, but in compensation the input signal is not attenuated (SW1 : opened).

Remark : In theory Rint value should be equal to 2 x R34. This not the case. This imperfection of the circuit will be corrected in a version which will be launched lately (STV0056A).

d) General Remark about the Audio De-emphasis

When the audio de-emphasis Pins are not used, it is required to directly connect them to V_{REF}.

3.3.3 - Volume Control, Mono Stereo Switch

Most of the informations relevant to the volume stage are given in the specification.

The mono/stereo switch allows to output on the volume controlled stage either the stereo signal or twice left or twice right.

Remark : The mono/stereo switch is only available on volume outputs.
In case of multilingual channels it is preferable to set the two FM demodulators on the same subcarrier, so that there is no problem for the other outputs : S2 and S3.

3.3.4 - Switching Array

The STV42/56 circuits offer many switching configurations, please refer to the specification for details.

3.3.5 - Input/Output Buffers

a) The input buffers (S2RTN, S3RTN Pins) have two important characteristics :
   - the input impedance is 25kΩ typically,
   - a 6dB attenuation : allowing to accept signals as high as $2V_{RMS}$.

b) The output buffers (S2OUT, S3OUT Pins) have the following characteristics :
   - 6dB gain : in order to have a $1V_{RMS}$ output signal at full deviation,
   - can be set to high impedance, this feature is interesting for twin tuner applications,
   - output impedance Z_{OUT} is about 60Ω (in active mode).

Remark :
Under certain conditions, this rather low impedance (60Ω Typ.), allows to realize the (L + R) function (required to drive the RF modulators) by simpling using two resistors without inducing high level of crosstalk (see Figure 26).

The crosstalk level can be calculated as

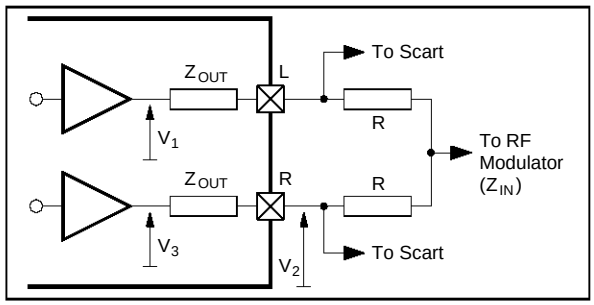
$$Ctk = \frac{V_2}{V_1} \text{ with } V_3 = 0$$

assuming $Z_{OUT} << R$, and $Req = R//Z_{IN}$

$$\frac{V_2}{V_1} \approx \frac{Z_{OUT}}{R + Z_{OUT}} \cdot \frac{Req}{Req + R}$$

Example :
a RF modulation with Z_{IN} = 10kΩ and requiring $1.24V_{PP}$ at full deviation
$\Rightarrow R = 27k\Omega$
$\Rightarrow (Ctk)_{dB} = -66dB$

Figure 26 : Simple (L + R) Function for RF Modulator Drive



3 - APPLICATION NOTES (continued)

3.4 - Others Functions, Miscellaneous

3.4.1 - Power Supplies

For operation, the STV42/56 circuits simultaneously require both a 5V (V_{DD}) and a 12V (V_{CC}). Due to an internal reset function, the STV42/56 circuits stop working when either the 5V or the 12V line is faulty (or both). Under this condition all the registers are reset and the I^2C decoder stops operating.

Remark : The reset signal is available at Pin I/O of STV0056 when R5 B7 = H and R5 B6 = L. Reset signal is active high.

Important Remark :
For power consumption and reliability, it is not recommanded to only supply either the 5V or the 12V. Under those conditions, high currents may circulate in the ESD protection circuit (electrostatical discharge protection diodes).

3.4.2 - Active/Stand-by Modes

The STV42/56 circuits features a stand-by mode in which the power consumption is greatly decreased (one thrird). However in this stand-by mode the following functions remain active :
- I^2C bus decoder,
- audio switching matrix,
- video clamp and switching matrix.

With such a configuration it is still possible to route signals during the stand-by mode of the receiver (example : to connect the VCR scart audio and video signals to the TV scart).

To enter or to exit the stand-by mode is simply done by driving R04 B3.

Remark :
To minimize the power consumption in stand-by, it is recommanded to set as many audio and video output stages in high impedance modes (minimizes the STV42/56 consumption and turns off the external 75Ω video buffers).

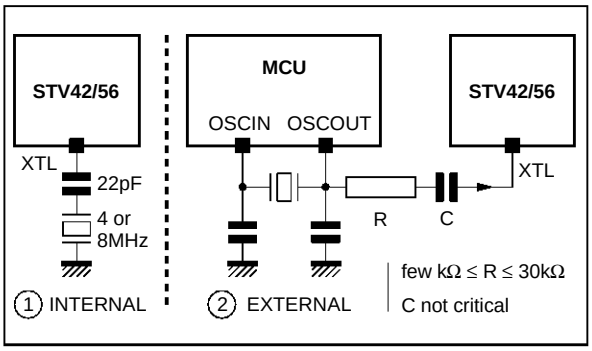
3.4.3 - Crystal / Clock

Two functions of the STV42/56 circuits require a precise reference frequency : the 22kHz tone generator and the frequency synthesis function of the FM demodulator (required accurary < 0.4%).

Two possible frequencies can be selected 4MHz or 8MHz (R02 B3).

The clock pin XTL of the STV42/56 have been designed to either work with a external crystal or to be an clock input. For instance, this second solution can be used if the microcontroller work with a 4MHz or 8MHz crystal (see Figure 27).

Figure 27 : External or Internal Clock Generation



Remark :
If for cost reasons, clock signals with an accurary ranging from 0.3 to 0.6% are prefered, please contact with SGS-THOMSON.

3.4.4 - 22kHz Tone Generator

The STV42/56 circuits can generate the 22kHz tone signal required to control the LNB systems. The actual frequency is 22.22kHz ; the frequency accuracy is very high because the tone signal is derived from the clock signal.

Depending on the register settings, there are several possibilities to get the 22kHz tone :

STV0042	Pin 13	R03 B3 : H	and R01 B7 : L
STV0056	Pin 16	R03 B3 : H	and R01 B7 : L
STV0056	Pin 29	R05 B6 : H	

Remark :
When STV0042 Pin 13 or STV0056 Pin 16 is used to generate the 22kHz tone signal, some care must be taken to avoid crosstalk on the VIDEEM1 Pin :
- to limit the parasitic capacitance of the PCB between VIDEEM2/22kHz Pin and VIDEEM1 Pin (optionnally some ground shielding track can be layout between those 2 pins).
- Optionnally, the slew rate on VIDEEM2/22kHz Pin can be decreased by connecting a capacitor to ground (≈ 100pF).
- The equivalent impedance at VIDEEM1 Pin can be decreased (see last remark of paragraph 3.1.1.3).

3.4.5 - I/O Interface

The Pin 29 of STV0056 circuit can be set as a general purpose digital I/O (Input/Output). To do so, R05 B6 B7 R06 B0 B1 are needed.

For example in combination with a resistor divider, this I/O may be used to monitor the Pin 8 of a scart connector.

3 - APPLICATION NOTES (continued)

3.5 - PCB Layout Recommandations

The pinout of the STV42/56 circuit has been defined to, in the widest extent as possible, simplify the PCB layout.
Dual in line plastic packages (SDIP42 or SDIP56) have been prefered to offer a low cost solution. Additionnaly with these packages very compact and efficient layout can be design by soldering surface mounted devices (SMD) under the circuit.

3.5.1 - Power Supplies and Ground Paths

With reference to the STV42/56 pinnout and to the Figure 30 of the specification (page 21/33 of the specification dated June 95). The STV42/56 circuits feature :
- 3 independants power supply lines (5V, 12V Video, 12V Audio),
- 4 independants ground pins (GND 5V, Video Ground, Audio Ground Left, Audio Ground Right).

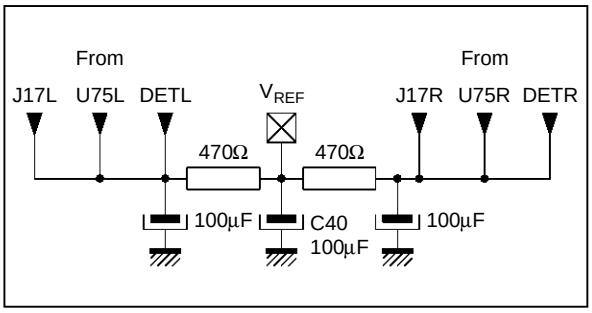
In such as a configuration, to avoid interferences between the different supply lines, it is important : (see example in Figure 29).
- To make a star connection of the four ground tracks.
- To have short connections to the decoupling capacitor of each supply line (at least to the ceramic capacitor which realizes a good decoupling of the high frequency components of the supply current).

3.5.2 - I_{REF}/V_{REF} Pins

With an external 240kΩ 1% resistor (or very close value), the I_{REF} Pin is used to produce a 10µA reference current which is used to bias most of the internal functions of the circuit.
The ground point to which this external resistor is connected must not be polluted ; ideally it is the audio ground right pin or in between audio ground pin and the ground star point.
A V_{REF} line (2.4V) is generated by the STV42/56 circuits. This reference line is used to bias the audio stages (audio de-emphasis, noise reduction). Typically a 470µF external capacitor C_{40} is used for decoupling, preferally this capacitor is connected close to the V_{REF} Pin.

Optionnally, to improve the left to right crosstalk at low audio frequencies, low pass filters can be used for both left and right current paths ; those two filters are connected to the V_{REF} decoupling capacitor C_{40} (see Figure 28).

Figure 28 : Optional V_{REF} decoupling with Separated Left and Right Paths



3.5.3 - Insulation between the Video Inputs and Outputs

A lot of care must be given in making two separate ground paths one for the video input, the other for video outputs.

Reason : Due to the low impedance (75Ω) of the video sources (TV return, VCR return, decoder Return) and of the video outputs (TV out, VCR out, decoder out), even small commun PCB pattern produces important crosstalk.

Example : a 0.1Ω commun impedance on the groud path between the input and the outputs would generate (-57dB) of crosstalk.

3.5.4 - Insulation between Video Outputs

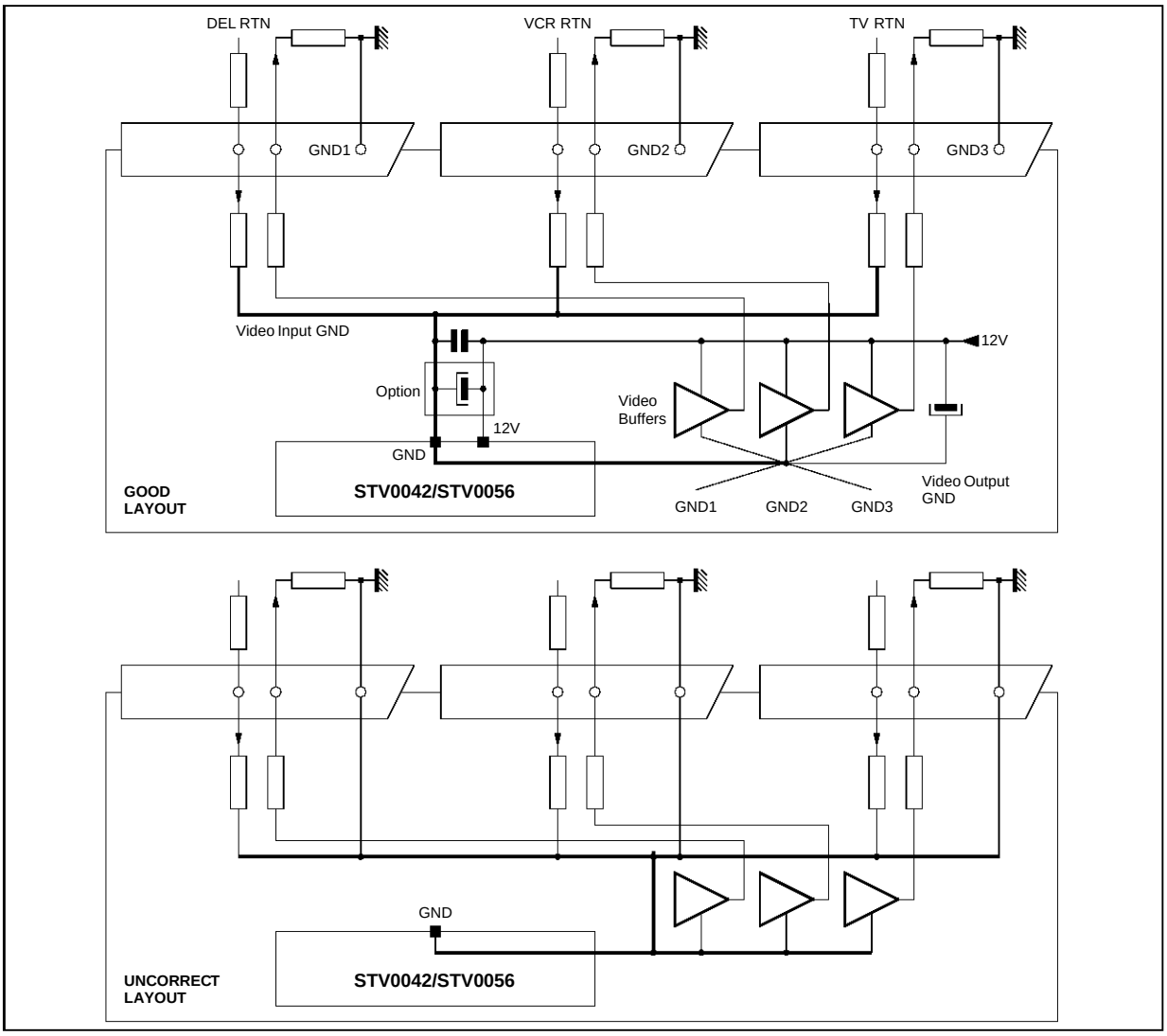
Again due to the low impedance it is important to minimize the commun impedance between the different outputs.

To do so, it is preferable to make a star connection with the output video buffers and with the video ground of each output connector (GND1, GND2, GND3) (see Figure 29).

Additionnaly it is recommanded to have a short connection between the ground star point and the video (12V) decoupling capacitor, C33.

3 - APPLICATION NOTES (continued)

Figure 29 : PCB Layout, Ground Pattern (good and uncorrect layout)



3.5.5 - Insulation between Video Inputs

As usually required with video signals, it is recommanded to minimize the parasitic capacitances between the video inputs.
For memory, one pF (picofarad) parasitic produces about 61dB crosstalk at 5MHz. When possible, to minimize this capacitance, a ground shield can be layout between the video tracks.

3.5.6 - 22Hz Tone Influence on VIDEEM1

When the VIDEEM2/22kHz Pin is used as a 22kHz tone generator some care has to be taken in the PCB layout.
The 22kHz tone track must be layout as far as possible from the VIDEEM1 Pin and from R_{10}, R_{11}, C_{13}, R_9, C_{12}.
It is also recommanded to layout a ground shield.

3.5.7 - Video Crosstalk on the Right Channel

Due to the circuit pinnout, the right channel noise reduction circuit is quite close to the video section. This remark is particularly important for FCR Pin which drives a high impedance ($\approx$ 51kΩ at 15kHz when the audio signal is low amplitude).

If no care is taken in the PCB layout, the video crosstalk may jeopardize the audio S/N which may become critical when applying for PANDA qualification.

Consequently, it is recommanded to minimize the capacitive coupling between FC right and the video tracks.

4 - APPLICATION OPTIONS

This part refers to some specific application cases (not typical cases).

4.1 - Simplified Video De-emphasis Channel

Some specific applications, or some specific markets do not require to ouput a baseband signal. Under this condition it is possible use the application diagram given in Figure 30.

The conventional emitter follower stage Q used at the tuner output is changed into a voltage amplifier (gain ≈ 3), and the video de-emphasis is done with the filter (R_a, R_b, C).

To recover the correct phase the inverter stage is set by software R01 B6. The de-emphasis amplifier is turned into a follower stage.

Remark :
R_a is choosen around 1kΩ in order not to be sensitive to the dispersion of the input stage impedance.

Advantages :

Compared with the typical application, this circuits offer two advantages :

- to save one electrolytre capacitor (C_{13}),
- to drive the input stage with attenuated high frequencies, this helps to minimize the potential intermodulation between the FM subcarriers with the video or the intermodulation of the parasitic side bands produced by the tuner with the wanted channel.

4.2 - J17 De-emphasis Generation with STV0042

In some specific applications, such as add-on board in TV set, the J17 de-emphasis may be required. There are two solutions (see Figure 31).

Solution 1

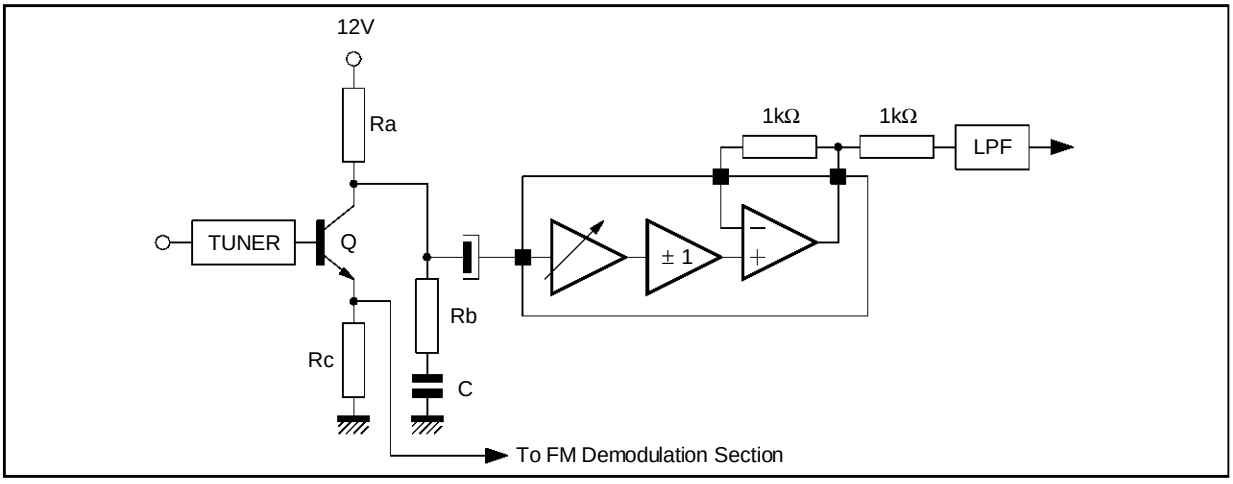
This solution can be implemented when the S2OUT and S2RTN are not required (no interface with decoder or when the interface function is implemented on the TV main board. In this solution, the PLL demodulator output signal is sent to S2OUT Pin (switch K5 to C, see STV0042 specification). And a J17 filter (R_1, R_2, C) is connected between S2OUT and S2RTN.

Remark :
With this solution, at full deviation the level is $1V_{PP}$ at S2RTN Pin. The level difference with 75µs needs to be compensated by the volume stage (+3dB).

Solution 2

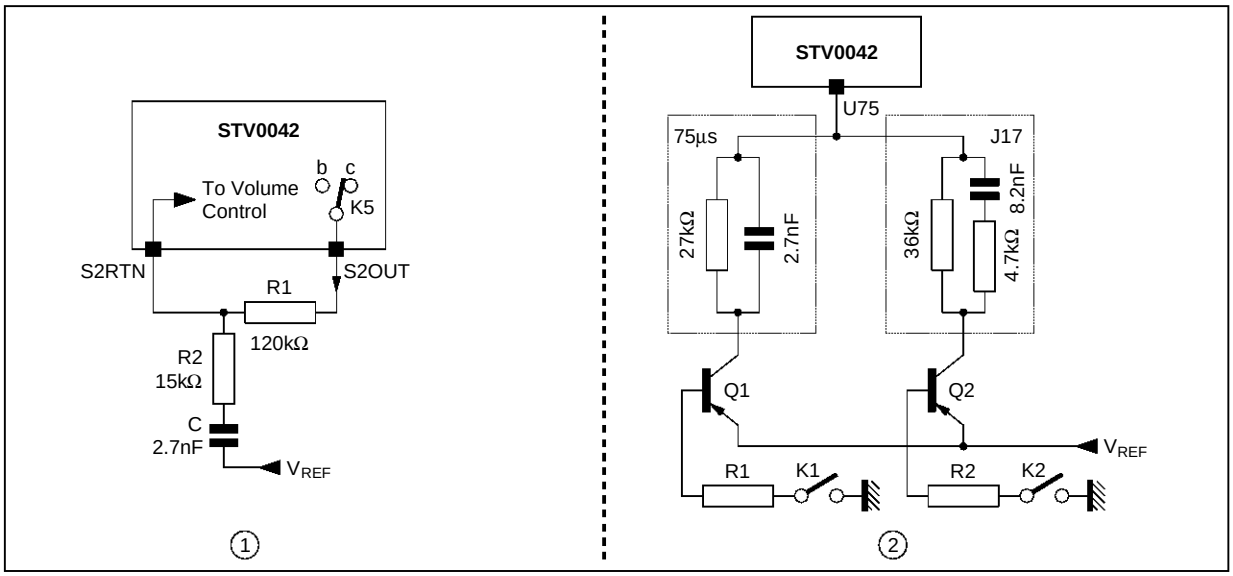
When solution 1 cannot be implemented, a second solution which switches de-emphais filters at U75 pin can be used.
The switch can be simply realized with PNP bipolar transistor, this solution does not provide distorsion if the base of those transistors is properly pulled down to the ground (R_1 and $R_2 \leq 10k\Omega$).
The control is done by two switches (transistors, or MCU I/O) which are in opposite state
(K_1 closed ⇔ K_2 opened, and vice-versa).

Figure 30 : Simplified Video De-emphasis Channel



4 - APPLICATION OPTIONS (continued)

Figure 31 : J17 De-emphasis with STV0042



4.3 - Simplified Audio Noise Reduction or No Noise Reduction

When it is not required to perfectly match with the PANDA noise reduction, the external filter used between LEVEl and PKIN Pins of STV0056 or SUMOUT and PKIN of STV0042 can be simplified (see Figure 32).

When no noise reduction is required, the following changes needs to be implemented in the application :

- to take all components connected to Pin LEVEL, or SUMOUT, PKIN, PKOUT, FC,
- to keep floating LEVEL or SUMOUT Pins,
- to connect to V_{REF} : PKOUT, PKIN Pins,
- to connect FC Pin either to V_{REF} or GND.

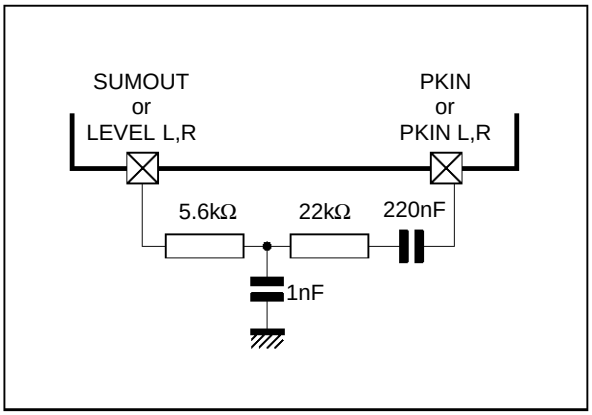
4.4 - Audio Mono Applications

This kind of application may be required for collective receiving systems where audio mono channels are processed. For those applications, more likely the STV0042 is choosen, and the following changes are recommanded :

- to remove all the components relevant to one channel (for example left)
- Following pins must be grounded : AGC, AMPLOCK
- Following pins must be connected to V_{REF} : DET, U75, CPUMP, FC
- The capacitor C_{40} may be reduced to 10 or 22µF.
- The resistor R_{57} must be reduced to half value (about 13 to 15kΩ) in case of STV0042.

A typical audio mono application diagram is given in Chapter 7.

Figure 32 : Noise Reduction, Simplified BPF



5 - TWIN TUNER APPLICATIONS

It is very easy to build twin tuner applications with STV42/56 circuits without extra audio and video switching hardware.

Twin applications are simply realized by paralleling the audio/video inputs and outputs (see Figure 33).

- The audio inputs impedance is 25kΩ, so a parallel configuration gives 12.5kΩ (still compatible with the Scart standard).
- The video inputs impedance is a few kΩ, so by far enough for parallel configuration.
- The audio and video outputs feature a high impedance mode (accessed by software) which allows to directly connect the outputs one to the other. By software one output is set to high impedance mode while the other is active.

Remark : Per default, to avoid conflicts at power-up all audio and video outputs are set to high impedance mode.

To avoid I^2C bus address conflicts, the STV0056 feature a hardware address pin HA which is used to define two addresses.

Twin tuner applications can be realized either with two STV0056 circuits or with STV0056 + STV0042.

6 - SATELLITE RECEIVER BUILT IN VCR OR TV SETS

For cost reasons, in these applications the STV0042 may be prefered. The add-on applications are basically the same as stand alone receivers, however here are some suggestions :

J17 with STV0042

Please refer to the chapter "Application Options" (section 4.2).

Clock Generator

In these applications, in order not to route a disturbing 4MHz or 8MHz clock signal from the main chassis ; the clock signal is generally generated locally on the add-on board.

There are two options :

- to use 4 or 8MHz crystal with the STV0042 circuit,
- or to use the 4MHz clock signal which is often generated inside the tuner (this point has to negociated with tuner makers).

Power Supplies

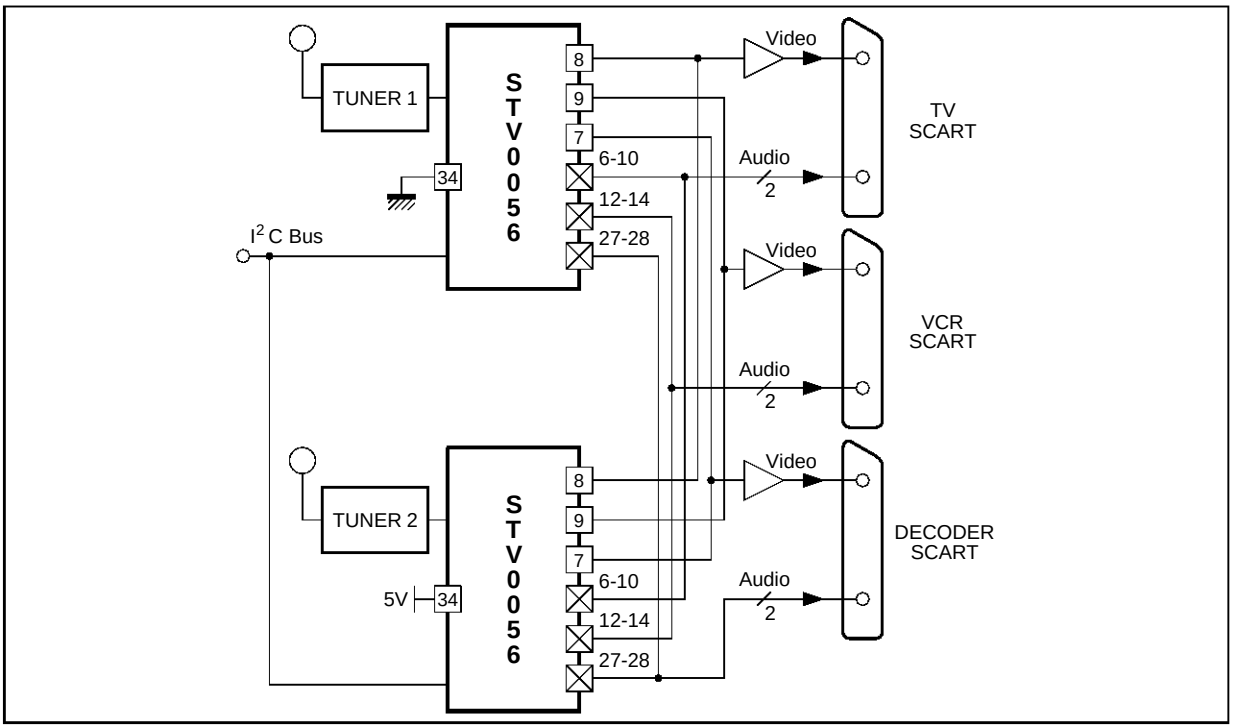
As mentioned in chapter "Other Functions/Miscellaneous" (section 3.4.1) , it is important to simultaneously maintain or turn-off both the 5V and 12V. It is important to bear this point in mind when designing the power system of the VCR or TV set.

Remark : Thanks to the low power consumption mode of the STV42/56, the power consumption remains reasonnable even when the add-on board is supplied during the stand-by mode of the VCR or TV set.

22kHz Tone

The signal can be output at the VIDEEM/22kHz Pin.

Figure 33 : Twin Tuner Applications. No Extra Switching Hardware Required.

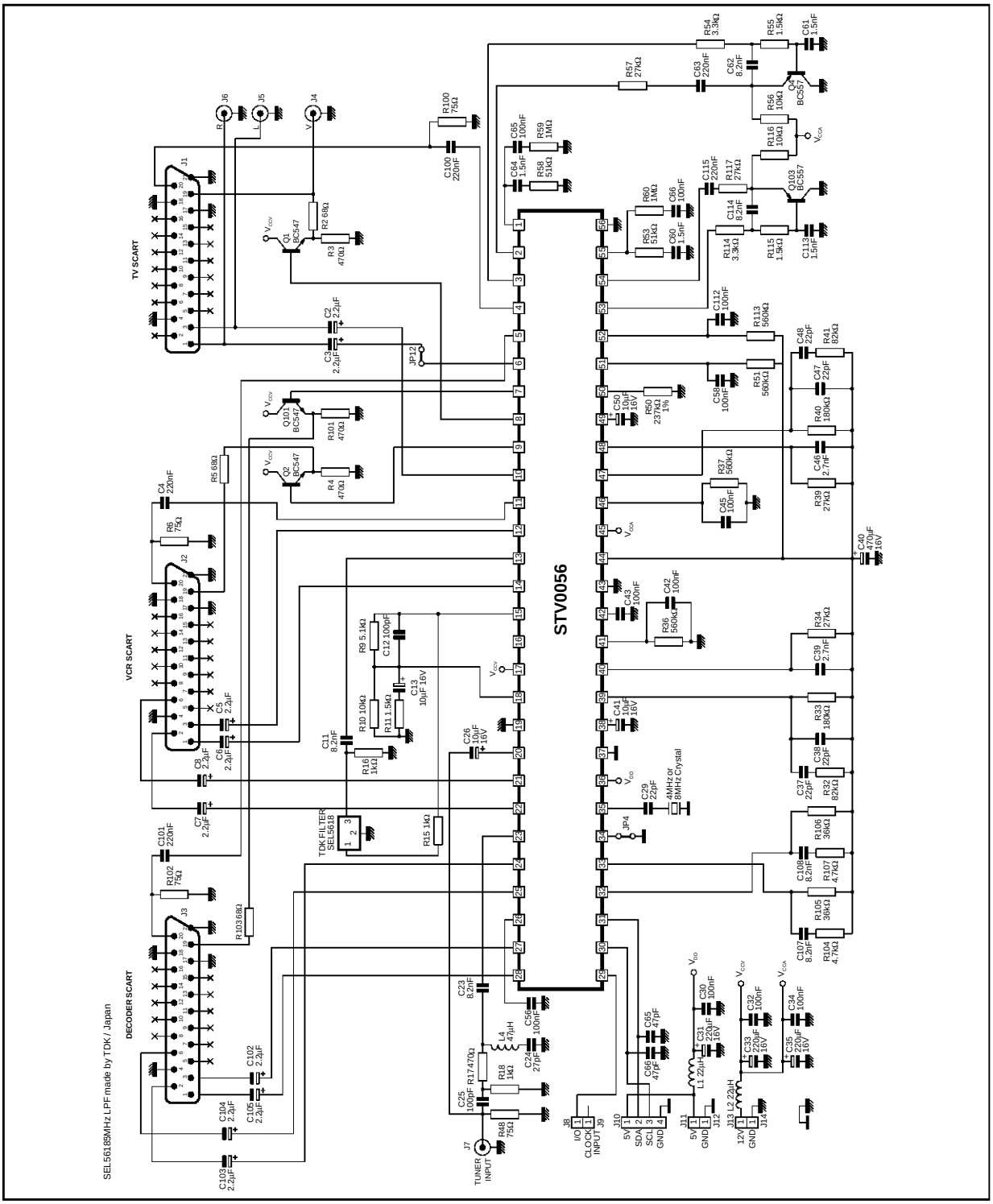


7 - TYPICAL APPLICATIONS DIAGRAMS

This chapter is simply a compilation of different typical application diagrams

7.1 - STV0056 : 3 Scarts PAL/Europe Application (Figure 34)

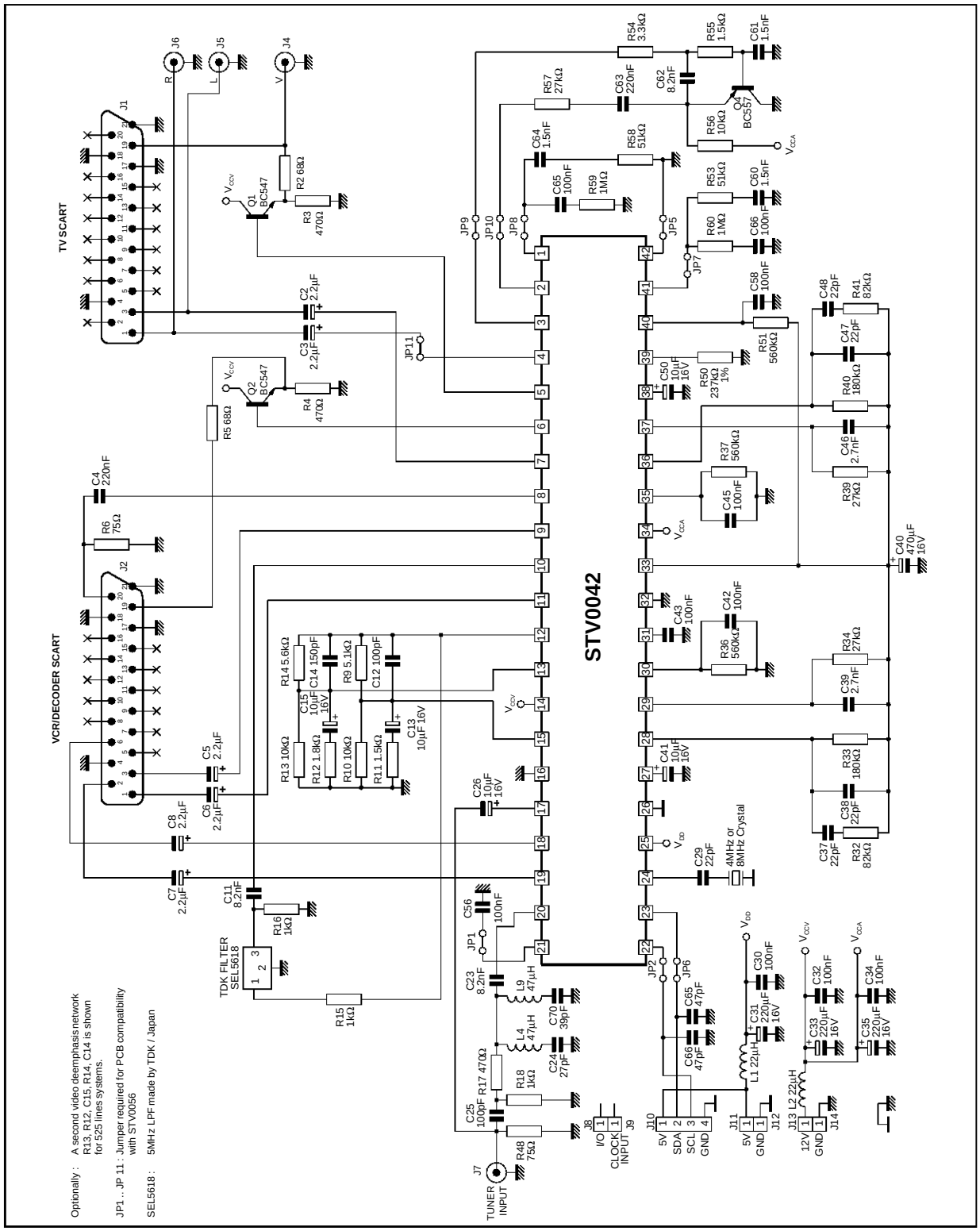
Figure 34



7 - TYPICAL APPLICATIONS DIAGRAMS (continued)

7.2 - STV0042 : PAL/NTSCApplication (2 video de-emphasis) (Figure 35)

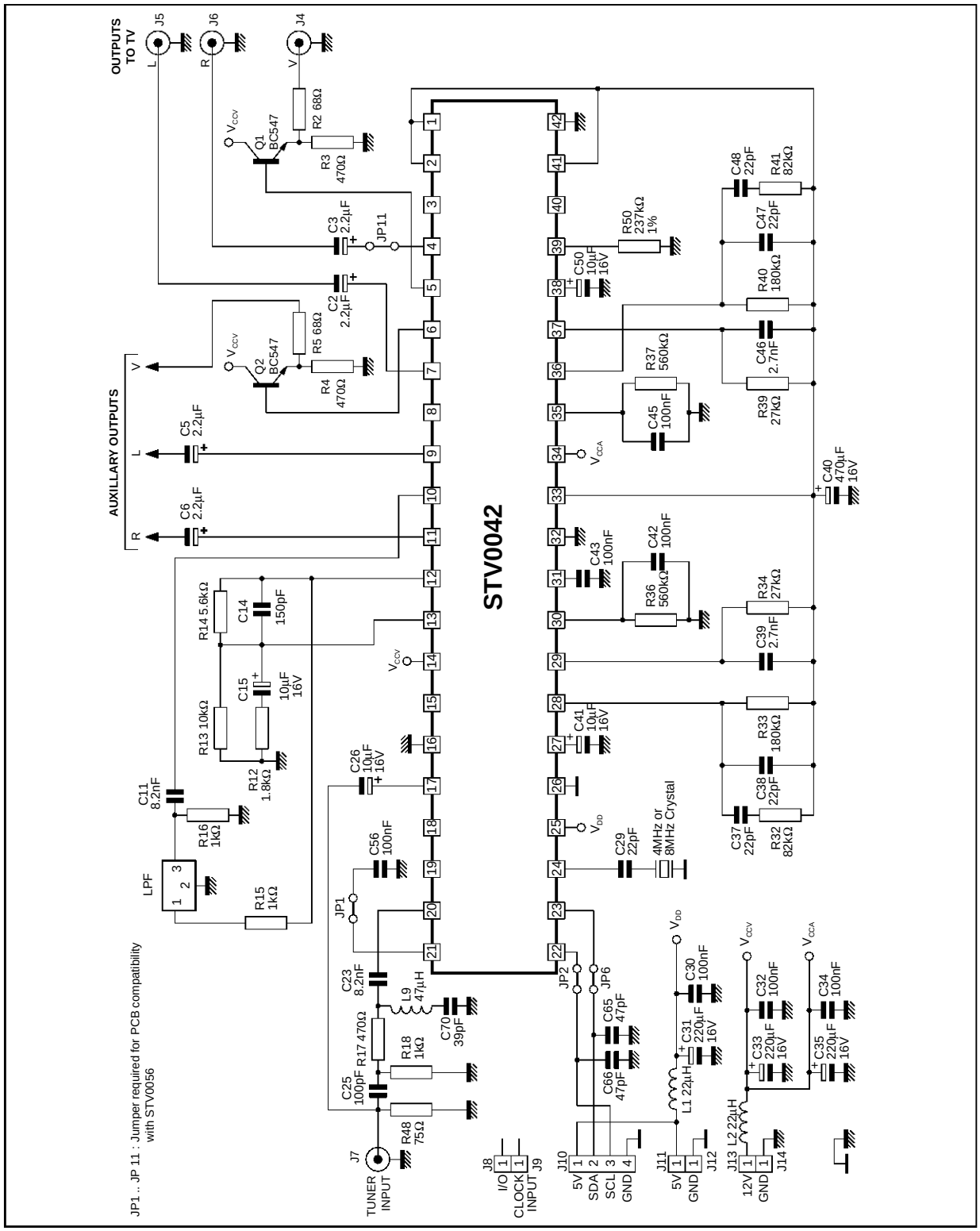
Figure 35



7 - TYPICAL APPLICATIONS DIAGRAMS (continued)

7.3 - STV0042 : PAL M / Brazil Application (Figure 36)

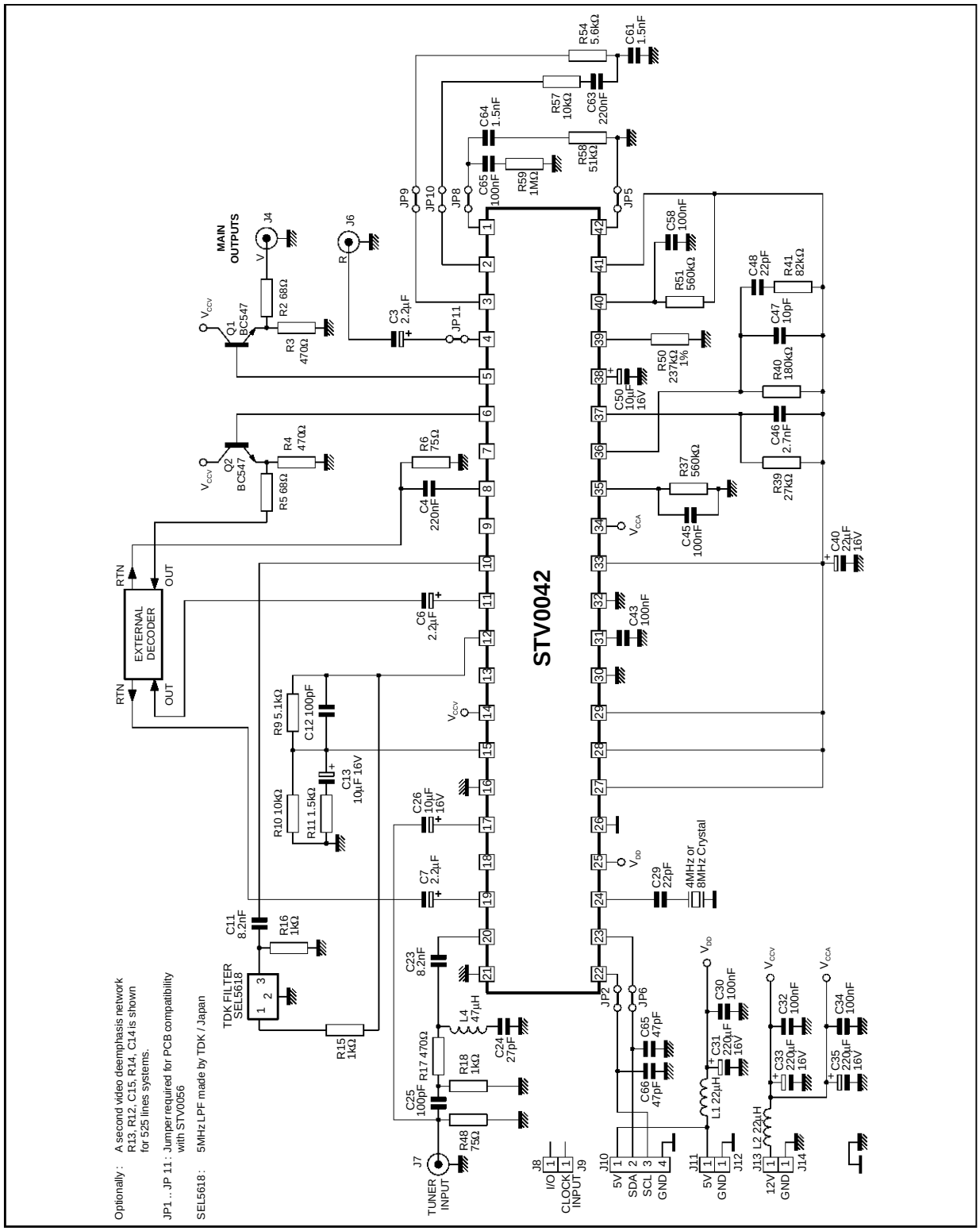
Figure 36



7 - TYPICAL APPLICATIONS DIAGRAMS (continued)

7.4 - STV0042 : Audio Mono Application, with Simplified Audio Noise Reduction (Figure 37)

Figure 37



8 - POTENTIAL PROBLEM AND SUGGESTED SOLUTIONS

This chapter deals with potential problems or undesired effects in the application and suggests solutions.

Remark : SGS-THOMSON will improve points 8.2, 8.4, 8.7 which directly depend on the STV42/56 circuit.

8.1 - Sound Cracking and Distorted Sibilance

When the characteristics of the PLL demodulator are not optimized, two effects may happen :

- Distorted sibilance ("S" sounds are emphazed) : this corresponds to a too narrow lock range.
- Small crackles (click) : this corresponds to a too wide capture range.

If such effects appear, it is important to check that the PLL gain is properly calibrated. To do so, a test signal is supplied to FM IN, and a $1V_{PP} \pm 8\%$ ideally (or $\pm 10\%$ can be accepted) must be found on the DET Pin.

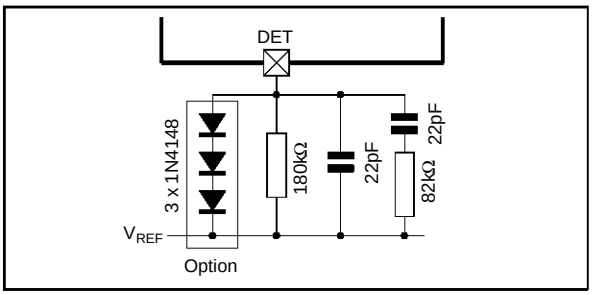
Test Signal : FM subcarrier : $\pm$ 50kHz full deviation, 400Hz modulating frequency

Very likely, a too large signal on DET Pin corresponds to distorded sibilance, and a too low signal corresponds to sound cracking.

After this test, the PLL calibration procedure must be optimized (see section 3.2.2.3).

Some crakles may remain on some paticular channels which slightly overmodulate. Normally this case is corrected inside the STV42/56 circuits by a clipping circuit which limits the DET Pin swing. To totally take out the remaining crakles, an external clipping circuit may be experimented (see Figure 38).

Figure 38 : Optional External Circuit to limit DET Signal Swing



8.2 - Audio Level with 50µs De-emphasis

Refering to the Section 3.3.2, the audio level and the actual roll-off frequency of the 50µs depends on an external filter and an internal resistor R_{int}.

Ideally the internal resistor value should be twice the value of the external resistor. Currently the situation is :

R_{int} = 30kΩ, R_{34} = 27kΩ (for left) (July 95).

This point will be corrected by SGS-THOMSON.

8.3 - Noisy Video Signal

If the selected tuner does not features a high rejection of the frequencies higher than 10MHz ; under certain conditions, it can be noticed an inter-modulation background noise in the video signal. One of the reasons of this effect is the wide band-width of the baseband input stage of the STV42/56 circuit which peaks or keeps some gain at frequencies as high as 25MHz.

SGS-THOMSON is evaluating this problem.

In the meantime, two solutions are suggested :

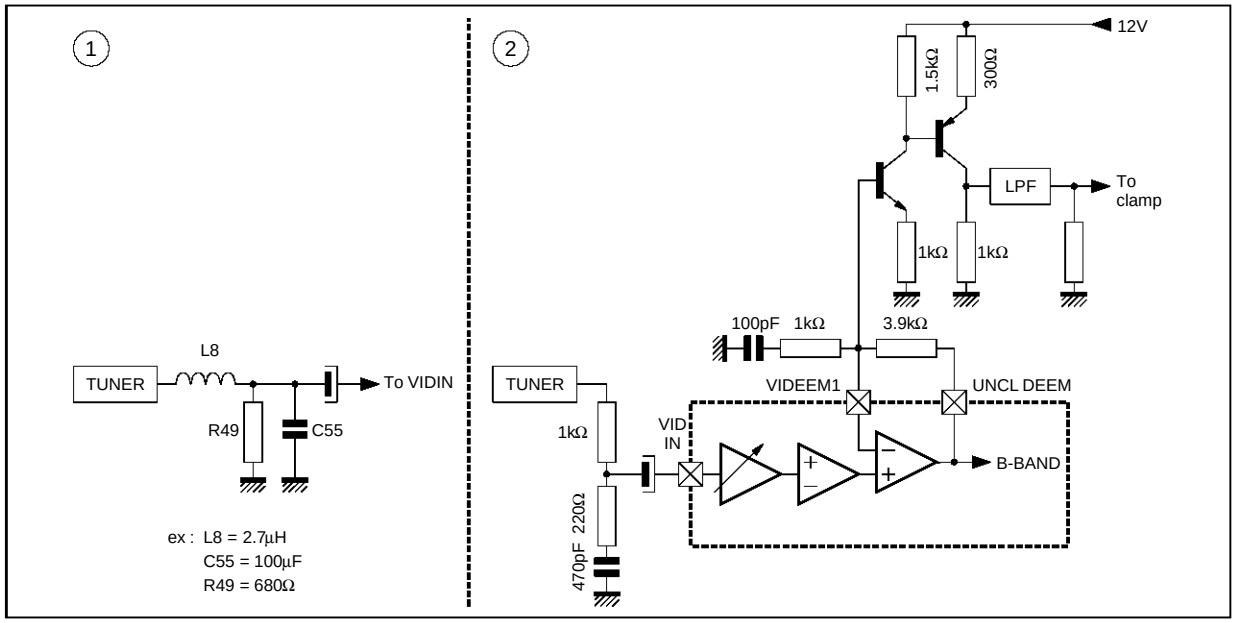
1) To implement an efficient low pass filter (roll-off at 10MHz) between the tuner and the base band input. A (R,L,C) filter can be used (see Figure 39-1)
2) To modify the typical video de-emphasized channel as follows : (see Figure 39-2)
   - Video de-emphasis is directly performed at the tuner output (R_a, Rb, R_c).
   - An the baseband signal is recovered by changing the de-emphasis amplifier into a pre-emphasis amplifier.
   - To get a $1V_{PP}$ output signal, and to recover the same phase as the baseband signal, a 2 transistors amplifier is implemented before the video LPF.

   This second solution provide a natural 14dB attenuation for all frequencies higher than the zero of the video pre-emphasis law, and makes the input stage working with lower amplitude signals.

Remark :
When the second solution is implemented, the baseband signal is selected by the de-emphazed video position of the switch matrix table.

8 - POTENTIAL PROBLEM AND SUGGESTED SOLUTIONS (continued)

Figure 39 : Back-up Solution, when some intermodulation noise is noticed



8.4 - 22kHz Tone Crosstalk on VIDEEM1

This potential problem and the suggested solution are mentioned in Sections 3.1.1.3, 3.4.4 and 3.5.6.

8.5 - Audio S/N, Influence of the Video Pattern

The S/N measurement conditions do not always describe which video pattern has to be used simultaneously with the audio.
When a color bar is displayed, the unweighted S/N is better than 63dB.
However when using patterns such as multiburst the S/N becomes lower (about 58dB). If it is required to get better than 63dB under this condition, then it is recommanded to used a more complex filter between the tuner and FM IN.
Figure 40 gives an example of a more sophisticated filter.

8.6 - STV0042 : Audio Level Modulation when Evaluating with a Signal Generator

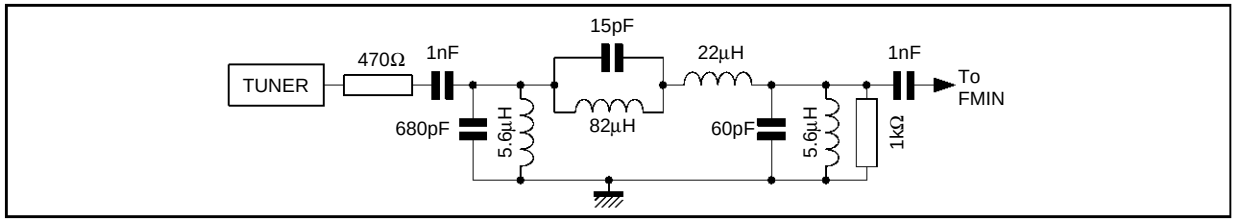
Refering to the block diagram of STV0042 noise reduction (see Figure 19 of Section 3.3.1). The signal at SUMOUT is the sum of the left and right signals.
When using signal generators it may happen that left and right signals are exactly in opposite phase or slowly beat. In such a case the SUMOUT signal becomes null and consequently the signal at PKOUT becomes low and the output amplifier have a low frequency response.
The final result is an amplitude modulation of the audio output signal.
This is a very specific case which may happen only when using signal generator and which likely never occurs in reality.

8.7 - Video Output, Limited Slew-rate

The video output stages of STV42/56 are internally pulled down with 1.3mA current sources.
This pulling down source may not be enough when the external load becomes highly capacitive ($C_{load} \geq 20pF$).

SGS-THOMSON will correct this effect.
In the meantime, when this problem is faced, pull-down resistors ($\approx 2.2k\Omega$) can be connected between the ground and the video outputs.

Figure 40 : More Sophisticated Video Rejection Filter

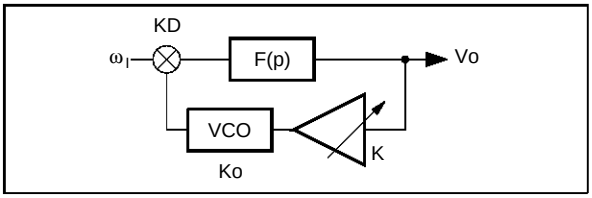


9 - ANNEXE : PLL DEMODULATOR THEORETICAL ANALYSIS

9.1 - Modelization of the STV42/56 FM Demodulator

A part from the AGC section, the FM demodulator of the STV42/56 can be modelized as a conventional PLL structure (see Figure 41).

Figure 41



The closed loop gain of the PLL is :

$$\left(\frac{V_O}{\omega_I}\right)(p) = \frac{1}{K \cdot KO} \cdot \frac{1}{1 + \frac{p}{K \cdot KO \cdot K_D}} \quad (1)$$

$\omega_I = 2\pi (f(t) - f_O)$ in radians
V_O : peak-to-peak output voltage
K : modulation depth coefficient (R05 B0-5)
Ko : VCO slope (in radians per volt)
K_D : Phase detector gain (volt per radian)

Remark : The phase detector gain can be determined as follows :

$$K_D = DETH \cdot \frac{R_{33}}{R_{36}} \cdot \sin\Phi \text{ (left channel)}$$

Φ : the angle difference between incoming signal and the VCO

The relation (1) shows that the DC gain of the PLL is :

$$G_{DC} = \frac{1}{K \cdot KO}$$

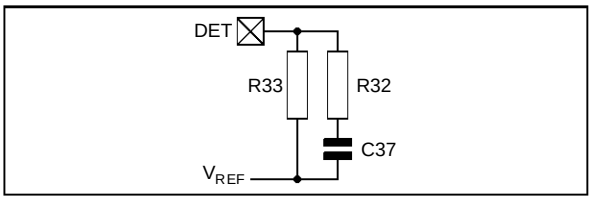
Typically the STV42/56 has been designed with :

$$KO = 2.89 \cdot 10^6 \text{ radians/volt}$$

9.2 - Frequency Response of the PLL Demodulator

In standard applications the STV42/56 is used with the following external loop filter (left channel).

Figure 42



With this type of filter the PLL closed loop gain becomes a second order low pass filter which can be compared to the following :

$$\left(\frac{V_O}{\omega_I}\right)(p) = \frac{1}{1 + 2\frac{\xi}{\omega_O} + \frac{p}{\omega_O}} \quad (2)$$

ξ : damping factor
ω_O : resonnating frequency (for $\xi = 0$)

Comparing relations (1) and (2), the damping factor and the resonnating frequency can be calculated as follows :

$$\omega_N = \sqrt{\frac{K \cdot KO \cdot K_D}{(R_{33} + R_{32}) \cdot C_{37}}}$$

$$\xi = \frac{1}{\sqrt{K \cdot KO \cdot K_D (R_{33} + R_{32}) C_{37}}} + R_{82}\sqrt{\frac{K \cdot KO \cdot K_D}{R_{33} + R_{32}}}$$

9.3 - Lock Range and Capture Range

Lock Range : $\omega_L = KO \cdot K \cdot K_D$

Capture Range : $\omega_C \approx \sqrt{\frac{\omega_L}{(R_{33} + R_{32}) \cdot C_{37}}}$