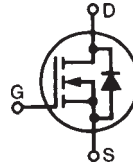


PolarHT™ Power MOSFET

IXTK 200N10P

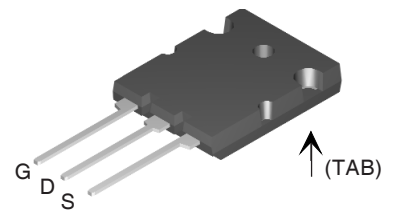
$$\begin{aligned} V_{DSS} &= 100 \text{ V} \\ I_{D25} &= 200 \text{ A} \\ R_{DS(on)} &= 7.5 \text{ m}\Omega \end{aligned}$$

N-Channel Enhancement Mode



Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ\text{C}$ to 175°C	100	V
V_{DGR}	$T_J = 25^\circ\text{C}$ to 175°C ; $R_{GS} = 1 \text{ M}\Omega$	100	V
V_{GSM}		± 20	V
I_{D25}	$T_C = 25^\circ\text{C}$	200	A
$I_{D(RMS)}$	External lead current limit	75	A
I_{DM}	$T_C = 25^\circ\text{C}$, pulse width limited by T_{JM}	400	A
I_{AR}	$T_C = 25^\circ\text{C}$	60	A
E_{AR}	$T_C = 25^\circ\text{C}$	100	mJ
E_{AS}	$T_C = 25^\circ\text{C}$	4	J
dv/dt	$I_S \leq I_{DM}$, $di/dt \leq 100 \text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DSS}$, $T_J \leq 150^\circ\text{C}$, $R_G = 4 \Omega$	10	V/ns
P_D	$T_C = 25^\circ\text{C}$	800	W
T_J		-55 ... +175	$^\circ\text{C}$
T_{JM}		175	$^\circ\text{C}$
T_{stg}		-55 ... +150	$^\circ\text{C}$
T_L	1.6 mm (0.062 in.) from case for 10 s	300	$^\circ\text{C}$
M_d	Mounting torque	1.13/10 Nm/lb.in.	
Weight		10	g

TO-264(SP) (IXTK)



G = Gate D = Drain
S = Source TAB = Drain

Features

- International standard packages
- Unclamped Inductive Switching (UIS) rated
- Low package inductance
 - easy to drive and to protect

Advantages

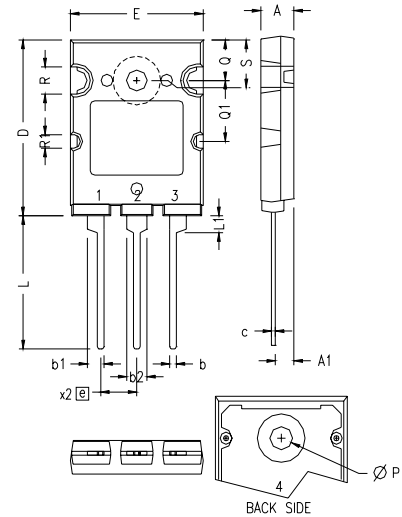
- Easy to mount
- Space savings
- High power density

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, unless otherwise specified)	Characteristic Values		
		Min.	Typ.	Max.
V_{DSS}	$V_{GS} = 0 \text{ V}$, $I_D = 250 \mu\text{A}$	100		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 500 \mu\text{A}$	2.5		5.0 V
I_{GSS}	$V_{GS} = \pm 20 \text{ V}_{DC}$, $V_{DS} = 0$			$\pm 200 \text{ nA}$
I_{DSS}	$V_{DS} = V_{DSS}$ $V_{GS} = 0 \text{ V}$ $T_J = 150^\circ\text{C}$			25 μA 250 μA
$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$, $I_D = 0.5 I_{D25}$ $V_{GS} = 15 \text{ V}$, $I_D = 400 \text{ A}$ Pulse test, $t \leq 300 \mu\text{s}$, duty cycle $d \leq 2\%$	5.5		7.5 $\text{m}\Omega$ $\text{m}\Omega$

PolarHT™ DMOS transistors utilize proprietary designs and process. US patent is pending.

Symbol	Test Conditions	Characteristic Values		
		(T _J = 25°C, unless otherwise specified)		
		Min.	Typ.	Max.
g_{fs}	V _{DS} = 10 V; I _D = 0.5 I _{D25} , pulse test	60	97	S
C_{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1 MHz		7600	pF
C_{oss}			2900	pF
C_{rss}			860	pF
t_{d(on)}	V _{GS} = 10 V, V _{DS} = 0.5 V _{DSS} , I _D = 60 A R _G = 3.3 Ω (External)		30	ns
t_r			35	ns
t_{d(off)}			150	ns
t_f			90	ns
Q_{g(on)}	V _{GS} = 10 V, V _{DS} = 0.5 V _{DSS} , I _D = 0.5 I _{D25}		240	nC
Q_{gs}			50	nC
Q_{gd}			135	nC
R_{thJC}				0.18 K/W
R_{thCK}		0.15		K/W

Symbol	Test Conditions	Characteristic Values		
		(T _J = 25°C, unless otherwise specified)		
		Min.	typ.	Max.
I_s	V _{GS} = 0 V			200 A
I_{SM}	Repetitive			400 A
V_{SD}	I _F = I _S , V _{GS} = 0 V, Pulse test, t ≤ 300 μs, duty cycle d ≤ 2 %			1.5 V
t_{rr}	I _F = 25 A -di/dt = 100 A/μs		120	ns
Q_{RM}		V _R = 100 V		3.3

TO-264(SP) Outline (IXTK)


SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.185	.209	4.70	5.30
A1	.102	.118	2.60	3.00
b	.035	.049	0.90	1.25
b1	.091	.106	2.30	2.70
b2	.110	.126	2.80	3.20
c	.020	.033	0.50	0.85
D	1.012	1.035	25.70	26.30
E	.776	.799	19.70	20.30
e	.215BSC		5.46 BSC	
L	.768	.807	19.50	20.50
L1	.091	.106	2.30	2.70
ØP	.122	.138	3.10	3.50
Q	.228	.244	5.80	6.20
Q1	.346	.362	8.80	9.20
ØR	.150	.165	3.80	4.20
ØR1	.071	.087	1.80	2.20
S	.228	.244	5.80	6.20

- 1 - GATE
- 2, 4 - DRAIN (COLLECTOR)
- 3 - SOURCE (EMITTER)

NOTE: Leads and back heatsink are solder plated.

IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585
	4,850,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	

Fig. 1. Output Characteristics @ 25°C

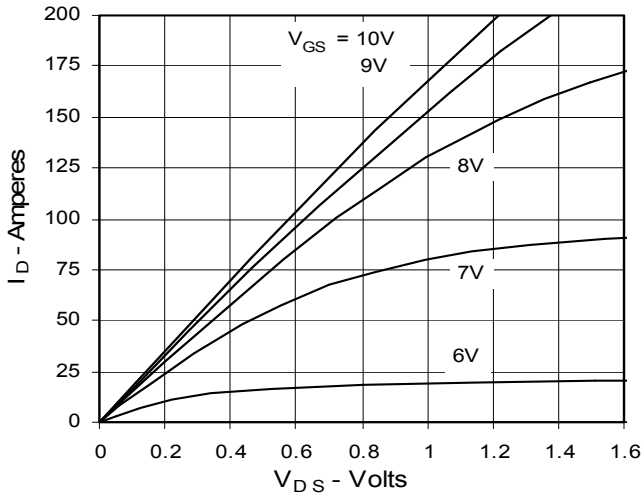


Fig. 2. Extended Output Characteristics @ 25°C

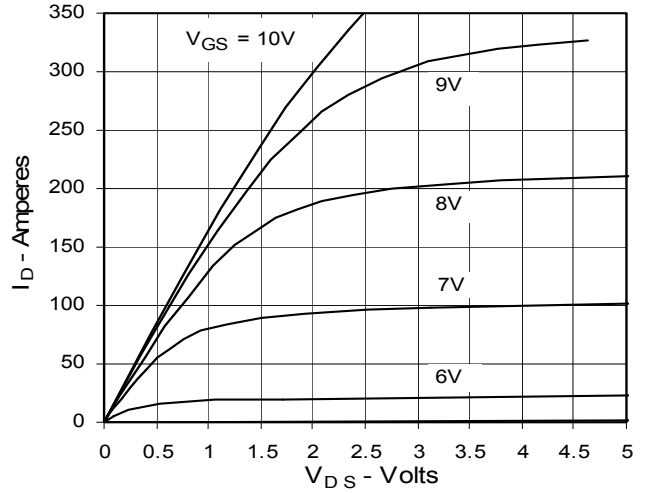


Fig. 3. Output Characteristics @ 150°C

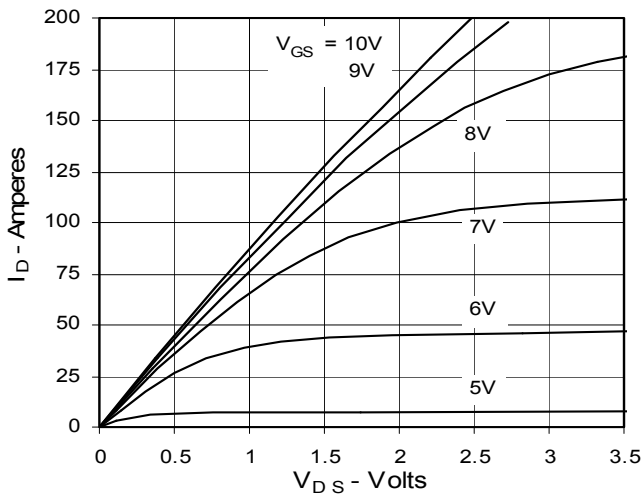


Fig. 4. $R_{DS(on)}$ Normalized to 0.5 I_{D25} Value vs. Junction Temperature

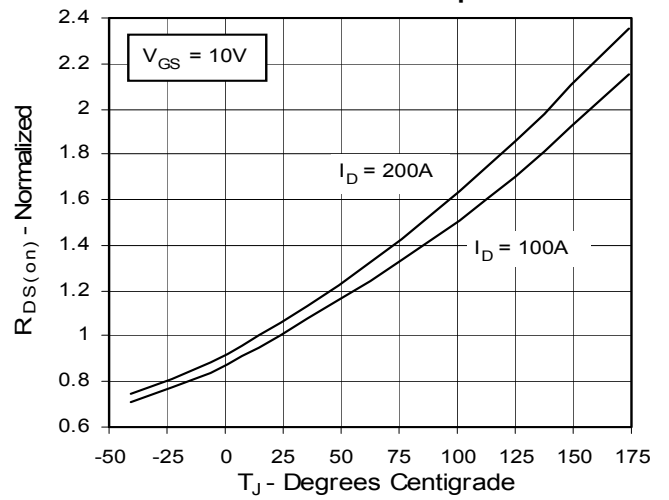


Fig. 5. $R_{DS(on)}$ Normalized to 0.5 I_{D25} Value vs. Drain Current

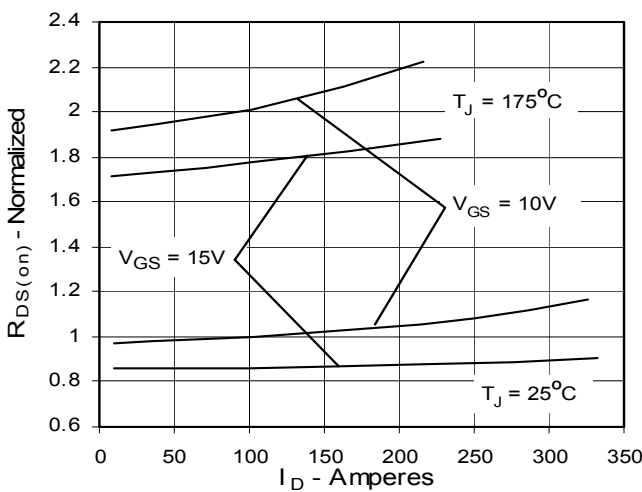


Fig. 6. Drain Current vs. Case Temperature

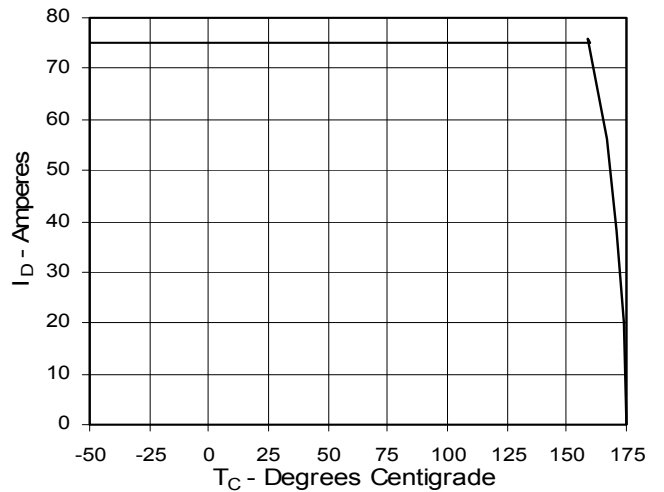


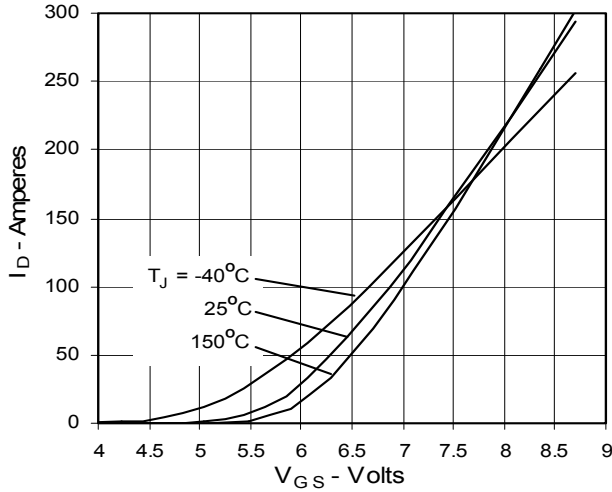
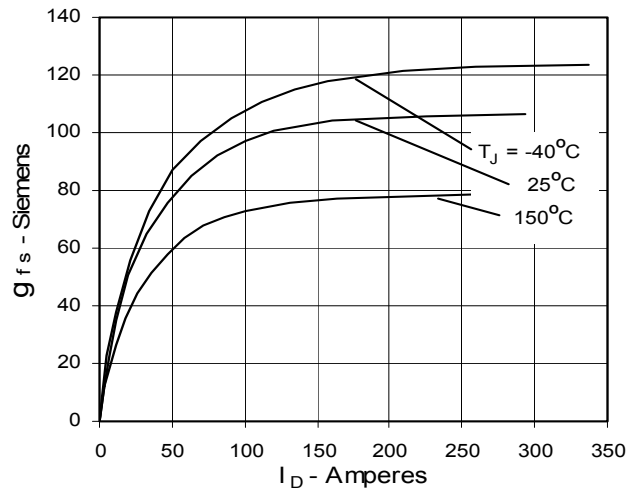
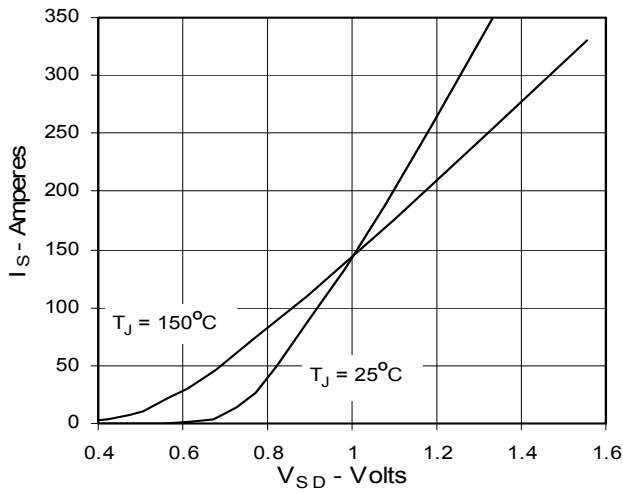
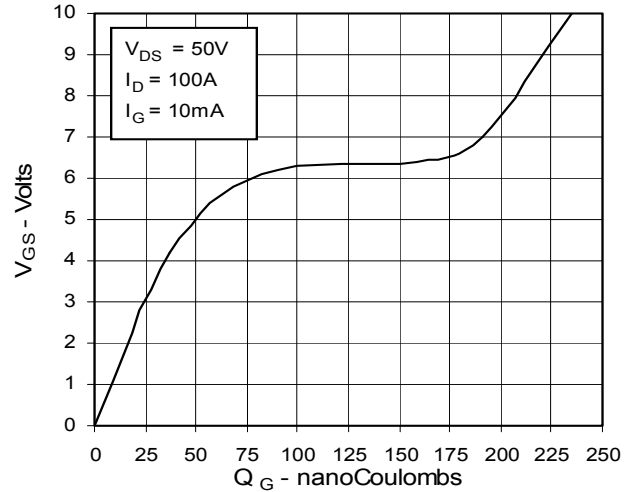
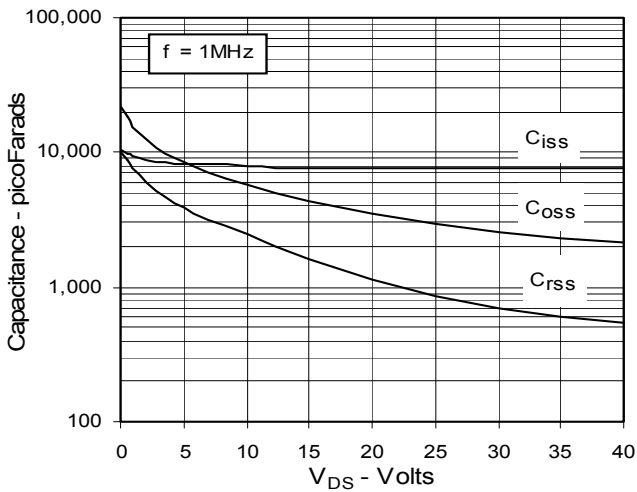
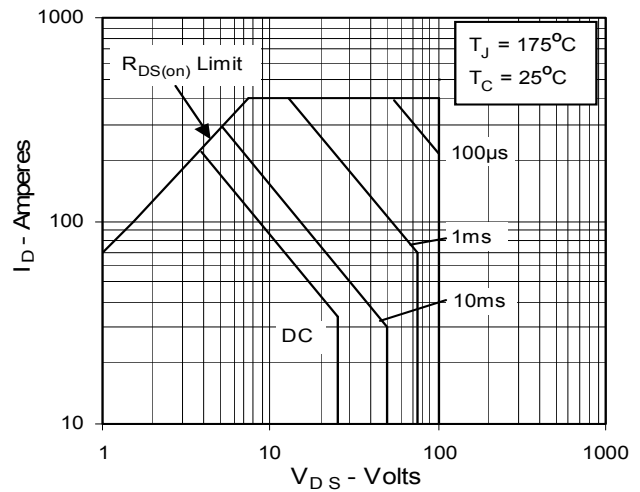
Fig. 7. Input Admittance

Fig. 8. Transconductance

Fig. 9. Source Current vs. Source-To-Drain Voltage

Fig. 10. Gate Charge

Fig. 11. Capacitance

Fig. 12. Forward-Bias Safe Operating Area


Fig. 13. Maximum Transient Thermal Resistance

