IS61LV12824

128K x 24 HIGH-SPEED CMOS STATIC RAM WITH 3.3V SUPPLY

FEATURES

- High-speed access time: 8, 9, 10, 12 ns
- CMOS low power operation
  - 720 mW (typical) operating @ 9 ns
  - 36 mW (typical) standby @ 9 ns
- TTL compatible interface levels
- Single 3.3V power supply
- Fully static operation: no clock or refresh required
- Three state outputs
- Available in 119-pin 14x22mm PBGA

DESCRIPTION

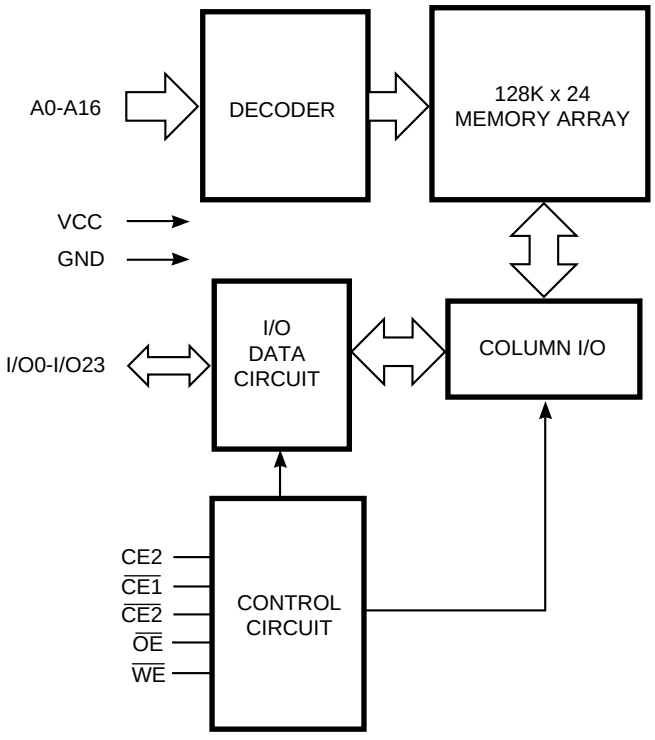
The *ICSI* IS61LV12824 is a high-speed, static RAM organized as 131,072 words by 24 bits. It is fabricated using *ICSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 8 ns with low power consumption.

When $\overline{CE1}$, $\overline{CE2}$ are HIGH and CE2 is LOW (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs, $\overline{CE1}$, CE2, $\overline{CE2}$ and $\overline{OE}$. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory.

The IS61LV12824 is packaged in the JEDEC standard 119-pin 14*22mm PBGA.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION
119-pin 14x22mm PBGA

	1	2	3	4	5	6	7
A	NC	A11	A14	A15	A16	A4	NC
B	NC	A12	A13	$\overline{CE1}$	A5	A3	NC
C	I/O16	NC	CE2	NC	$\overline{CE2}$	NC	I/O0
D	I/O17	V_{CCQ}	GND	GND	GND	V_{CCQ}	I/O1
E	I/O18	GND	V_{CC}	GND	V_{CC}	GND	I/O2
F	I/O19	V_{CCQ}	GND	GND	GND	V_{CCQ}	I/O3
G	I/O20	GND	V_{CC}	GND	V_{CC}	GND	I/O4
H	I/O21	V_{CCQ}	GND	GND	GND	V_{CCQ}	I/O5
J	V_{CCQ}	GND	V_{CC}	GND	V_{CC}	GND	V_{CCQ}
K	I/O22	V_{CCQ}	GND	GND	GND	V_{CCQ}	I/O6
L	I/O23	GND	V_{CC}	GND	V_{CC}	GND	I/O7
M	I/O12	V_{CCQ}	GND	GND	GND	V_{CCQ}	I/O8
N	I/O13	GND	V_{CC}	GND	V_{CC}	GND	I/O9
P	I/O14	V_{CCQ}	GND	GND	GND	V_{CCQ}	I/O10
R	I/O15	NC	NC	NC	NC	NC	I/O11
T	NC	A10	A8	$\overline{WE}$	A0	A1	NC
U	NC	A9	A7	$\overline{OE}$	A6	A2	NC

PIN DESCRIPTIONS

A0-A16	Address Inputs
I/O0-I/O23	Data Inputs/Outputs
$\overline{CE1}$, $\overline{CE2}$	Chip Enable Input LOW
CE2	Chip Enable Input HIGH
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
NC	No Connection
Vcc	Power
V_{CCQ}	I/O Power
GND	Ground

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE1}$	CE2	$\overline{CE2}$	$\overline{OE}$	I/O0-I/O23	Vcc Current
Not Selected	X	H	X	X	X	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	L	H	High-Z	I_{CC}
	X	L	H	L	X	High-Z	
Read	H	L	H	L	L	D_{OUT}	1$_{CC}$
	H	L	H	L	H	High-Z	
Write	L	L	H	L	X	D_{IN}	I_{CC}
	L	L	H	L	H	H_{IHG}-Z	

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter		Value	Unit
V_{CC}	Power Supply Voltage Relative to GND		–0.5 to 5.0	V
V_{TERM}	Terminal Voltage with Respect to GND		–0.5 to Vcc + 0.5	V
T_{STG}	Storage Temperature		–65 to + 150	°C
T_{BIAS}	Temperature Under Bias:	Com.	–10 to + 85	°C
		Ind.	–45 to + 90	°C
P_T	Power Dissipation		2.0	W
I_{OUT}	DC Output Current		±20	mA

Note:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	Vcc (8, 9, 10 ns)	Vcc (12 ns)
Commercial	0°C to +70°C	3.3V + 10%, – 5%	3.3V ± 10%
Industrial	–40°C to +85°C	3.3V + 10%, – 5%	3.3V ± 10%

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA	2.4	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA	—	0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage(1)		–0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{CC}	–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{CC}, Outputs Disabled	–1	1	µA

Note:
1. V_{IL} (min.) = –0.3V DC; V_{IL} (min.) = –2.0V AC (pulse width ≤ 2.0 ns).
   V_{IH} (max.) = V_{CC} + 0.3V DC; V_{IH} (max.) = V_{CC} + 2.0V AC (pulse width ≤ 2.0 ns).

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-8 ns Min.	-8 ns Max.	-9 ns Min.	-9 ns Max.	-10 ns Min.	-10 ns Max.	-12 ns Min.	-12 ns Max.	Unit
I_{CC}	Vcc Dynamic Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX}	Com.	—	210	—	200	—	180	—	190	mA
			Ind.	—	—	—	220	—	210	—	190	
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{CC} = Max., $V_{IN} = V_{IH}$ or V_{IL}, f = 0 $\overline{CE1}$, $\overline{CE2}$, $\geq V_{IH}$, CE2 $\leq V_{IL}$	Com.	—	70	—	60	—	50	—	50	mA
			Ind.	—	70	—	70	—	55	—	55	
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{CC} = Max., $\overline{CE1}$, $\overline{CE2}$ $\geq V_{CC}$ – 0.2V, CE2 $\leq$ 0.2V, $V_{IN} \geq V_{CC}$ – 0.2V, or $V_{IN} \leq$ 0.2V, f = 0	Com.	—	10	—	10	—	10	—	10	mA
			Ind.	—	—	—	20	—	20	—	20	

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

CAPACITANCE[1]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	8	pF

Note:
1. Tested initially and after any design or process changes that may affect these parameters.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	2 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

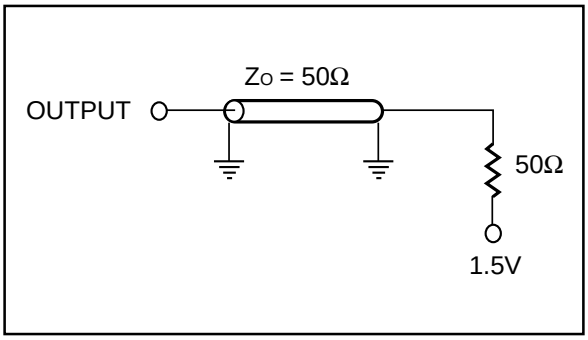


Figure 1

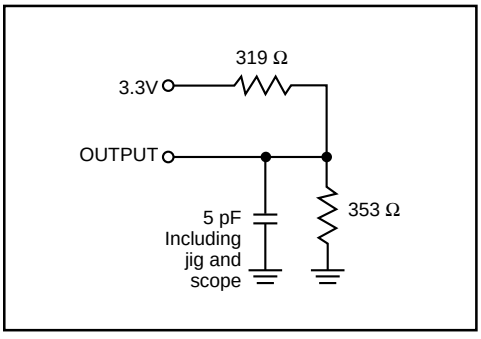


Figure 2

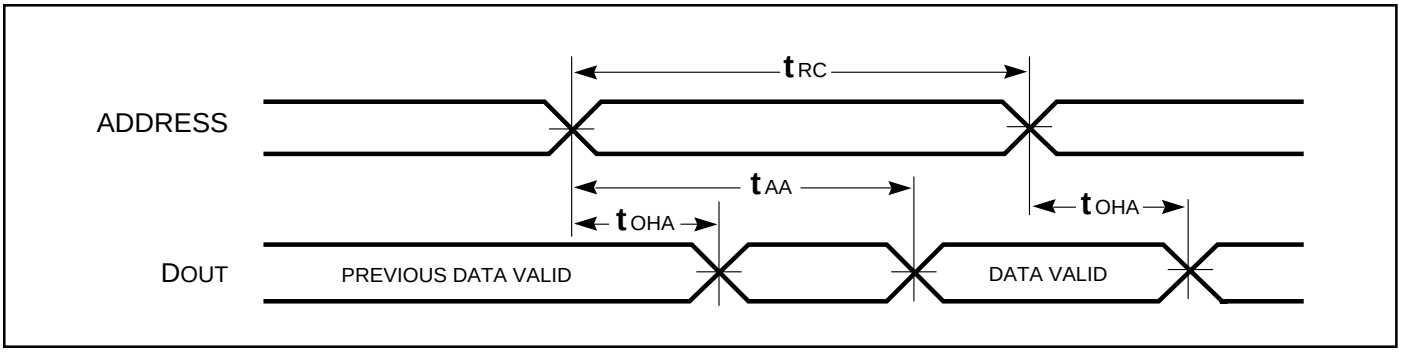
READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	-8 Min.	-8 Max.	-9 Min.	-9 Max.	-10 Min.	-10 Max.	-12 Min.	-12 Max.	Unit
t_{RC}	Read Cycle Time	9	—	10	—	12	—	15	—	ns
t_{AA}	Address Access Time	—	9	—	10	—	12	—	15	ns
t_{OHA}	Output Hold Time	3	—	3	—	3	—	3	—	ns
t_{ACE} t_{ACE2}	$\overline{CE1}$, $\overline{CE2}$ Access Time CE2 Access Time	—	8	—	9	—	10	—	12	ns
t_{DOE}	$\overline{OE}$ Access Time	—	4	—	4	—	4	—	4	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	0	5	0	5	0	6	0	7	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	0	—	0	—	0	—	0	—	ns
t_{HZCE}[2] t_{HZCE2}[2]	$\overline{CE1}$, $\overline{CE2}$ to High-Z Output CE2 to High-Z Output	0	5	0	5	0	6	0	7	ns
t_{LZCE}[2] t_{LZCE2}[2]	$\overline{CE}$, $\overline{CE2}$ to Low-Z Output CE2 to Low-Z Output	3	—	3	—	3	—	3	—	ns

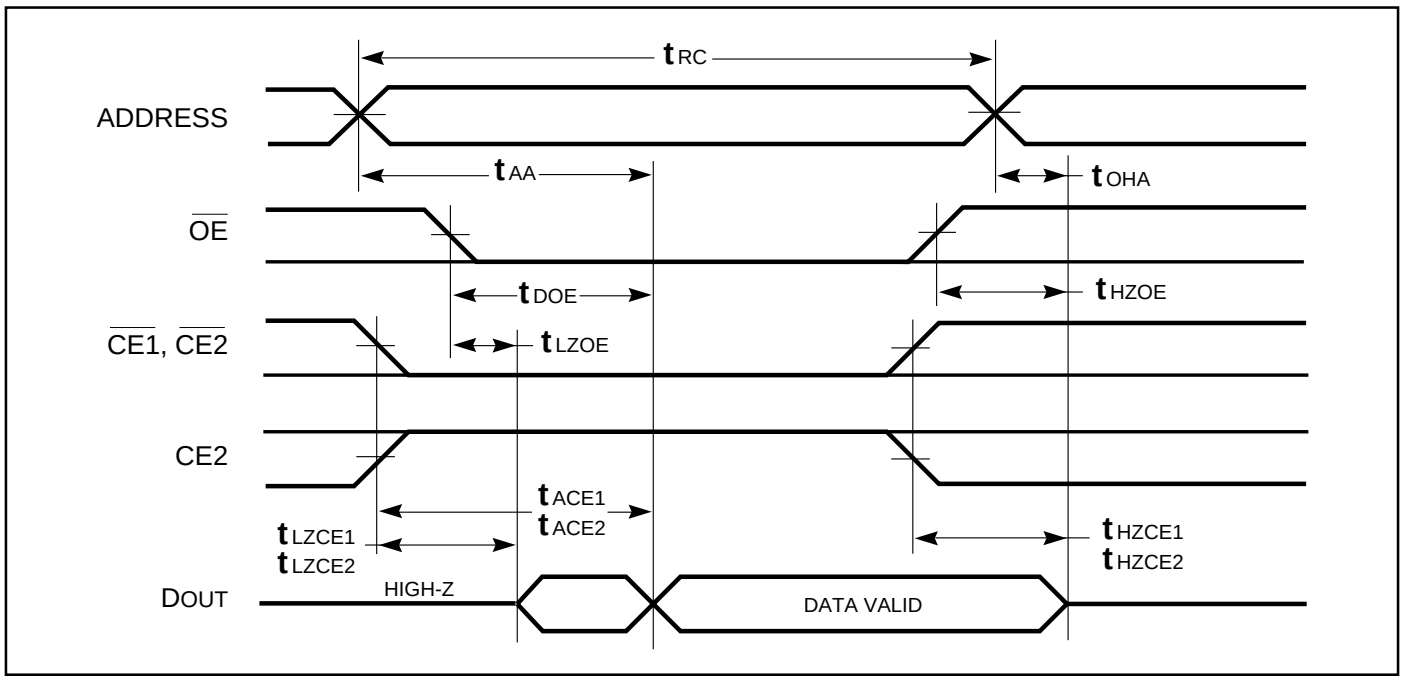
Notes:
1. Test conditions assume signal transition times of 2 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±200 mV from steady-state voltage. Not 100% tested.

AC WAVEFORMS

READ CYCLE NO. 1[1,2] (Address Controlled) ($\overline{CE1}$ = $\overline{CE2}$ = $\overline{OE}$ = V_{IL}; CE2 = V_{IH})



READ CYCLE NO. 2[1,3]



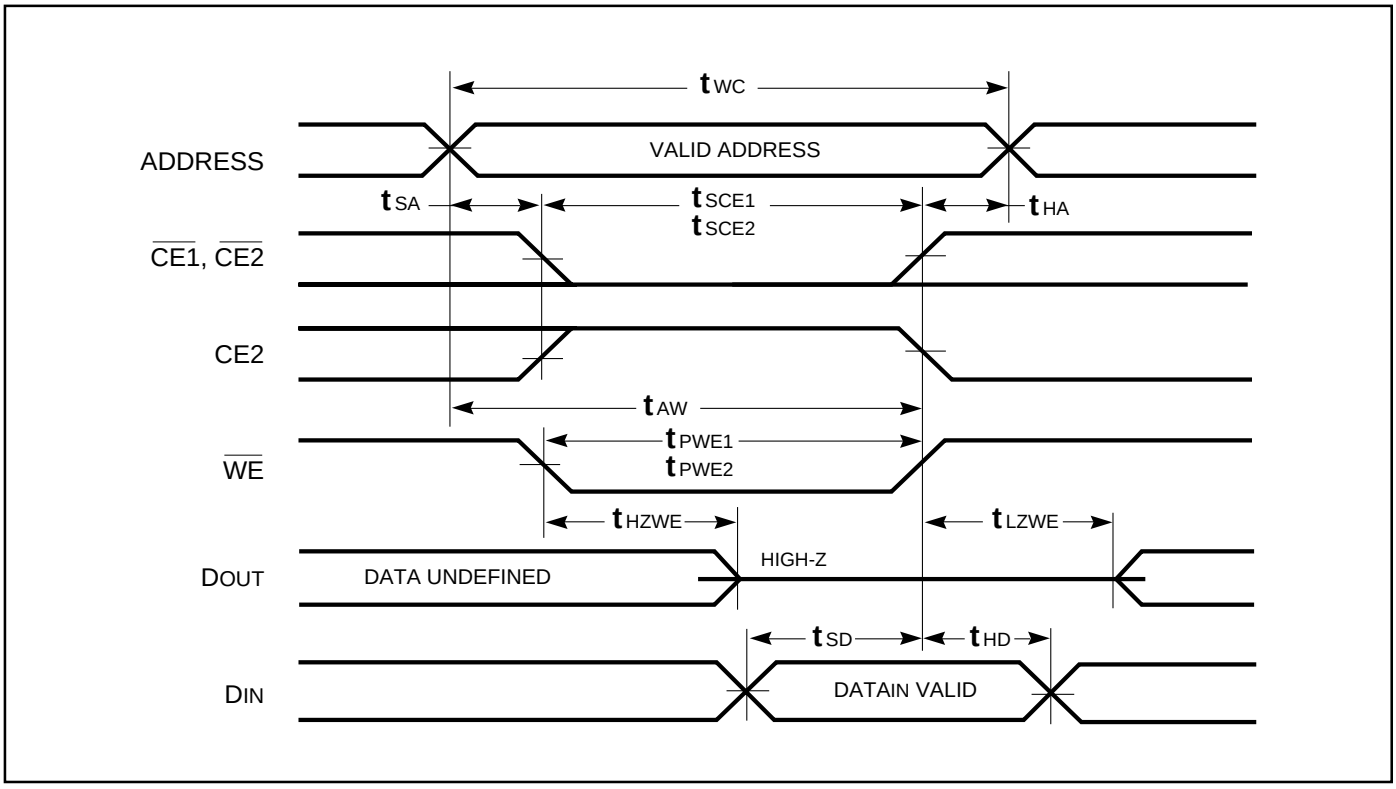
Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE1}$, $\overline{CE2}$ = V_{IL}. CE2 = V_{IH}.
3. Address is valid prior to or coincident with $\overline{CE1}$, $\overline{CE2}$ LOW and CE2 HIGH transition.

WRITE CYCLE SWITCHING CHARACTERISTICS[1,3] (Over Operating Range)

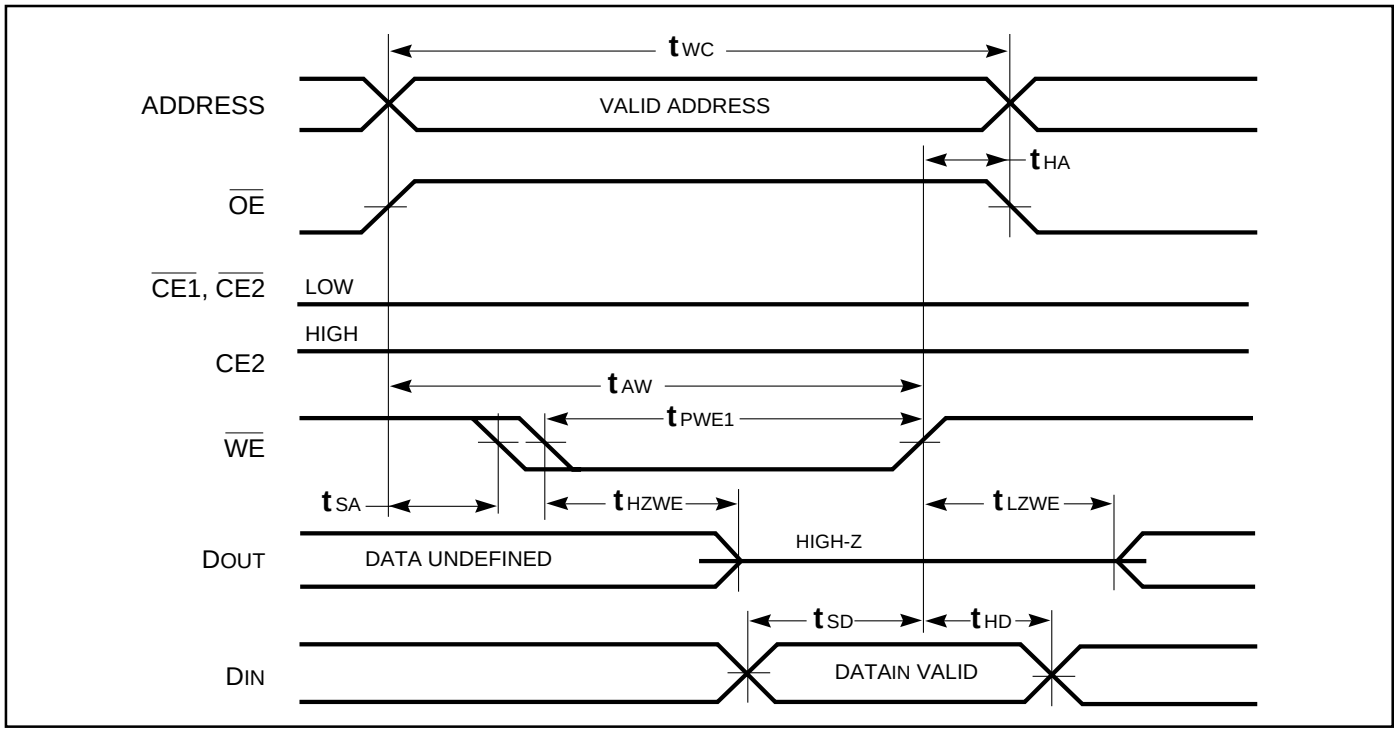
Symbol	Parameter	-8 Min.	-8 Max.	-9 Min.	-9 Max.	-10 Min.	-10 Max.	-12 Min.	-12 Max.	Unit
t_{WC}	Write Cycle Time	8	—	9	—	10	—	12	—	ns
t_{SCE}	$\overline{CE1}$, $\overline{CE2}$ to Write End	7	—	8	—	8	—	9	—	ns
t_{SCE2}	CE2 to Write End	7	—	8	—	8	—	9	—	
t_{AW}	Address Setup Time to Write End	7	—	8	—	8	—	9	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	0	—	0	—	ns
t_{PWE1}	$\overline{WE}$ Pulse Width ($\overline{OE}$ = HIGH)	6	—	8	—	8	—	9	—	ns
t_{PWE2}	$\overline{WE}$ Pulse Width ($\overline{OE}$ = LOW)	6	—	9	—	9	—	10	—	ns
t_{SD}	Data Setup to Write End	4.5	—	5	—	5	—	5	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	0	—	0	—	ns
t_{HZWE}[2]	$\overline{WE}$ LOW to High-Z Output	—	3.5	—	3.5	—	3.5	—	3.5	ns
t_{LZWE}[2]	$\overline{WE}$ HIGH to Low-Z Output	3	—	3	—	3	—	3	—	ns

Notes:
1. Test conditions assume signal transition times of 2 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±200 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE1}$, $\overline{CE2}$ LOW, CE2 HIGH and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

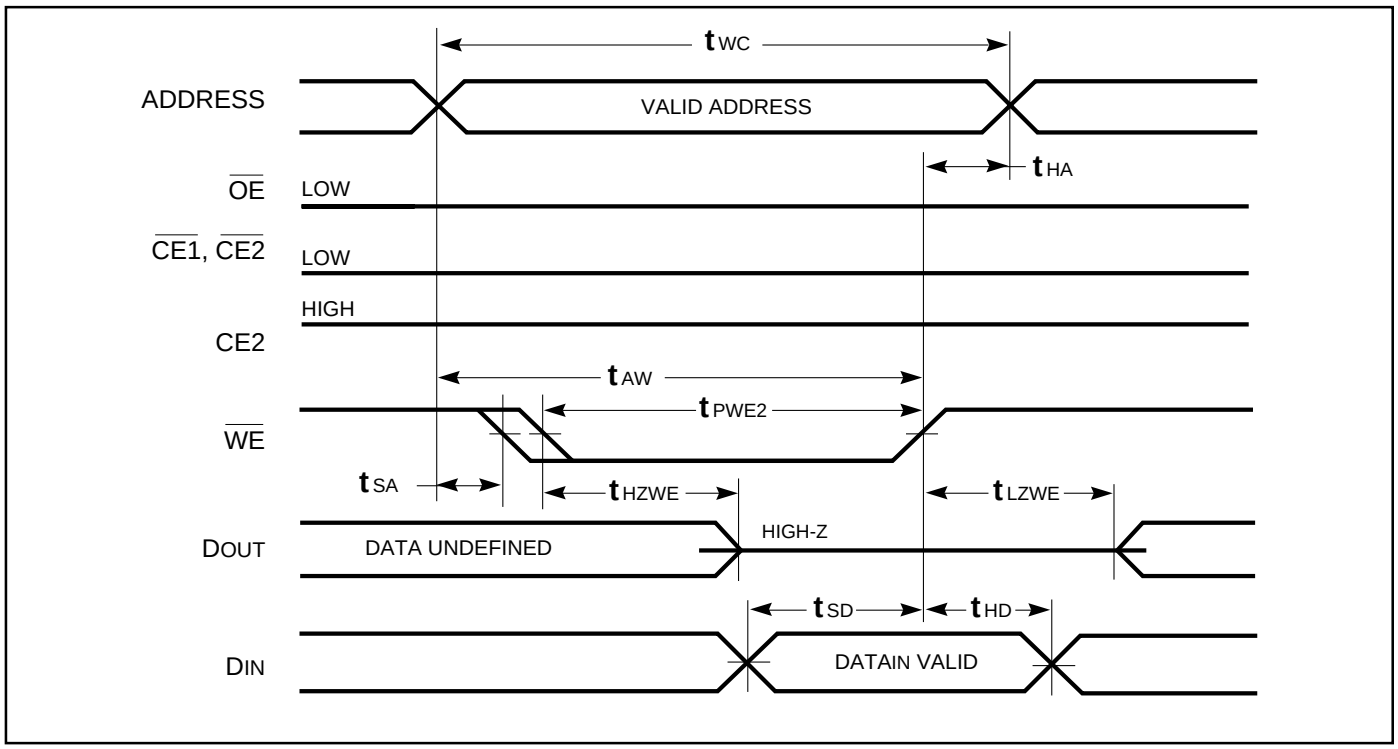
WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)



WRITE CYCLE NO. 2[1] ($\overline{CE}$ Controlled: $\overline{OE}$ = HIGH or LOW: $\overline{CE1}$, $\overline{CE2}$ or CE2 Terminates Write)



WRITE CYCLE NO. 2[1] ($\overline{WE}$ Controlled: $\overline{OE}$ = LOW, $\overline{CE1}$, $\overline{CE2}$ = LOW; CE2 = HIGH: $\overline{WE}$ TEMINATES WRITE)



Note:

1. The internal Write time is defined by the overlap of $\overline{CE1}$ and $\overline{CE2}$ = LOW, CE2 = HIGH and $\overline{WE}$ = LOW. All signals must be in valid states to initiate a Write, but any can be deasserted to terminate the Write. The Data Input Setup and Hold timing is referenced to the rising or falling edge of the signal that terminates the Write.

ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
8	IS61LV12824-8B	14*22mm PBGA
9	IS61LV12824-9B	14*22mm PBGA
10	IS61LV12824-10B	14*22mm PBGA
12	IS61LV12824-12B	14*22mm PBGA

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