

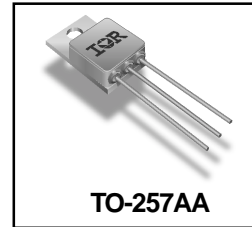
**POWER MOSFET  
 THRU-HOLE (TO-257AA)**

**IRFY9140C, IRFY9140CM  
 100V, P-CHANNEL**

**HEXFET<sup>®</sup> MOSFET TECHNOLOGY**

**Product Summary**

Part Number	R <sub>DS(on)</sub>	I <sub>D</sub>	Eyelets
IRFY9140C	0.20 Ω	-15.8A	Ceramic
IRFY9140CM	0.20 Ω	-15.8A	Ceramic



HEXFET<sup>®</sup> MOSFET technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry design achieves very low on-state resistance combined with high transconductance. HEXFET transistors also feature all of the well-established advantages of MOSFETs, such as voltage control, very fast switching, ease of paralleling and electrical parameter temperature stability. They are well-suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, high energy pulse circuits, and virtually any application where high reliability is required. The HEXFET transistor's totally isolated package eliminates the need for additional isolating material between the device and the heatsink. This improves thermal efficiency and reduces drain capacitance.

**Features:**

- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Electrically Isolated
- Ceramic Eyelets
- Ideally Suited For Space Level Applications

**Absolute Maximum Ratings**

	Parameter		Units
I <sub>D</sub> @ V <sub>GS</sub> = -10V, T <sub>C</sub> = 25°C	Continuous Drain Current	-15.8	A
I <sub>D</sub> @ V <sub>GS</sub> = -10V, T <sub>C</sub> = 100°C	Continuous Drain Current	-10	
I <sub>DM</sub>	Pulsed Drain Current ①	-60	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Max. Power Dissipation	100	W
	Linear Derating Factor	0.8	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	±20	V
E <sub>AS</sub>	Single Pulse Avalanche Energy ②	640	mJ
I <sub>AR</sub>	Avalanche Current ①	-15.8	A
E <sub>AR</sub>	Repetitive Avalanche Energy ①	10	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-5.5	V/ns
T <sub>J</sub>	Operating Junction	-55 to 150	°C
T <sub>STG</sub>	Storage Temperature Range		
	Lead Temperature	300(0.063in./1.6mm from case for 10 sec)	
	Weight	4.3 (Typical)	g

For footnotes refer to the last page

**Electrical Characteristics @ T<sub>j</sub> = 25°C (Unless Otherwise Specified)**

	Parameter	Min	Typ	Max	Units	Test Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	-100	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -1.0mA
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Temperature Coefficient of Breakdown Voltage	—	-0.1	—	V/°C	Reference to 25°C, I <sub>D</sub> = -1.0mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-State Resistance	—	—	0.20	Ω	V <sub>GS</sub> = -10V, I <sub>D</sub> = -10A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	-2.0	—	-4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA
g <sub>fs</sub>	Forward Transconductance	6.2	—	—	S (r <sub>θ</sub> )	V <sub>DS</sub> > -15V, I <sub>DS</sub> = -10A ④
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	—	—	-25	μA	V <sub>DS</sub> = -80V, V <sub>GS</sub> = 0V
		—	—	-250		V <sub>DS</sub> = -80V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Leakage Forward	—	—	-100	nA	V <sub>GS</sub> = -20V
I <sub>GSS</sub>	Gate-to-Source Leakage Reverse	—	—	100		V <sub>GS</sub> = 20V
Q <sub>g</sub>	Total Gate Charge	—	—	30	nC	V <sub>GS</sub> = -10V, I <sub>D</sub> = -15.8A V <sub>DS</sub> = -50V
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	7.1		
Q <sub>gd</sub>	Gate-to-Drain ('Miller') Charge	—	—	21		
t <sub>d(on)</sub>	Turn-On Delay Time	—	—	35	ns	V <sub>DD</sub> = -50V, I <sub>D</sub> = -15.8A, R <sub>G</sub> = 7.5Ω
t <sub>r</sub>	Rise Time	—	—	85		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	—	85		
t <sub>f</sub>	Fall Time	—	—	65		
L <sub>S</sub> + L <sub>D</sub>	Total Inductance	—	6.8	—	nH	Measured from drain lead (6mm/0.25in. from package) to source lead (6mm/0.25in. from package)
C <sub>iss</sub>	Input Capacitance	—	1400	—	pF	V <sub>GS</sub> = 0V, V <sub>DS</sub> = -25V f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	600	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	200	—		

**Source-Drain Diode Ratings and Characteristics**

	Parameter	Min	Typ	Max	Units	Test Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	-15.8	A	
I <sub>SM</sub>	Pulse Source Current (Body Diode) ①	—	—	-60		
V <sub>SD</sub>	Diode Forward Voltage	—	—	-4.2	V	T <sub>j</sub> = 25°C, I <sub>S</sub> = -15.8A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	—	280	nS	T <sub>j</sub> = 25°C, I <sub>F</sub> = -15.8A, di/dt ≤ -100A/μs
Q <sub>RR</sub>	Reverse Recovery Charge	—	—	3.6	μC	V <sub>DD</sub> ≤ -50V ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L <sub>S</sub> + L <sub>D</sub> .				

**Thermal Resistance**

	Parameter	Min	Typ	Max	Units	Test Conditions
R <sub>thJC</sub>	Junction-to-Case	—	—	1.25	°C/W	Typical socket mount
R <sub>thCS</sub>	Case-to-sink	—	0.21	—		
R <sub>thJA</sub>	Junction-to-Ambient	—	—	80		

**Note: Corresponding Spice and Saber models are available on the G&S Website.**

For footnotes refer to the last page

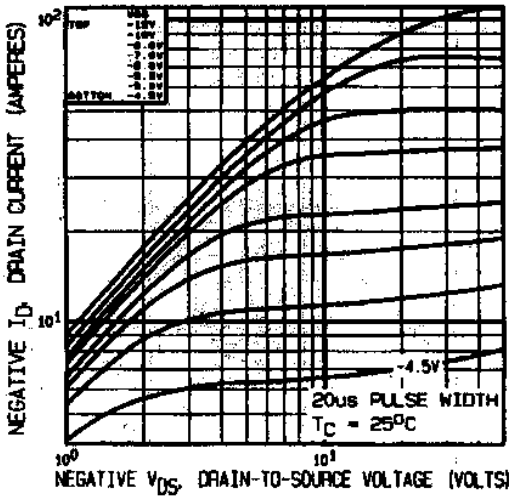


Fig 1. Typical Output Characteristics

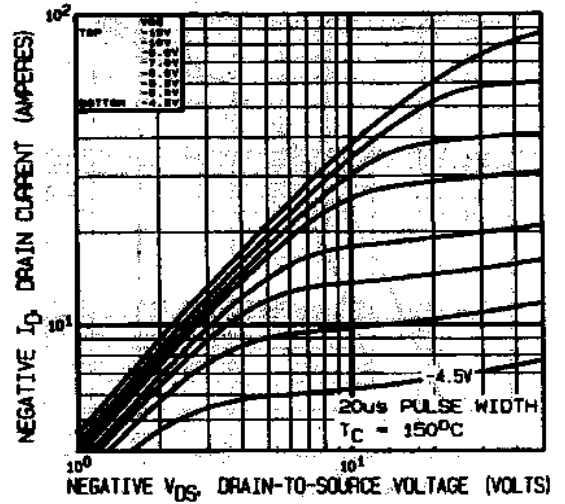


Fig 2. Typical Output Characteristics

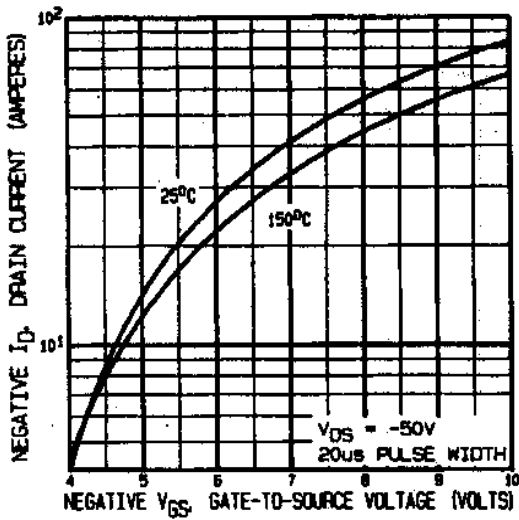


Fig 3. Typical Transfer Characteristics

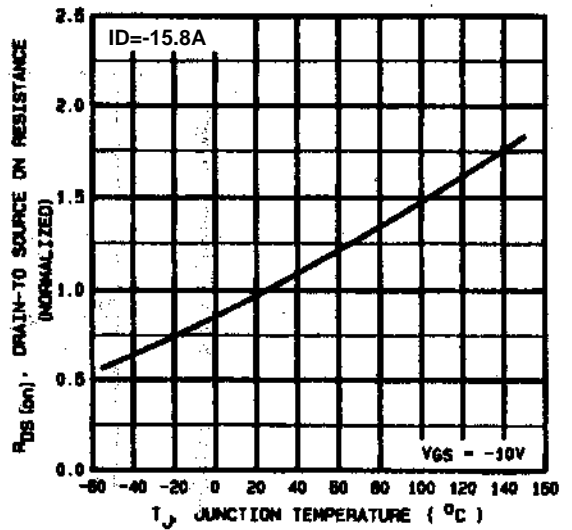


Fig 4. Normalized On-Resistance Vs. Temperature

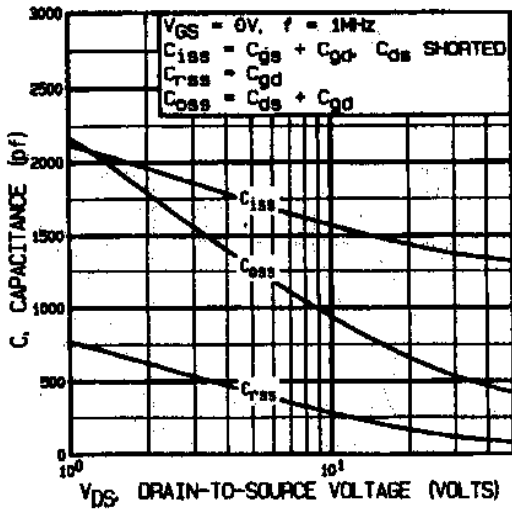


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

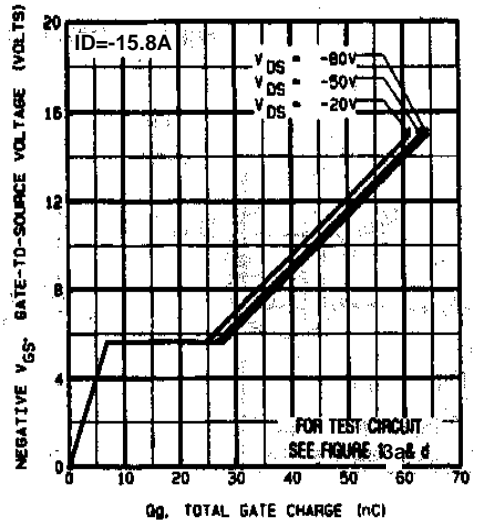


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

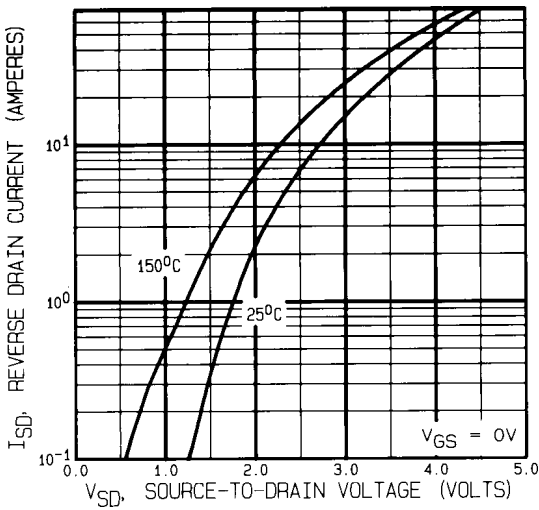


Fig 7. Typical Source-Drain Diode Forward Voltage

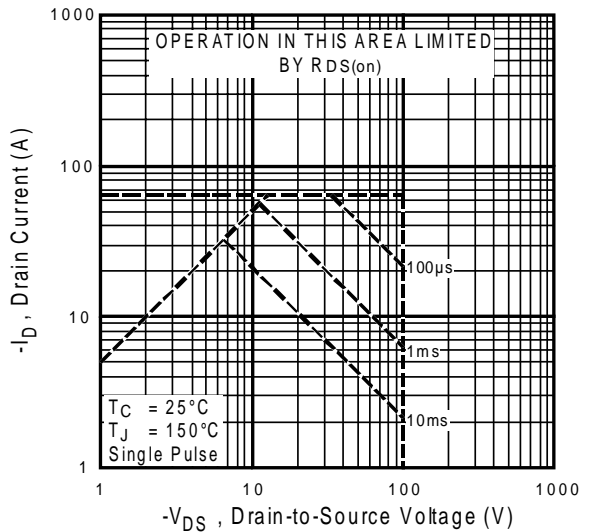


Fig 8. Maximum Safe Operating Area

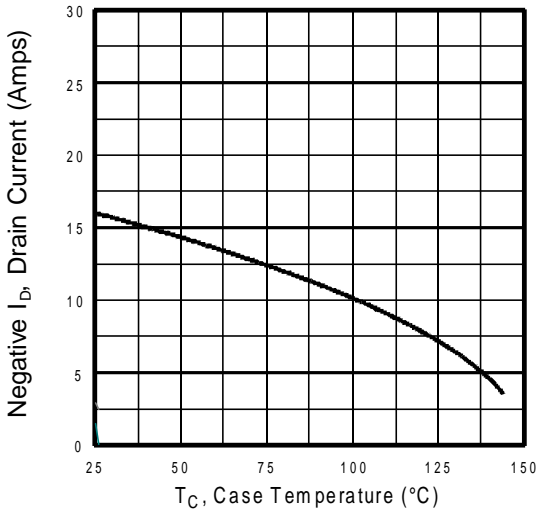


Fig 9. Maximum Drain Current Vs. Case Temperature

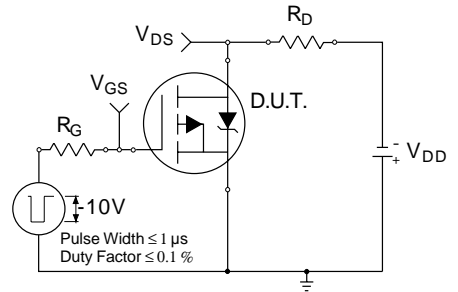


Fig 10a. Switching Time Test Circuit

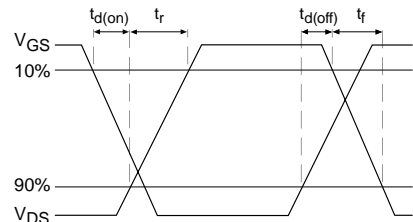


Fig 10b. Switching Time Waveforms

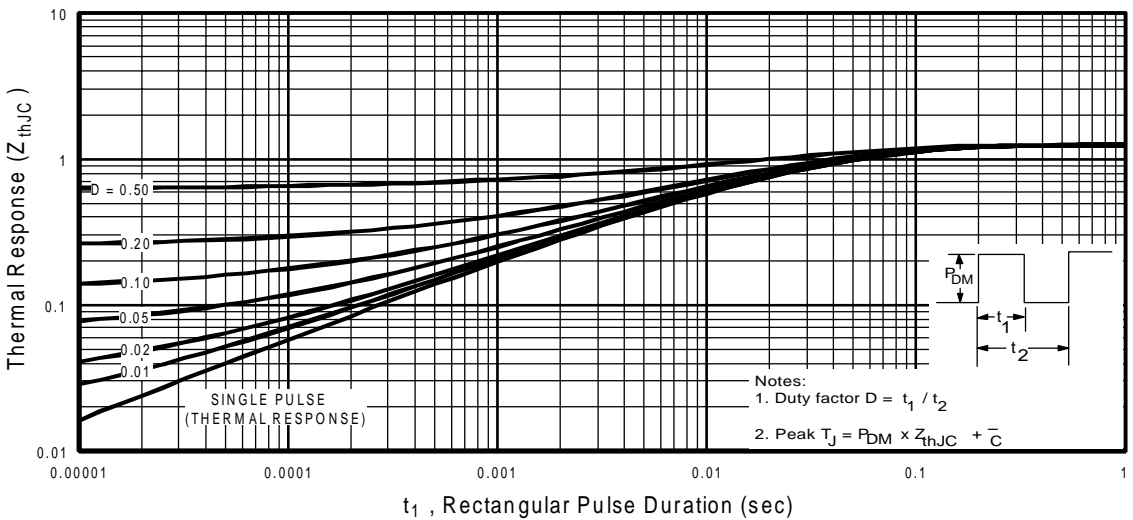


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

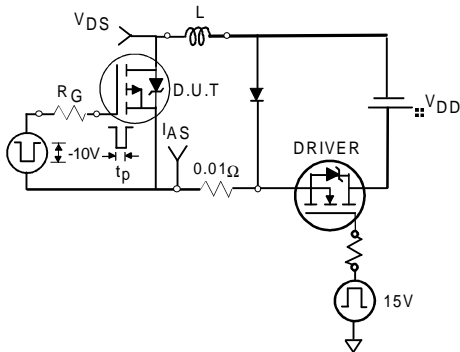


Fig 12a. Unclamped Inductive Test Circuit

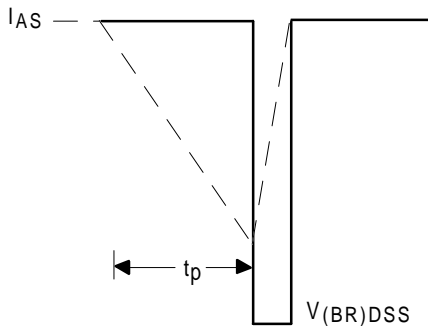


Fig 12b. Unclamped Inductive Waveforms

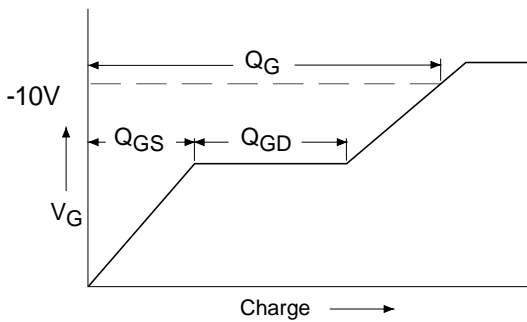


Fig 13a. Basic Gate Charge Waveform

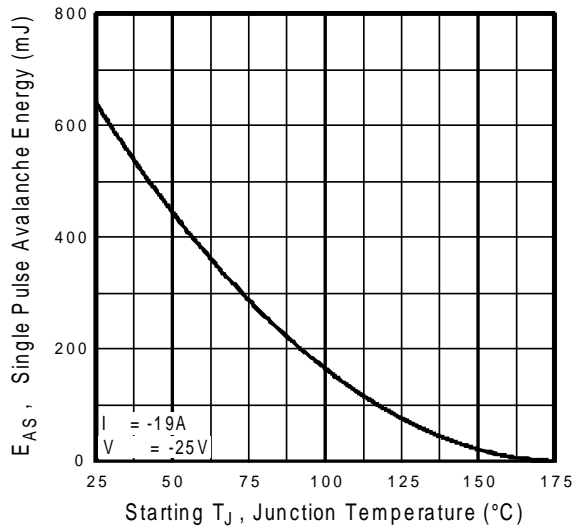


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

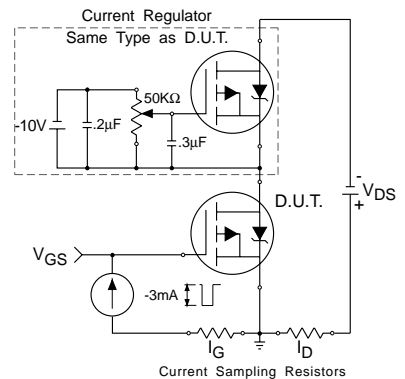
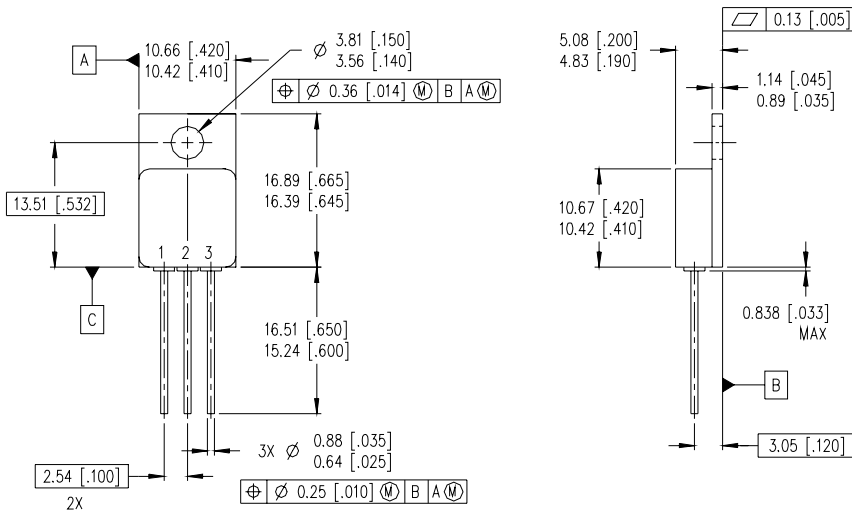


Fig 13b. Gate Charge Test Circuit

**Foot Notes:**

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ②  $V_{DD} = -50V$ , starting  $T_J = 25^\circ C$ ,  $L = 5.1mH$   
 Peak  $I_L = -15.8A$ ,  $V_{GS} = -10V$
- ③  $I_{SD} \leq -15.8A$ ,  $di/dt \leq -200A/\mu s$ ,  
 $V_{DD} \leq -100V$ ,  $T_J \leq 150^\circ C$
- ④ Pulse width  $\leq 300 \mu s$ ; Duty Cycle  $\leq 2\%$

**Case Outline and Dimensions — TO-257AA**



**NOTES:**

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-257AA.

**LEGEND**

- D - DRAIN
- S - SOURCE
- G - GATE

