



# CMOS Static RAM 1 Meg (128K x 8-Bit)

IDT71024

### Features

- ◆ 128K x 8 advanced high-speed CMOS static RAM
- ◆ Commercial (0°C to +70°C), Industrial (-40°C to +85°C)
- ◆ Equal access and cycle times  
— *Commercial and Industrial: 12/15/20ns*
- ◆ Two Chip Selects plus one Output Enable pin
- ◆ Bidirectional inputs and outputs directly TTL-compatible
- ◆ Low power consumption via chip deselect
- ◆ Available in 300 and 400 mil Plastic SOJ.

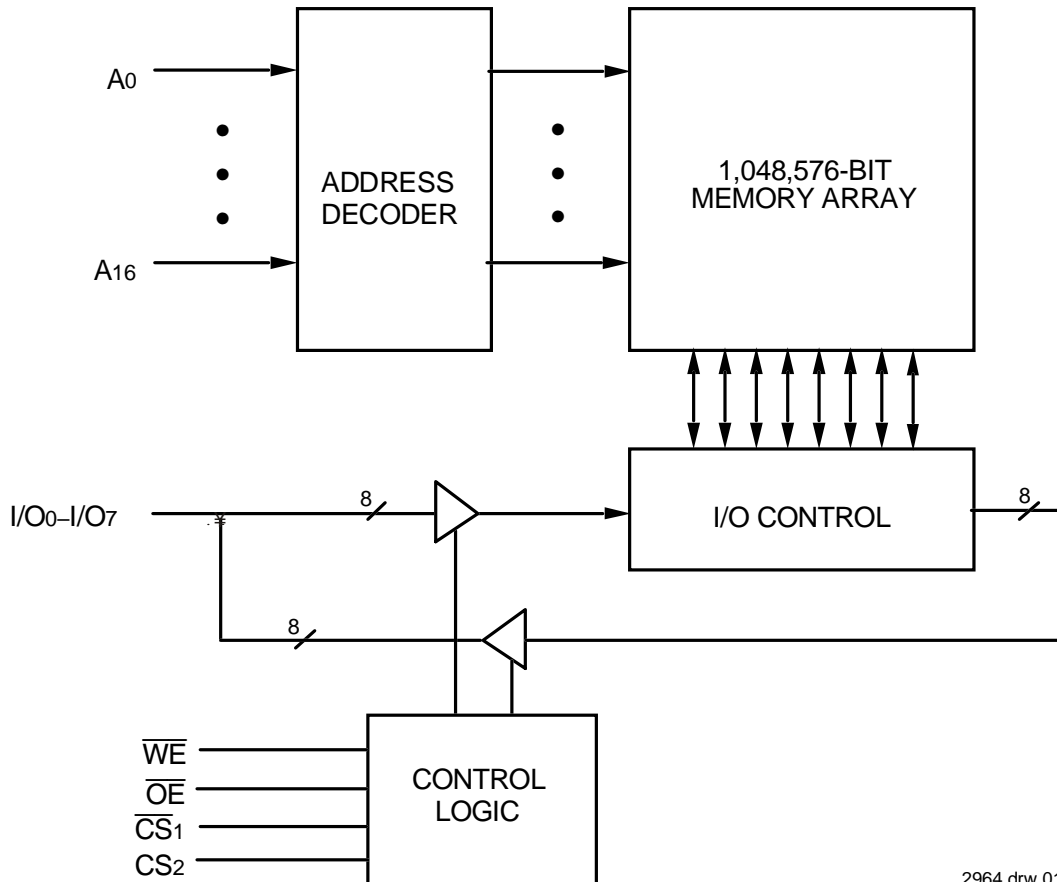
### Description

The IDT71024 is a 1,048,576-bit high-speed static RAM organized as 128K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

The IDT71024 has an output enable pin which operates as fast as 6ns, with address access times as fast as 12ns available. All bidirectional inputs and outputs of the IDT71024 are TTL-compatible, and operation is from a single 5V supply. Fully static asynchronous circuitry is used; no clocks or refreshes are required for operation.

The IDT71024 is packaged in 32-pin 300 mil Plastic SOJ and 32-pin 400 mil Plastic SOJ.

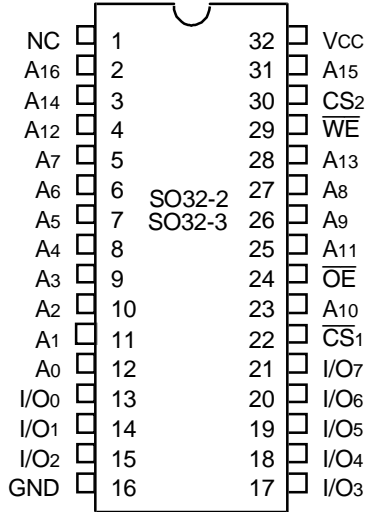
### Functional Block Diagram



2964 drw 01

FEBRUARY 2001

## Pin Configuration



SOJ  
Top View

2964 drw 02

## Absolute Maximum Ratings<sup>(1)</sup>

Symbol	Rating	Value	Unit
V <sub>TERM</sub> <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	°C
P <sub>T</sub>	Power Dissipation	1.25	W
I <sub>OUT</sub>	DC Output Current	50	mA

2964 tbl 02

### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>TERM</sub> must not exceed V<sub>CC</sub> + 0.5V.

## Truth Table<sup>(1,2)</sup>

Inputs				I/O	Function
WE	CS <sub>1</sub>	CS <sub>2</sub>	OE		
X	H	X	X	High-Z	Deselected – Standby (I <sub>SB</sub> )
X	V <sub>HC</sub> <sup>(3)</sup>	X	X	High-Z	Deselected – Standby (I <sub>SB1</sub> )
X	X	L	X	High-Z	Deselected – Standby (I <sub>SB</sub> )
X	X	V <sub>LC</sub> <sup>(3)</sup>	X	High-Z	Deselected – Standby (I <sub>SB1</sub> )
H	L	H	H	High-Z	Outputs Disabled
H	L	H	L	DATA <sub>OUT</sub>	Read Data
L	L	H	X	DATA <sub>IN</sub>	Write Data

2964 tbl 01

### NOTES:

- H = V<sub>H</sub>, L = V<sub>L</sub>, X = Don't care.
- V<sub>LC</sub> = 0.2V, V<sub>HC</sub> = V<sub>CC</sub> - 0.2V.
- Other inputs ≥ V<sub>HC</sub> or ≤ V<sub>LC</sub>.

## Capacitance

(T<sub>A</sub> = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter <sup>(1)</sup>	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 3dV	7	pF
C <sub>I/O</sub>	I/O Capacitance	V <sub>OUT</sub> = 3dV	8	pF

2964 tbl 03

### NOTE:

- This parameter is guaranteed by device characterization, but is not production tested.

## Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V <sub>IH</sub>	Input High Voltage	2.2	—	V <sub>CC</sub> +0.5	V
V <sub>IL</sub>	Input Low Voltage	-0.5 <sup>(1)</sup>	—	0.8	V

2964 tbl 04

### NOTE:

- V<sub>IL</sub> (min.) = -1.5V for pulse width less than 10ns, once per cycle.

## Recommended Operating Temperature and Supply Voltage

Grade	Temperature	GND	V <sub>CC</sub>
Commercial	0°C to +70°C	0V	5.0V ± 0.5V
Industrial	-40°C to +85°C	0V	5.0V ± 0.5V

2964 tbl 05

## DC Electrical Characteristics

( $V_{CC} = 5.0V \pm 10\%$ , Commercial and Industrial Temperature Ranges)

Symbol	Parameter	Test Condition	IDT71024		Unit
			Min.	Max.	
$ I_{LI} $	Input Leakage Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND to } V_{CC}$	—	5	$\mu\text{A}$
$ I_{LO} $	Output Leakage Current	$V_{CC} = \text{Max.}, \overline{CS}_1 = V_{IH}, V_{OUT} = \text{GND to } V_{CC}$	—	5	$\mu\text{A}$
$V_{OL}$	Output Low Voltage	$I_{OL} = 8\text{mA}, V_{CC} = \text{Min.}$	—	0.4	V
$V_{OH}$	Output High Voltage	$I_{OH} = -4\text{mA}, V_{CC} = \text{Min.}$	2.4	—	V

2964 tbl 06

## DC Electrical Characteristics<sup>(1)</sup>

( $V_{CC} = 5.0V \pm 10\%$ ,  $V_{LC} = 0.2V$ ,  $V_{HC} = V_{CC} - 0.2V$ )

Symbol	Parameters	71024S12		71024S15		71024S20		Unit
		Com'l.	Ind.	Com'l.	Ind.	Com'l.	Ind.	
$I_{CC}$	Dynamic Operating Current, $CS_2 \geq V_{IH}$ and $\overline{CS}_1 \leq V_{IL}$ , Outputs Open, $V_{CC} = \text{Max.}, f = f_{MAX}^{(2)}$	160	160	155	155	140	140	mA
$I_{SB}$	Standby Power Supply Current (TTL Level) $CS_1 \geq V_{IH}$ or $CS_2 \leq V_{IL}$ , Outputs Open, $V_{CC} = \text{Max.}, f = f_{MAX}^{(2)}$	40	40	40	40	40	40	mA
$I_{SB1}$	Full Standby Power Supply Current (CMOS Level), $\overline{CS}_1 \geq V_{HC}$ or $CS_2 \leq V_{LC}$ , Outputs Open, $V_{CC} = \text{Max.}, f = 0^{(2)}, V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$	10	10	10	10	10	10	mA

2964 tbl 07

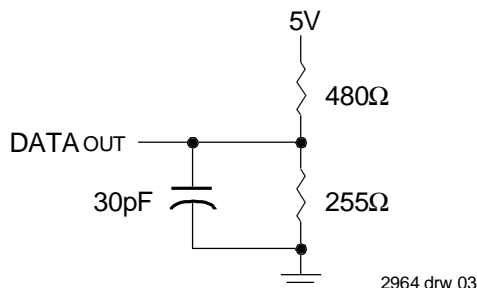
### NOTES:

- All values are maximum guaranteed values.
- $f_{MAX} = 1/t_{rc}$  (all address inputs are cycling at  $f_{MAX}$ ):  $f = 0$  means no address input lines are changing.

## AC Test Conditions

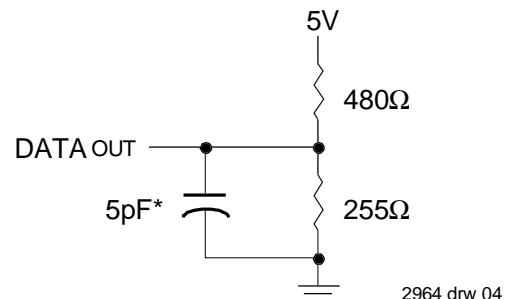
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2964 tbl 08



2964 drw 03

Figure 1. AC Test Load



2964 drw 04

\*Including jig and scope capacitance.

Figure 2. AC Test Load  
(for  $t_{CLZ}$ ,  $t_{OLZ}$ ,  $t_{CHZ}$ ,  $t_{OHZ}$ ,  $t_{OW}$ , and  $t_{WHZ}$ )

## AC Electrical Characteristics

(V<sub>CC</sub> = 5.0V ± 10%, Commercial and Industrial Temperature Ranges)

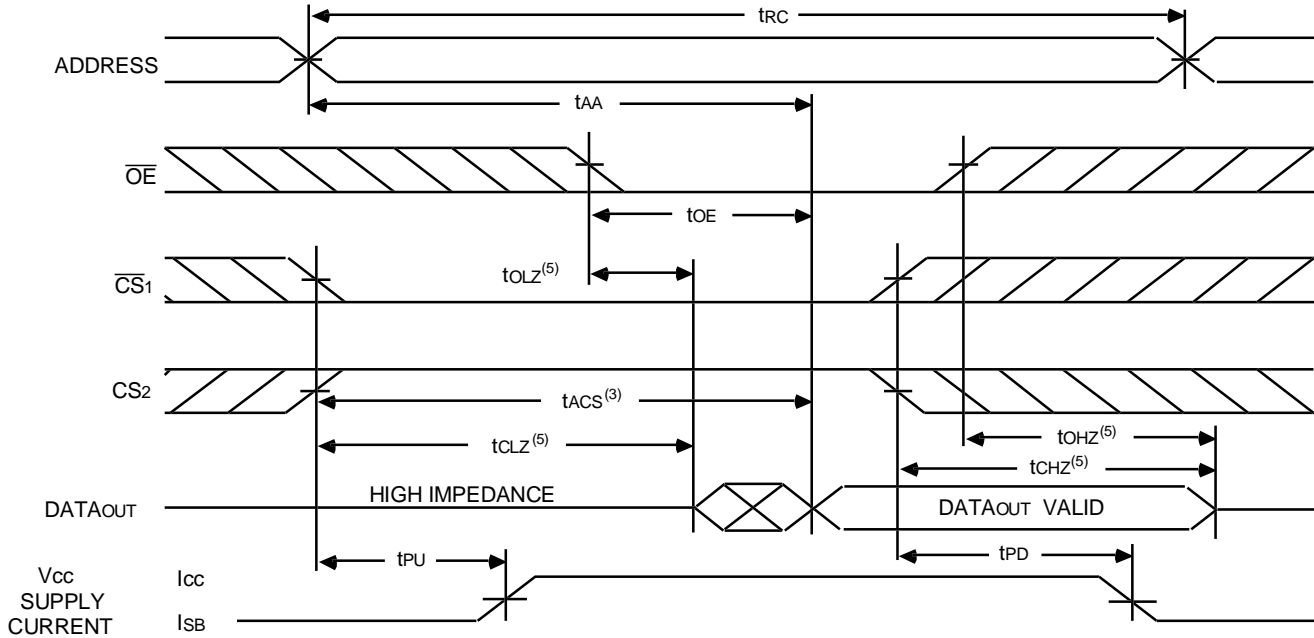
Symbol	Parameter	71024S12		71024S15		71024S20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>Read Cycle</b>								
t <sub>RC</sub>	Read Cycle Time	12	—	15	—	20	—	ns
t <sub>AA</sub>	Address Access Time	—	12	—	15	—	20	ns
t <sub>ACS</sub>	Chip Select Access Time	—	12	—	15	—	20	ns
t <sub>CLZ</sub> <sup>(1)</sup>	Chip Select to Output in Low-Z	3	—	3	—	3	—	ns
t <sub>CHZ</sub> <sup>(1)</sup>	Chip Deselect to Output in High-Z	0	6	0	7	0	8	ns
t <sub>OE</sub>	Output Enable to Output Valid	—	6	—	7	—	8	ns
t <sub>OLZ</sub> <sup>(1)</sup>	Output Enable to Output in Low-Z	0	—	0	—	0	—	ns
t <sub>OHZ</sub> <sup>(1)</sup>	Output Disable to Output in High-Z	0	5	0	5	0	7	ns
t <sub>OH</sub>	Output Hold from Address Change	4	—	4	—	4	—	ns
t <sub>PU</sub> <sup>(1)</sup>	Chip Select to Power-Up Time	0	—	0	—	0	—	ns
t <sub>PD</sub> <sup>(1)</sup>	Chip Deselect to Power-Down Time	—	12	—	15	—	20	ns
<b>Write Cycle</b>								
t <sub>WC</sub>	Write Cycle Time	12	—	15	—	20	—	ns
t <sub>AW</sub>	Address Valid to End-of-Write	10	—	12	—	15	—	ns
t <sub>CW</sub>	Chip Select to End-of-Write	10	—	12	—	15	—	ns
t <sub>AS</sub>	Address Set-Up Time	0	—	0	—	0	—	ns
t <sub>WP</sub>	Write Pulse Width	8	—	12	—	15	—	ns
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	0	—	ns
t <sub>DW</sub>	Data Valid to End-of-Write	7	—	8	—	9	—	ns
t <sub>DH</sub>	Data Hold Time	0	—	0	—	0	—	ns
t <sub>OW</sub> <sup>(1)</sup>	Output Active from End-of-Write	3	—	3	—	4	—	ns
t <sub>WHZ</sub> <sup>(1)</sup>	Write Enable to Output in High-Z	0	5	0	5	0	8	ns

**NOTE:**

1. This parameter guaranteed with the AC load (Figure 2) by device characterization, but is not production tested.

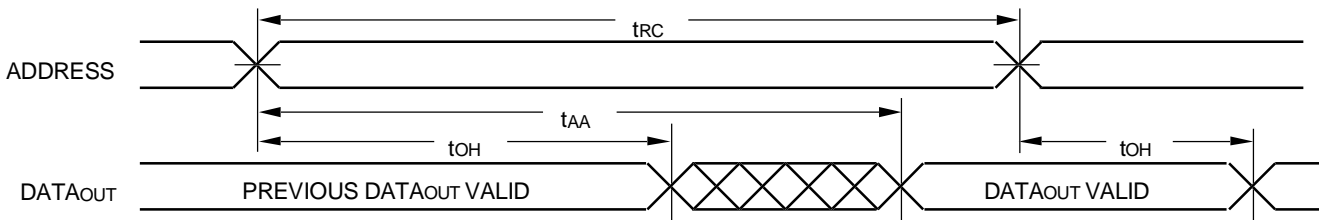
2964 tbl 09

### Timing Waveform of Read Cycle No. 1<sup>(1)</sup>



2964 drw 05

### Timing Waveform of Read Cycle No. 2<sup>(1,2,4)</sup>

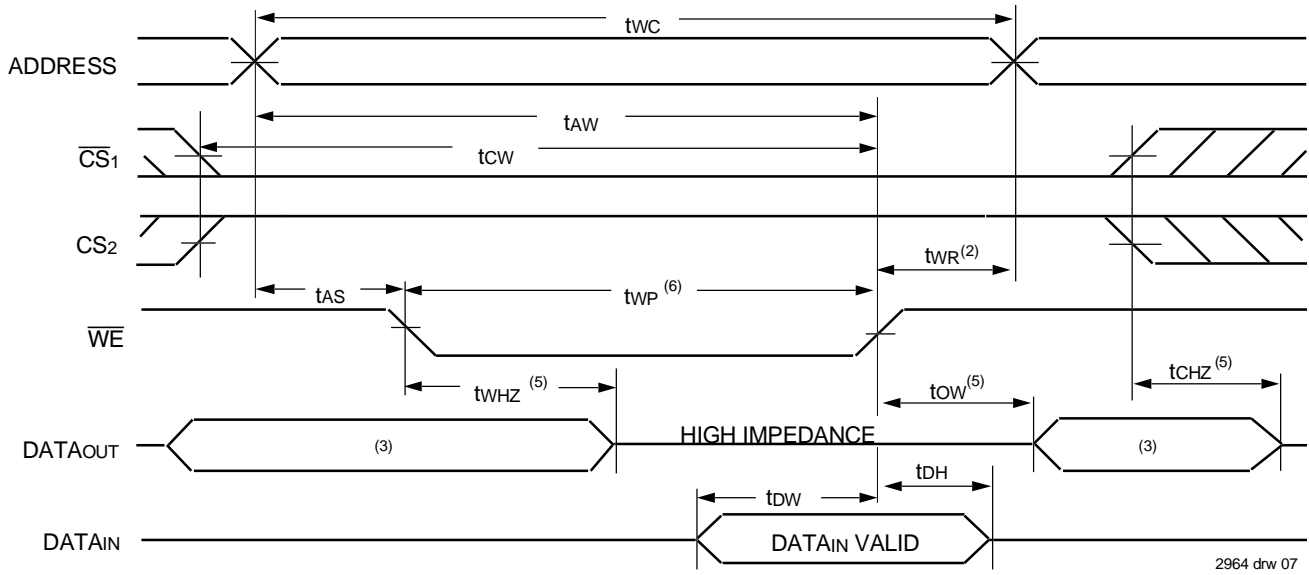


2964 drw 06

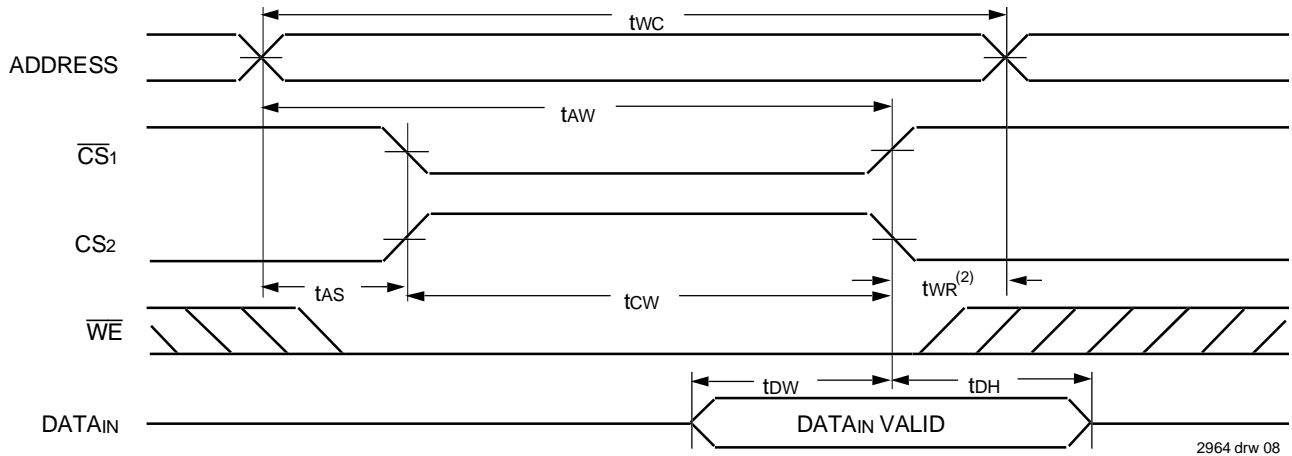
**NOTES:**

- $\overline{WE}$  is HIGH for Read Cycle.
- Device is continuously selected,  $\overline{CS1}$  is LOW,  $CS2$  is HIGH.
- Address must be valid prior to or coincident with the later of  $\overline{CS1}$  transition LOW and  $CS2$  transition HIGH; otherwise  $t_{AA}$  is the limiting parameter.
- $\overline{OE}$  is LOW.
- Transition is measured  $\pm 200\text{mV}$  from steady state.

## Timing Waveform of Write Cycle No. 1 ( $\overline{WE}$ Controlled Timing)<sup>(1,4,6)</sup>



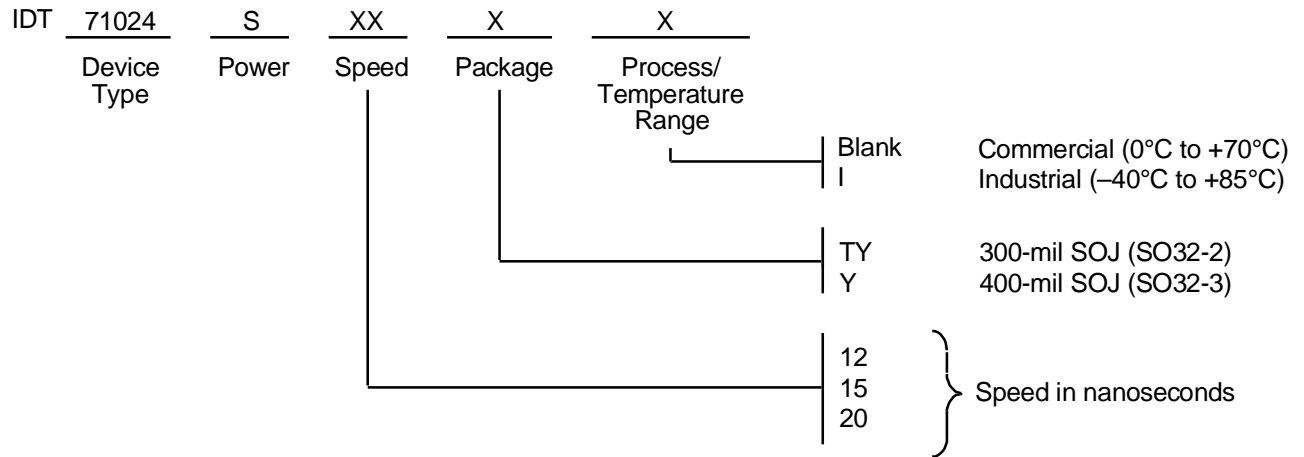
## Timing Waveform of Write Cycle No. 2 ( $\overline{CS1}$ AND $\overline{CS2}$ Controlled Timing)<sup>(1,4)</sup>



### NOTES:

1. A write occurs during the overlap of a LOW  $\overline{CS1}$ , HIGH  $CS2$ , and a LOW  $\overline{WE}$ .
2.  $t_{WR}$  is measured from the earlier of either  $\overline{CS1}$  or  $\overline{WE}$  going HIGH or  $CS2$  going LOW to the end of the write cycle.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the  $\overline{CS1}$  LOW transition or the  $CS2$  HIGH transition occurs simultaneously with or after the  $\overline{WE}$  LOW transition, the outputs remain in a high impedance state.  $\overline{CS1}$  and  $CS2$  must both be active during the  $t_{CW}$  write period.
5. Transition is measured  $\pm 200\text{mV}$  from steady state.
6.  $\overline{OE}$  is continuously HIGH. During a  $\overline{WE}$  controlled write cycle with  $\overline{OE}$  LOW,  $t_{WP}$  must be greater than or equal to  $t_{WHZ} + t_{OW}$  to allow the I/O drivers to turn off and data to be placed on the bus for the required  $t_{OW}$ . If  $\overline{OE}$  is HIGH during a  $\overline{WE}$  controlled write cycle, this requirement does not apply and the minimum write pulse is the specified  $t_{WP}$ .

## Ordering Information



2964 drw 09

## Datasheet Document History

9/30/99		Updated to new format
	Pg. 1, 3, 4, 7	Added 12ns industrial speed grade offering
	Pg. 1-4, 7	Removed military temperature offerings
		Removed 17ns and 25ns speed grades
	Pg. 3	Revised Icc and ISB1 for 15ns and 20ns industrial speed grades
	Pg. 6	Removed Note 1, reordered notes and footnotes
	Pg. 8	Added Datasheet Document History
1/6/2000	Pg. 4	Changed tWP(min) for 12ns speed grade from 10ns to 8ns.
2/18/00	Pg. 3	Revised Icc and ISB for Industrial Temperature offerings to meet commercial specifications
3/14/00	Pg. 3	Revised ISB to accomidate speed functionality
08/09/00		Not recommended for new designs
02/01/01		Removed "Not recommended for new designs"



**CORPORATE HEADQUARTERS**

2975 Stender Way  
Santa Clara, CA 95054

**for SALES:**

800-345-7015 or 408-727-6116  
fax: 408-492-8674  
www.idt.com

**for Tech Support:**

sramhelp@idt.com  
800-544-7726, x4033