Integrated Circuit Systems, Inc.

ICS9179-19

Advance Information

Zero Delay Buffer

Features

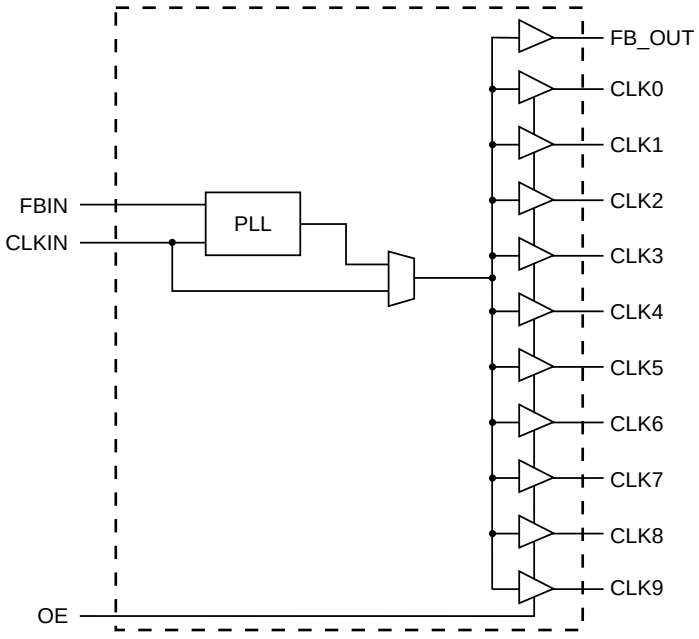
- Spread Spectrum Clock Compatible
- Distributes one clock input to ten outputs
- Operating frequency 33MHz to 150MHz
- External feedback input (FBIN) terminal is used to synchronize the outputs to the clock input
- No external RC network required
- Operates at 3.3V
- Plastic 28-pin 209mil SSOP package
- Slew rate 1.5V/ns into 30pF.

General Description

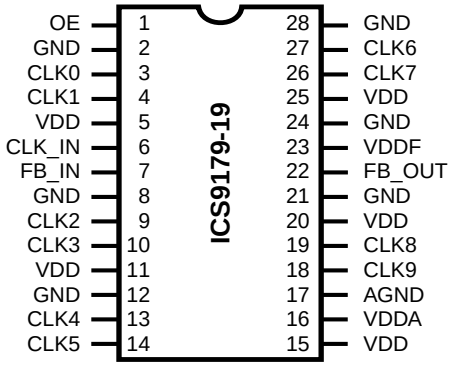
The **ICS9179-19** generates low skew clock buffers required for high speed microprocessor systems such as today's Intel Pentium III or AMD K7. Outputs can be enabled or disabled separately via OE.

The device is a buffer with low output to output skew. This is a zero delay buffer device, using an internal PLL. This buffer can be used for phase synchronization to a master clock. With the wide PLL loop BW, this buffer is compatible to Spread Spectrum input clocks from clock generator products.

Block Diagram



Pin Configuration



28 Pin SSOP

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	OE[2]	IN	Output Enable
2, 8, 12, 21, 24, 28	GND	PWR	Ground for output buffers
5, 11, 15, 20, 25	VDD	PWR	Power Supply (3.3V)
6	CLK_IN	IN	Clock input
7	FBIN	IN	Feedback input
16	AVDD	PWR	Analog power supply (3.3V)
17	AGND	PWR	Ground for analog PLL stages
22	FBOUT[1]	OUT	Feedback output
23	VDDF	PWR	Power supply for feedback circuit (3.3V)
27, 26, 19, 18, 14, 13, 10, 9, 4, 3	CLK (9:0)	OUT	Buffered clock outputs

Notes:
1. Weak pull-down on all outputs
2. Weak pull-ups on these inputs

Absolute Maximum Ratings

Supply Voltage (AVDD) . . . . . AVDD < (V_{DD} + 0.7V)
Supply Voltage (VDD) . . . . . 4.3 V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 3.3V

V_{DD} = 3.0 – 3.6V, T_A = 0 – 70° C unless otherwise stated

Recommended operating condition

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	Power Supply Voltage	3	3.3	3.6	V
VIH	High-level Input Voltage	2			V
VIL	Low-level Input Voltage			0.8	V
VI	Input Voltage	0		VCC	V
TA	Operating free-air temperature	0		70	℃

Electrical Characteristics Over Operating free-air Temperature Range

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VIK	Input clamp voltage	V_{DD}=3V,Ii=-18mA			-1.2	V
VOH	Output High Voltage	V_{DD}=MIN to MAX,Ii=-100uA	VDD-0.2			V
		V_{DD}=3V,Ii=-6mA	2.4			V
		V_{DD}=3V,Ii=-12mA	2.1			V
VOL	Output Low Voltage	V_{DD}=MIN to MAX,Ii=100uA			0.2	V
		V_{DD}=3V,Ii=6mA			0.55	V
		V_{DD}=3V,Ii=12mA			0.8	V
Ii	Input current	V_{DD}=3.6V,Vi=VDD or GND			±5	uA
AICC	Analog Supply Current	V_{DD}=3.3V @ 133MHz				mA
ICC	Quiescent Supply Current (test mode)	V_{DD}=MAX, AVDD=LOW,CLKIN=LOW Oex=HIGH,all outputs unloaded				mA
ICC	Power Supply Current	V_{DD} = 3.3 to 3.6V @ 100MHz all outputs unloaded			TBD	mA
Cin	Input Capacitance	V_{DD}=3.3V,Vi=VDD or GND		4		pF
Co	Output Capacitance	V_{DD}=3.3V,Vi=VDD or GND		8		pF

Note: For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating condidion

Timing requirements over recommended ranges of supply voltage and operating free-air temperature

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
Fclk	Input clock frequency		25	175	MHz
	Input clock frequency duty cycle		40	60	%
	Stabilization time	After power up		1	ms

Note: Time required for the PLL circuit to obtain phase lock of its feedback signal to its reference
In order for phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be
Until phase lock is obtained, the specifications for parameters given in the switching characteristics table are not

Switching characteristics over recommended ranges of supply voltage and operating free-air temperature CL=25pF,RL=500ohms[1]

				VCC=3.3V ±0.165V			VCC=3.3V ±0.3V			
Symbol	Parameter	From(INPUT)	TO(OUTPUT)	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
Tpe	Phase error	60MHz<CLKIN↑<125MHz	FBIN↑				-125		125	ps
Tpe[3]	Phase error-jitter	CLKIN↑=100MHz	FBIN↑	-50		50		0		ps
Tsk(0)[2]	Output-Output Skew	Any CLKOUT or FBOUT	Any CLK or FBOUT				-100		100	ps
	Jitter(pk-pk)	CLKIN=66MHz to 100MHz	Any CLK or FBOUT				-80		80	ps
	Jitter(cycle-cycle)	CLKIN=66MHz to 100MHz	Any CLK or FBOUT				TBD		TBD	ps
Tdty	Duty cycle	CLKIN>30MHz	Any CLK or FBOUT				45		55	%
Tr	Output rise time (0.4V to 2V)		Any CLK or FBOUT		1.3	1.9	0.5		2.1	ns/V
Tf	Output fall time (2V to 0.4V)		Any CLK or FBOUT		1.3	1.9	0.5		2.7	ns/V
Tpd	Propagation Delay for Buffer Mode AVCC=0, Vt=1.5V	CLK_IN	Any CLK or FBOUT	1			1		TBD	ns
	JittterSSC[4]	CLK_IN=33 + 166MHz	Any CLK						70	ns

Notes:
1. Guaranteed by design and characterization. Not subject to 100% test.
2. The Tsk specification is only valid for equal loading of all outputs.
3. Phase error does not include jitter. The total phase error is -230 ps to 230 ps for the 5% VCC range.
4. JitterSSC = Spread Spectrum Clock induce tracking error

PARAMETER MEASUREMENT INFORMATION

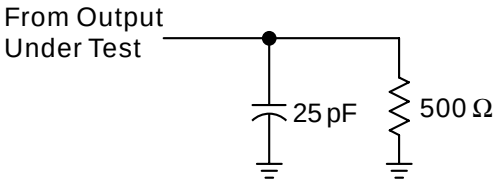


Figure 1. Load Circuit for Outputs

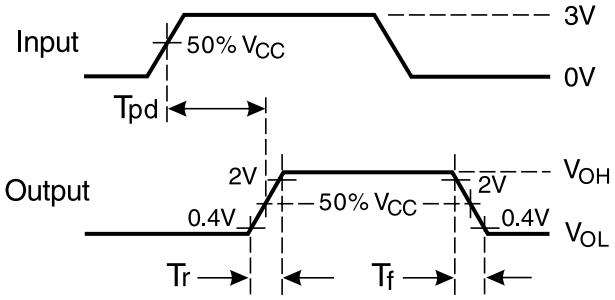


Figure 2. Voltage Waveforms Propagation Delay Times

Notes:

1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤ 133MHz, Z_O = 50Ω, T_r ≤ 1.2ns, T_f ≤ 1.2ns.
3. The outputs are measured one at a time with one transition per measurement.

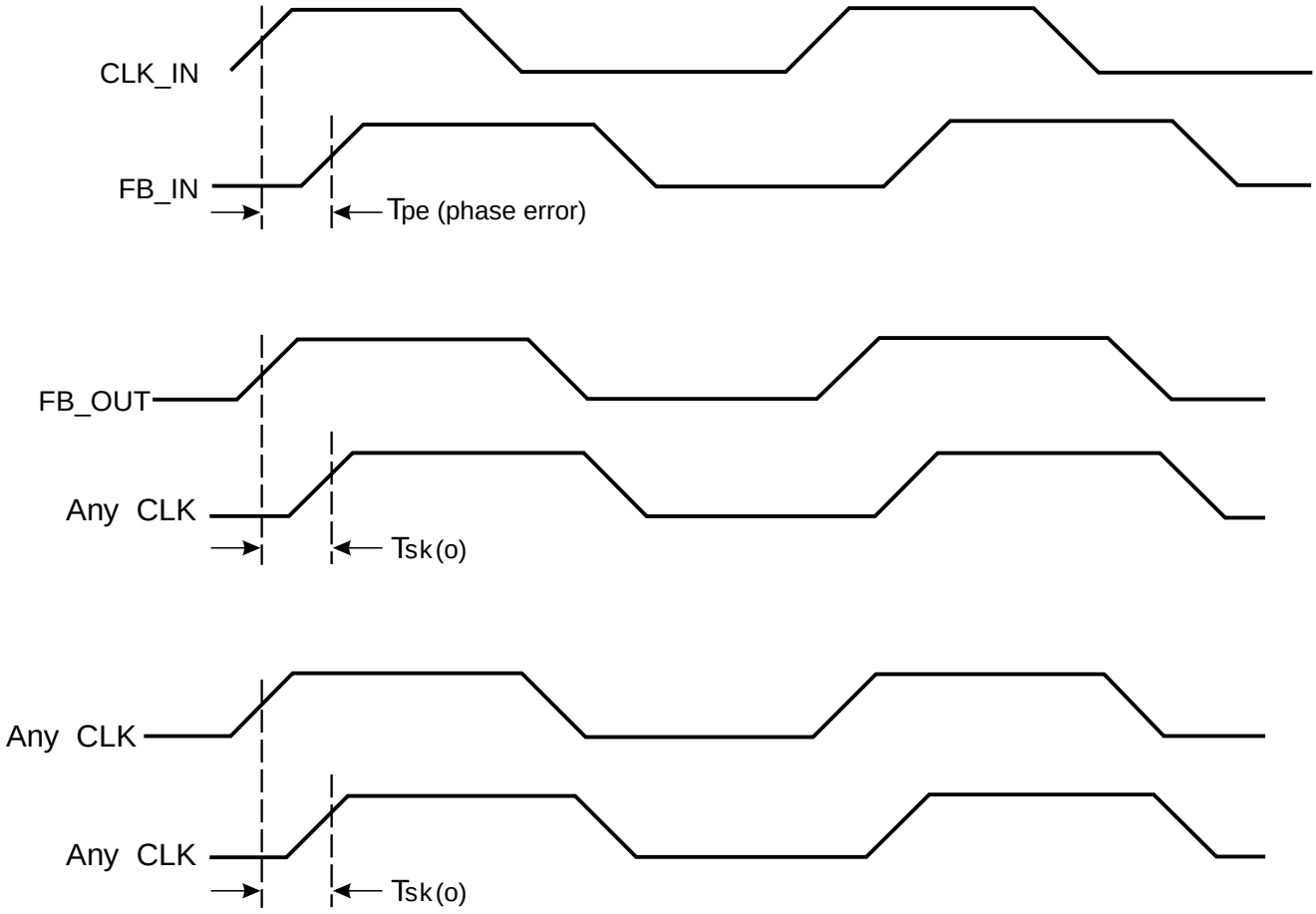
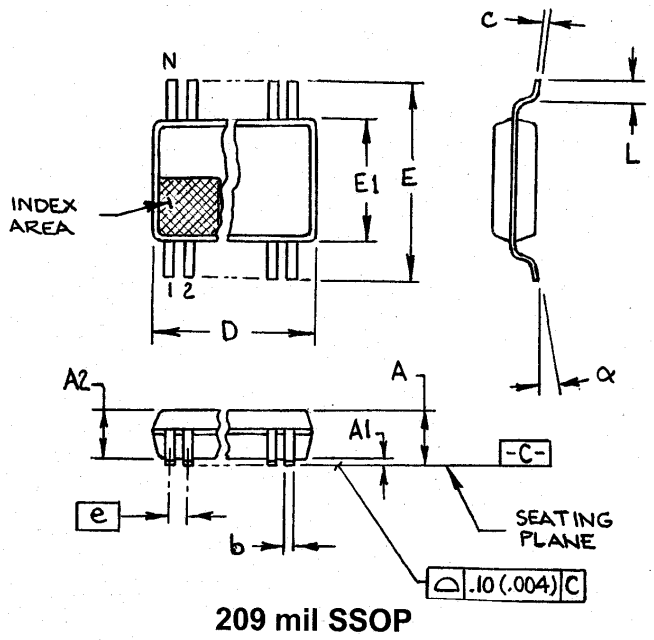


Figure 3. Phase Error and Skew Calculations



209 mil SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	-	2.00	-	.079
A1	0.05	-	.002	-
A2	1.65	1.85	.065	.073
b	0.22	0.38	.009	.015
c	0.09	0.25	.0035	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	7.40	8.20	.291	.323
E1	5.00	5.60	.197	.220
e	0.65 BASIC		0.0256 BASIC	
L	0.55	0.95	.022	.037
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
28	9.90	10.50	.390	.413

MO-150 JEDEC 6/1/00 Rev B
Doc.# 10-0033

Ordering Information

ICS9179yF-19-T

Example:

ICS XXXX y F - PPP - T

- **Designation for tape and reel packaging**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  F=SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device