



## Zero Delay Buffer for PC133 SDRAMs

### General Description

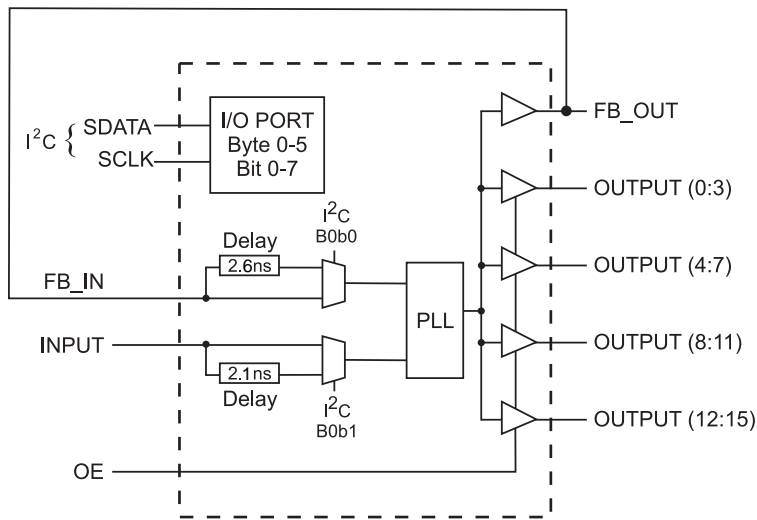
The **ICS9179-06** generates low skew SDRAM clocks required by high-speed RISC or CISC based microprocessor systems. The **ICS9179-06** is a zero delay buffer with low output-to-output skew. The buffer is compatible with Spread Spectrum clocks such as those provided by the ICS 9248-55.

Individual outputs can be disabled via the I2C interface for reduced power consumption and EMI. The nominal delay for the **ICS9179-06** can also be programmed to either 0.0, -2.6, +2.1 or -0.7 ns via the I2C interface. An output enable pin eases testability.

### Features

- 16-out zero delay buffer
- Supports up to 4 PC133 SDRAM DIMMs
- Spread Spectrum compatible
- I<sup>2</sup>C Interface
- Four nominal input-to-output delays from +2.1 to -2.6 ns selectable via I<sup>2</sup>C
- 250 ps output-to-output skew
- 33 MHz to 133 MHz operating frequency
- Multiple VDD, VSS pins for noise reduction
- 1.5V/ns minimum slew rate into 30 pF load
- VDD = 3.3V +/-5%, Commercial temperature range
- All outputs except FB\_OUT tri-state with OE low.
- 48-pin SSOP package

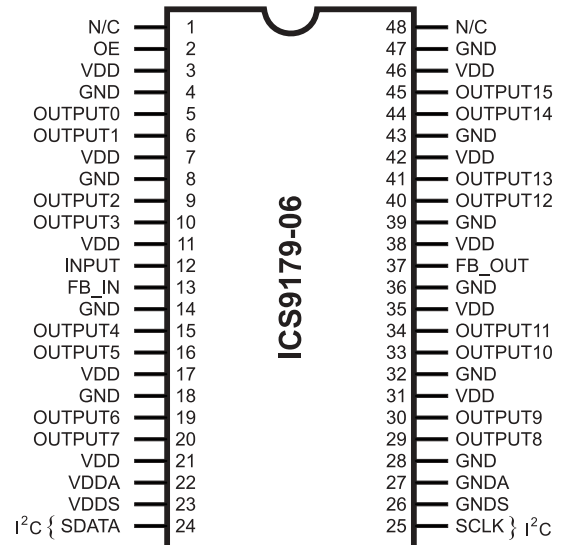
### Block Diagram



### Functionality

OE#	OUTPUT (0:15)	FB_OUT
0	Hi-Z	1 X INPUT
1	1 X INPUT	1 X INPUT

### Pin Configuration



### 48-Pin SSOP



## Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
2	OE	IN	Tri-states all outputs except FB_OUT when held LOW. Has internal pull-up. <sup>2</sup>
5, 6, 9, 10	OUTPUT (0:3)	OUT	SDRAM Byte 0 clock outputs <sup>1</sup>
15, 16, 19, 20	OUTPUT (4:7)	OUT	SDRAM Byte 1 clock outputs <sup>1</sup>
29, 30, 33, 34	OUTPUT (8:11)	OUT	SDRAM Byte 2 clock outputs <sup>1</sup>
40, 41, 44, 45	OUTPUT (12:15)	OUT	SDRAM Byte 3 clock outputs <sup>1</sup>
12	INPUT	IN	Input for reference clock.
13	FB_IN	IN	Feedback input.
24	SDATA	I/O	Data pin for I <sup>2</sup> C circuitry <sup>3</sup>
25	SCLK	I/O	Clock pin for I <sup>2</sup> C circuitry <sup>3</sup>
37	FB_OUT	OUT	Feedback output to input FB_IN.
3, 7, 11, 17, 21, 31, 35, 38, 42, 46	VDD	PWR	3.3V Power supply for output buffers
4, 8, 14, 18, 28, 32, 36, 39, 43, 47	GND	PWR	Ground for output buffers
22	VDDA	PWR	3.3V Power supply for Analog PLL stages
23	VDDS	PWR	3.3V Power supply for I <sup>2</sup> C circuitry
26	GNDS	PWR	Ground for I <sup>2</sup> C circuitry
27	GNDA	PWR	Ground for Analog PLL stages
1, 48	N/C	-	Pins are not internally connected

### Notes:

- At power up all sixteen outputs are enabled and active.
- OE has a 100K Ohm internal pull-up resistor to keep all outputs active.
- The SDATA and SCLK inputs both also have internal pull-up resistors with values above 100K Ohms as well for complete platform flexibility.
- I<sup>2</sup>C Byte0, bits 0 & 1 used to select delay. Default\* values at power up are 0

## Power Groups

VDD = Power supply for OUTPUT buffers

VDDS = Power supply for I<sup>2</sup>C circuitry

VDDA = Power supply for Analog PLL circuitry

## Ground Groups

GND = Ground supply for OUTPUT buffer

GNDS = Ground supply for I<sup>2</sup>C circuitry

GNDA = Ground supply for Analog PLL circuitry

## Delay Selection Table

INPUT Control Byte0 bit1	FB_IN Control Byte0 bit0	Nominal Delay, INPUT to FB_IN pins.
0*	0*	0ns
0	1	-2.7ns
1	0	+2.0ns
1	1	-0.7ns



### General I<sup>2</sup>C serial interface information

The information in this section assumes familiarity with I<sup>2</sup>C programming. For more information, contact ICS for an I<sup>2</sup>C programming application note.

#### How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2<sub>(H)</sub>
- ICS clock will *acknowledge*
- Controller (host) sends a dummy command code
- ICS clock will *acknowledge*
- Controller (host) sends a dummy byte count
- ICS clock will *acknowledge*
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will *acknowledge* each byte *one at a time*.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	ICS (Slave/Receiver)
Start Bit	
Address D2 <sub>(H)</sub>	
	<b>ACK</b>
Dummy Command Code	
	<b>ACK</b>
Dummy Byte Count	
	<b>ACK</b>
Byte 0	
	<b>ACK</b>
Byte 1	
	<b>ACK</b>
Byte 2	
	<b>ACK</b>
Byte 3	
	<b>ACK</b>
Byte 4	
	<b>ACK</b>
Byte 5	
	<b>ACK</b>
Stop Bit	

#### How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3<sub>(H)</sub>
- ICS clock will *acknowledge*
- ICS clock will send the *byte count*
- Controller (host) acknowledges
- ICS clock sends first byte (*Byte 0*) through *byte 5*
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	ICS (Slave/Receiver)
Start Bit	
Address D3 <sub>(H)</sub>	
	<b>ACK</b>
	<b>Byte Count</b>
ACK	
	<b>Byte 0</b>
ACK	
	<b>Byte 1</b>
ACK	
	<b>Byte 2</b>
ACK	
	<b>Byte 3</b>
ACK	
	<b>Byte 4</b>
ACK	
	<b>Byte 5</b>
ACK	
Stop Bit	

#### Notes:

1. The ICS clock generator is a slave/receiver, I<sup>2</sup>C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol.**
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I<sup>2</sup>C interface, the protocol is set to use only **"Block-Writes"** from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.



## Serial Configuration Command Bitmaps

### Byte 0: OUTPUT Clock Register (default = 0)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	0	Reserved
Bit 6	-	0	Reserved
Bit 5	-	0	Reserved
Bit 4	-	0	Reserved
Bit 3	-	0	Reserved
Bit 2	-	0	Reserved
Bit 1 <sup>2</sup>	12	0	(See Delay Selection Table)
Bit 0 <sup>2</sup>	13	0	(See Delay Selection Table)

**Notes:** 2 = Default = 0; 1 = Delay element enabled,  
0 = No delay path.

### Byte 1: OUTPUT Clock Register

BIT	PIN#	PWD	DESCRIPTION
Bit7	20	1	OUTPUT 7 (Act/Inact)
Bit6	19	1	OUTPUT 6 (Act/Inact)
Bit5	16	1	OUTPUT 5 (Act/Inact)
Bit4	15	1	OUTPUT 4 (Act/Inact)
Bit3	10	1	OUTPUT 3 (Act/Inact)
Bit2	9	1	OUTPUT 2 (Act/Inact)
Bit1	6	1	OUTPUT 1 (Act/Inact)
Bit0	5	1	OUTPUT 0 (Act/Inact)

**Notes:** 1 = Enabled; 0 = Disabled, outputs held low

**Note:** PWD = Power-Up Default

### Byte 2: OUTPUT Clock Register (Default = 1)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	45	1	OUTPUT 15 (Act/Inact)
Bit 6	44	1	OUTPUT 14 (Act/Inact)
Bit 5	41	1	OUTPUT 13 (Act/Inact)
Bit 4	40	1	OUTPUT 12 (Act/Inact)
Bit 3	34	1	OUTPUT 11 (Act/Inact)
Bit 2	33	1	OUTPUT 10 (Act/Inact)
Bit 1	30	1	OUTPUT 9 (Active/Inactive)
Bit 0	29	1	OUTPUT 8 (Active/Inactive)

**Notes:** 1 = Enabled; 0 = Disabled, outputs held low

**Note:** PWD = Power-Up Default

### Byte (3:5): Reserved

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	-	1	Reserved



### Absolute Maximum Ratings

- Supply Voltage ..... 7.0 V
- Logic Inputs ..... GND –0.5 V to V<sub>DD</sub> +0.5 V
- Ambient Operating Temperature ..... 0°C to +70°C
- Storage Temperature ..... –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

### Electrical Characteristics - Input & Supply

T<sub>A</sub> = 0 - 70°C; Supply Voltage V<sub>DD</sub> = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V <sub>IH</sub>		2		V <sub>DD</sub> + 0.3	V
Input Low Voltage	V <sub>IL</sub>		V <sub>SS</sub> - 0.3		0.8	V
Input High Current	I <sub>IH</sub>	V <sub>IN</sub> = V <sub>DD</sub>			5	uA
Input Low Current	I <sub>IL1</sub>	V <sub>IN</sub> = 0 V; Inputs with no pull-up resistors	-5			uA
Input Low Current	I <sub>IL2</sub>	V <sub>IN</sub> = 0 V; Inputs with pull-up resistors	-60	-33		uA
Operating Current	I <sub>DD</sub>	C <sub>L</sub> = 0 pF; F <sub>IN</sub> @ 66MHz		115	150	mA
		C <sub>L</sub> = 0 pF; F <sub>IN</sub> @ 100MHz		170	190	mA
		C <sub>L</sub> = 0 pF; F <sub>IN</sub> @ 133.33MHz		220	270	mA
Standby Current	I <sub>DDSB</sub>	C <sub>L</sub> = 0 pF; 33.33MHz ≤ F <sub>IN</sub> ≤ 133.33MHz			30	mA
Input frequency	F <sub>IN</sub>	Outputs Disabled	33.33		133.33	MHz
Input Duty Cycle	D <sub>I</sub>	33.33MHz ≤ F <sub>IN</sub> ≤ 133.33MHz	40		60	%
Input Capacitance	C <sub>IN</sub>	Logic Inputs			5	pF

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.



### Electrical Characteristics - SDRAM

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = V_{DDL} = 3.3 \text{ V} \pm 5\%$ ;  $C_L = 20 - 30 \text{ pF}$  (unless otherwise)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	$F_O$		33		133	MHz
Output High Voltage	$V_{OH}$	$I_{OH} = -30 \text{ mA}$	2.4			V
Output Low Voltage	$V_{OL}$	$I_{OL} = 23 \text{ mA}$			0.4	V
Output High Current	$I_{OH}$	$V_{OH} = 2.0 \text{ V}$			-54	mA
Output Low Current	$I_{OL}$	$V_{OL} = 0.8 \text{ V}$	40			mA
Rise Time	$T_r$	$V_{OL} = 0.4 \text{ V}, V_{OH} = 2.4 \text{ V}$			1.33	ns
Fall Time	$T_f$	$V_{OH} = 2.4 \text{ V}, V_{OL} = 0.4 \text{ V}$			1.33	ns
Duty Cycle	$D_t$	$V_T = 1.5 \text{ V}$	45		55	%
Output to Output Skew Window	$T_{sk}$	$V_T = 1.5 \text{ V}$			250	ps
IN to FB_IN Skew <sup>1, 2</sup>	$T_{skd1}$	$V_T = 1.5 \text{ V}$ , default Zero delay, I <sup>2</sup> C B0 bits 0, 1 = 00	-250	0	250	ps
	$T_{skd2}$	$V_T = 1.5 \text{ V}$ bits 0, 1 = 10	-2.2	-2.6	-3.2	ns
	$T_{skd3}$	$V_T = 1.5 \text{ V}$ bits 0, 1 = 01	+1.5	+2.1	+2.5	ns
	$T_{skd4}$	$V_T = 1.5 \text{ V}$ bits 0, 1 = 11	-0.2	-0.7	-1.2	ns

#### Notes:

1. Guaranteed by design and characterization, not 100% tested in production

2. Delay elements FBIN and clock INPUT path are selected by I<sup>2</sup>C BYTE2; bit 0 = clock input control, bit 1 = Clock INPUT Control. (Default is 0). A 0 = No delay in path, 1 = Delay element selected.

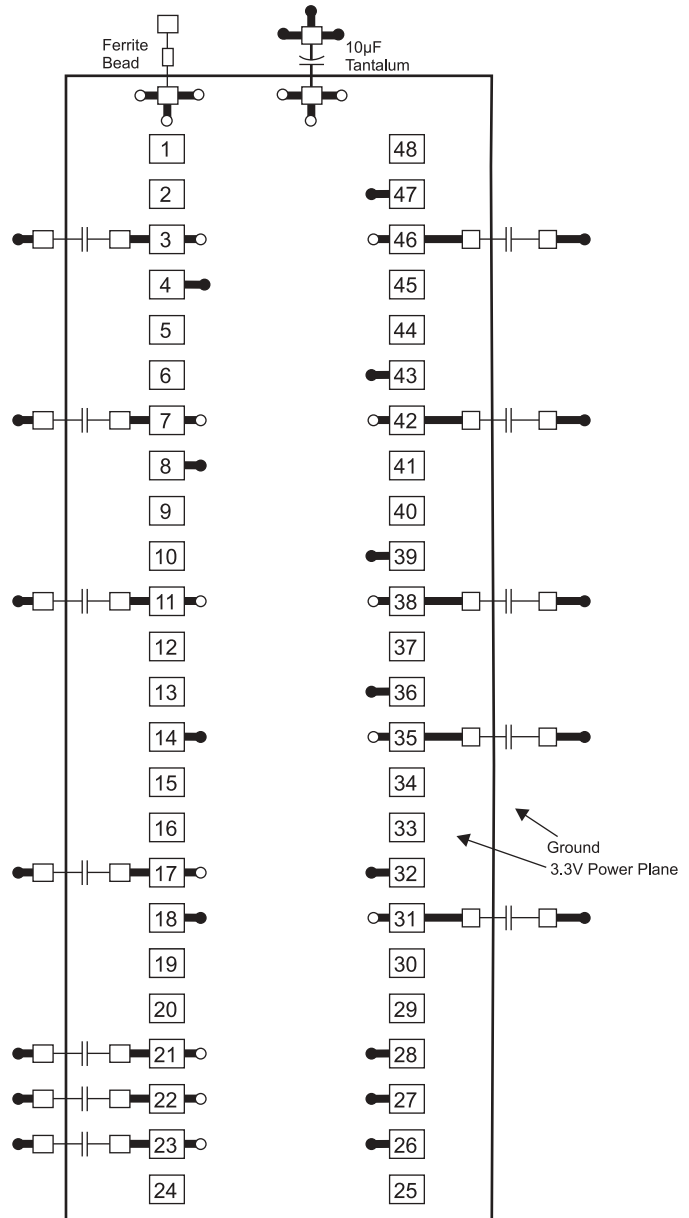


**General Layout Precautions:**

- 1) Use a ground plane on the top layer of the PCB in all areas not used by traces.
- 2) Make all power traces and vias as wide as possible to lower inductance.

**Notes:**

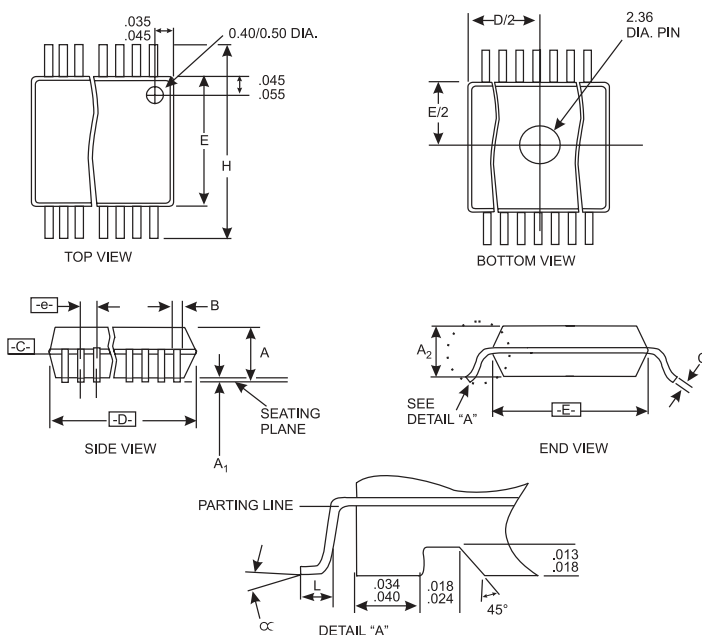
- 1 All clock outputs should have series terminating resistor. Not shown in all places to improve readability of diagram
- 2 Optional EMI capacitor should be used on all CPU, SDRAM, and PCI outputs.



**Capacitor Values:**

All unmarked capacitors are 0.01µF ceramic

- = Ground Plane Connection
- = Power Plane Connection
- = Solder Pads



## SSOP Package

SYMBOL	COMMON DIMENSIONS			VARIATIONS	D			N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	.095	.101	.110	AC	.620	.625	.630	48
A1	.008	.012	.016					
A2	.088	.090	.092					
B	.008	.010	.0135					
C	.005	-	.010					
D	See Variations							
E	.292	.296	.299					
e	0.025 BSC							
H	.400	.406	.410					
h	.010	.013	.016					
L	.024	.032	.040					
N	See Variations							
μ	0°	5°	8°					
X	.085	.093	.100					

## Ordering Information

### ICS9179F-06

Example:

**ICS XXXX F - PPP**

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Package Type  
F=SSOP

Device Type (consists of 3 or 4 digit numbers)

Prefix  
ICS, AV = Standard Device