CX74016

RF/IF Transceiver For GSM Applications

Product Description

The CX74016 RF/IF Transceiver is a highly integrated, monolithic device optimized for use in Global System for Mobile Communications (GSM) and other Time Division Multiple Access (TDMA) single-band or multi-band applications.

The receive path of the device consists of three Intermediate Frequency (IF) amplifiers with selectable gain, an I/Q demodulator, baseband filters, DC offset compensation circuitry, and selectable gain baseband amplifiers.

The transmit path of the device consists of an In-Phase and Quadrature-Phase (I/Q) modulator and a frequency translation loop designed to perform frequency up-conversion with high output spectral purity. The translation loop consists of a phase/frequency detector, a charge-pump, a mixer, and buffers for the required isolation between the RF section, Local Oscillator (LO), and IF inputs.

In addition, the CX74016 features an on-chip dual-loop UHF/VHF frequency synthesizer circuit. It includes two sets of reference dividers, phase/frequency detectors, charge pumps, prescalers, main dividers, lock detector, and control circuits.

The device package and pin configuration are shown in Figure 1. A block diagram of the CX74016 is shown in Figure 2. The signal pin assignments and functional pin descriptions are found in Table 1.
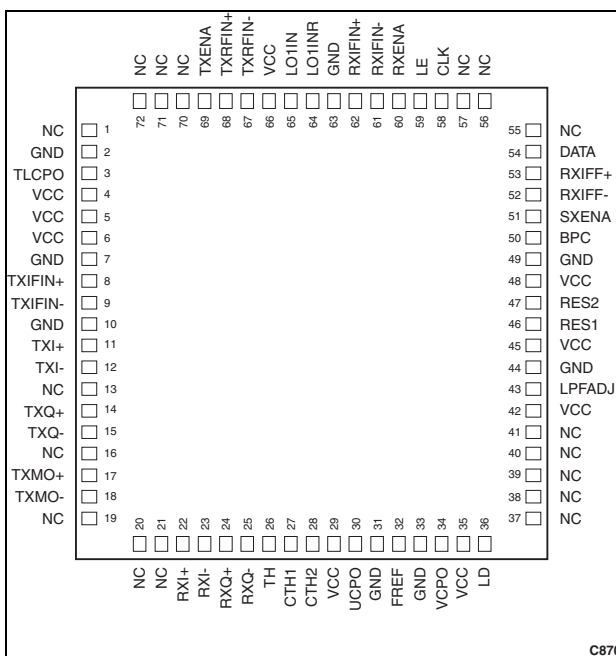
Features

- Quadrature demodulator for downconversion
- 80 dB IF gain range and 30 dB baseband gain range
- Integrated receive baseband filters with tunable bandwidth
- Integrated transmit path with high phase accuracy
- Reduced filtering requirements for the transmit path
- Broad RF and IF range for multi-band operation
- Integrated selectable local oscillator dividers/phase shifters and high/low-side injection for frequency plan flexibility
- On-chip second local oscillator
- Includes fully programmable dual-loop synthesizer
- Selectable charge pump currents for both synthesizers
- Digital lock detector
- Separate enable lines for transmit, receive, and synthesizer modes for power management
- 72-pin Land Grid Array (LGA) 10 mm x 10 mm package

Applications

- GSM900/DCS1800/PCS1900 digital cellular telephony
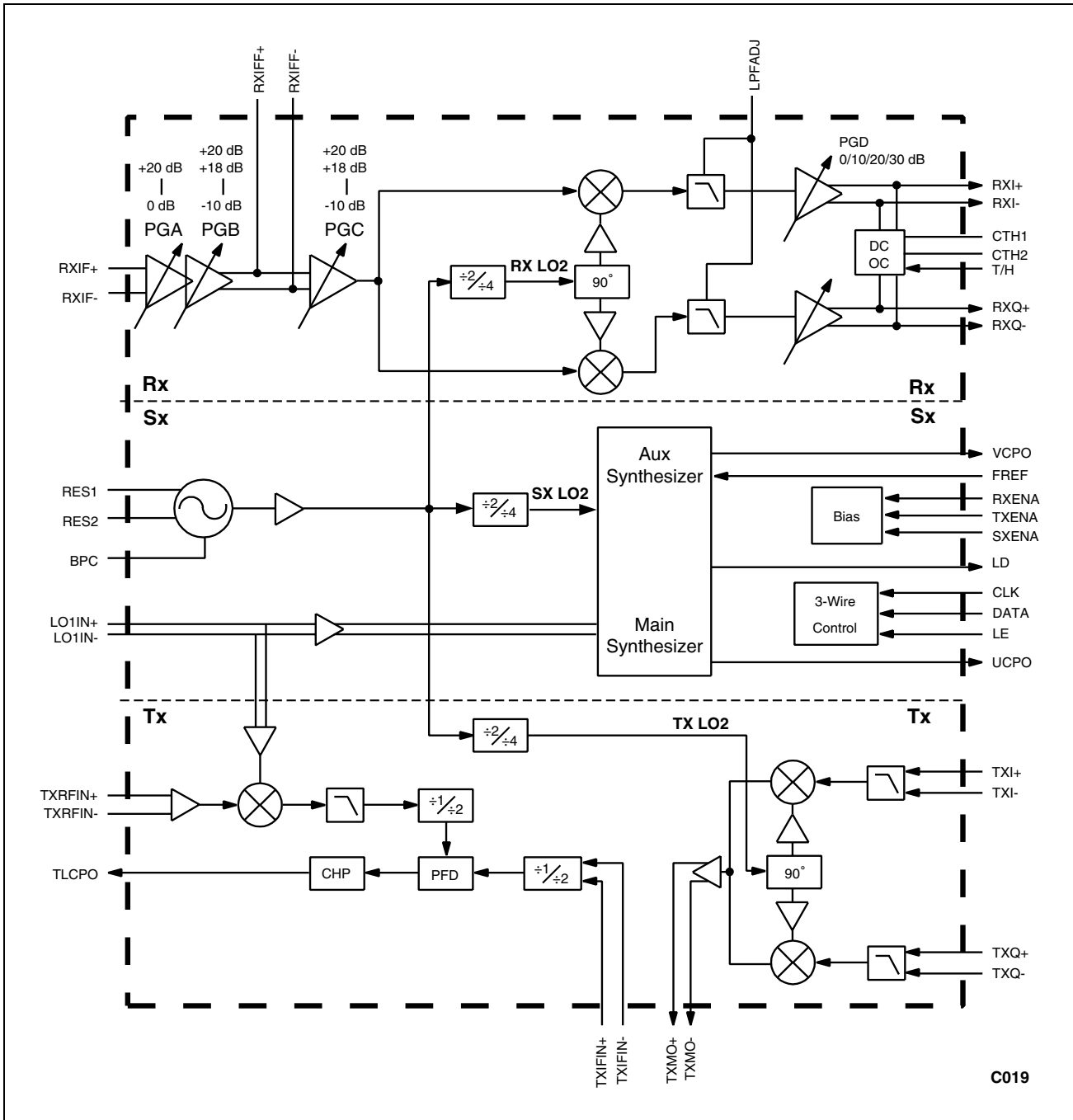- Multi-mode, multi-band terminals

Figure 1. CX74016 Pin Configuration – 72-Pin LGA

Figure 2. CX74016 Block Diagram

Table 1. CX74016 Signal Description

Pin #	Name	Description	Pin #	Name	Description
1	NC	No connect	37	NC	No connect
2	GND	Ground for translational loop	38	NC	No connect
3	TLCPO	Translation loop charge pump output	39	NC	No connect
4	VCC	Supply for translation loop	40	NC	No connect
5	VCC	Supply	41	NC	No connect
6	VCC	Supply	42	VCC	Supply
7	GND	Ground for Tx IF and baseband	43	LPFADJ	Adjustment pin for baseband low pass filter corner frequency
8	TXIFIN+	Tx IF positive input	44	GND	Ground
9	TXIFIN–	Tx IF negative input	45	VCC	Supply for oscillator
10	GND	Ground	46	RES1	Resonator pin
11	TXI+	Tx modulator positive input	47	RES2	Resonator pin
12	TXI–	Tx modulator negative input	48	VCC	Supply for oscillator
13	NC	No connect	49	GND	Ground for oscillator
14	TXQ+	Tx modulator positive input	50	BPC	Bypass capacitor
15	TXQ–	Tx modulator negative input	51	SXENA	Synthesizer enable
16	NC	No connect	52	RXIFF–	Rx IF filter pin
17	TXMO+	Tx modulator positive output	53	RXIFF+	Rx IF filter pin
18	TXMO–	Tx modulator negative output	54	DATA	Serial data input
19	NC	No connect	55	NC	No connect
20	NC	No connect	56	NC	No connect
21	NC	No connect	57	NC	No connect
22	RXI+	Rx baseband positive output	58	CLK	Serial clock input
23	RXI–	Rx baseband negative output	59	LE	Latch enable for serial data
24	RXQ+	Rx baseband positive output	60	RXENA	Receiver enable
25	RXQ–	Rx baseband negative output	61	RXIFIN–	Rx IF input
26	TH	Track and hold signal	62	RXIFIN+	Rx IF input
27	CTH1	Capacitor for track and hold	63	GND	Ground for translation loop mixer and Rx IF section
28	CTH2	Capacitor for track and hold	64	LO1INR	1st local oscillator input reference
29	VCC	Supply for UHF loop	65	LO1IN	1st local oscillator input
30	UCPO	UHF charge pump output (main synthesizer)	66	VCC	Supply for translation loop mixer and Rx IF section
31	GND	Ground	67	TXRFIN–	Transmit RF negative input reference
32	FREF	Synthesizer reference frequency input	68	TXRFIN+	Transmit RF positive input
33	GND	Ground	69	TXENA	Transmit enable
34	VCPO	VHF charge pump output	70	NC	No connect
35	VCC	Supply for VHF loop	71	NC	No connect
36	LD	Lock detect output	72	NC	No connect

Technical Description

The CX74016 RF/IF transceiver is comprised of a receive path, a transmit path, and a synthesizer section as shown in Figure 2. The receive path consists of a selectable gain IF chain, a quadrature demodulator, and baseband amplifier circuitry with I and Q outputs. The transmit path is essentially an I/Q modulator with a translation loop for frequency up-conversion. An on-chip oscillator and a dual-loop UHF/VHF frequency synthesizer circuit make up the synthesizer section. Each section of the CX74016 is separately enabled via the enable signals TXENA, RXENA, and SXENA.

The block diagram in Figure 3 shows a complete RF/IF dual-band transceiver chipset using the CX74016.

Receive Path _____

Selectable Gain IF Chain and Quadrature Mixer. The receive path of the CX74016 is composed of an IF section and a baseband section. The IF section consists of three programmable gain amplifiers: PGA, PGB, and PGC.

PGA has two gain settings, either 0 dB or 20 dB. Both PGB and PGC have a gain range of –10 dB to 20 dB, programmable in 2 dB steps. The output of PGC is fed to a quadrature mixer. The LO inputs to the quadrature mixer are taken from the outputs of a quadrature divider (divide by 2 or 4).

Baseband Integrated Filters, Baseband Amplifiers, and DC Offset Compensation. Immediately following the quadrature mixer (demodulator) is the baseband section (DC offset compensation circuitry, two integrated baseband filters, and two programmable gain amplifiers). Each programmable gain amplifier in the baseband section, both labelled PGD, has four different gain settings: 0 dB, 10 dB, 20 dB, or 30 dB.

The corner frequency of the integrated baseband filters is adjustable by using an appropriate value resistor at pin 43, LPFADJ. At the nominal cutoff frequency of 105 kHz, the resistor value is 75.1 kΩ.

Due to possible high gain of the baseband amplifiers (PGD), any DC offsets at the outputs of the quadrature mixer are amplified and, if uncorrected, the I and Q outputs can suffer from significant unwanted DC offset voltages. To cancel out these effects, the CX74016 must be calibrated.

During compensation, the correction voltages are stored in external hold capacitors, CTH1 and CTH2, and then the loop is opened immediately thereafter. The corrected I and Q outputs are then fed directly to external circuitry for further baseband processing.
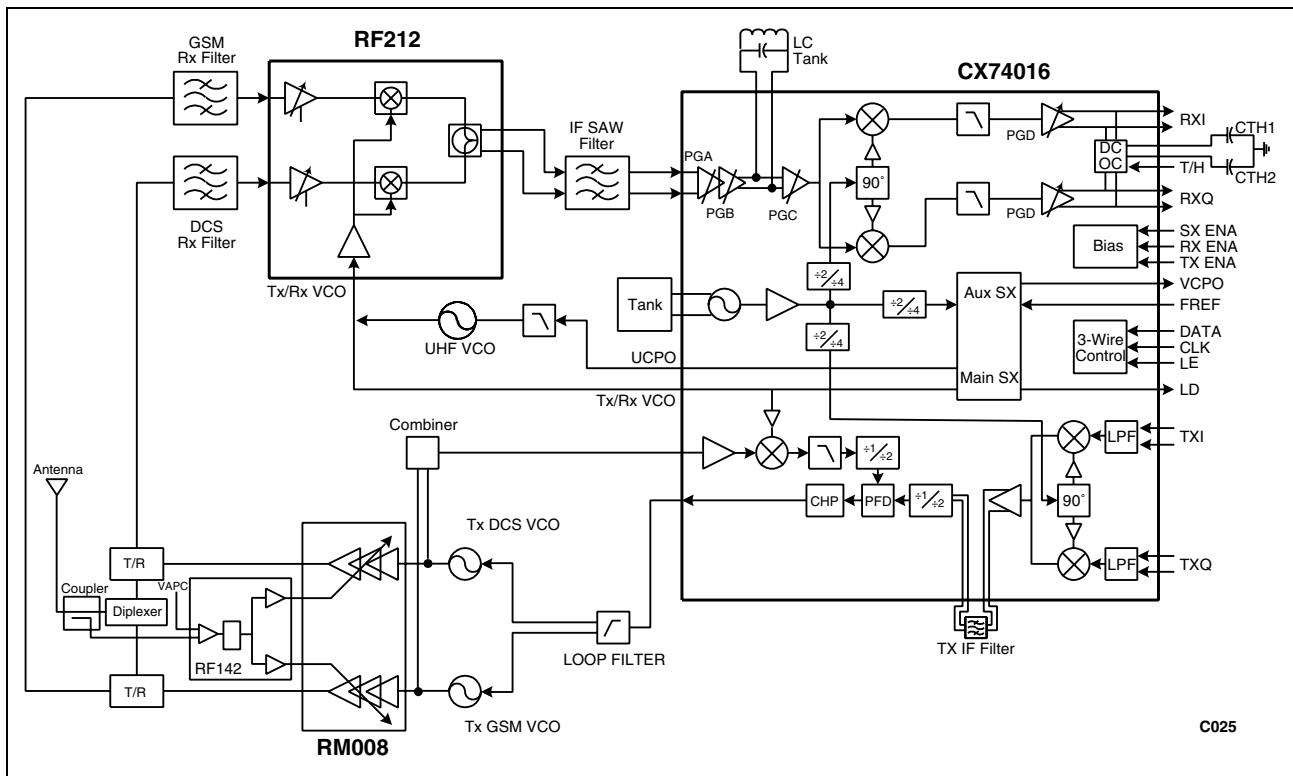

Figure 3. Typical Dual-Band Transceiver Application Block Diagram Using the CX74016
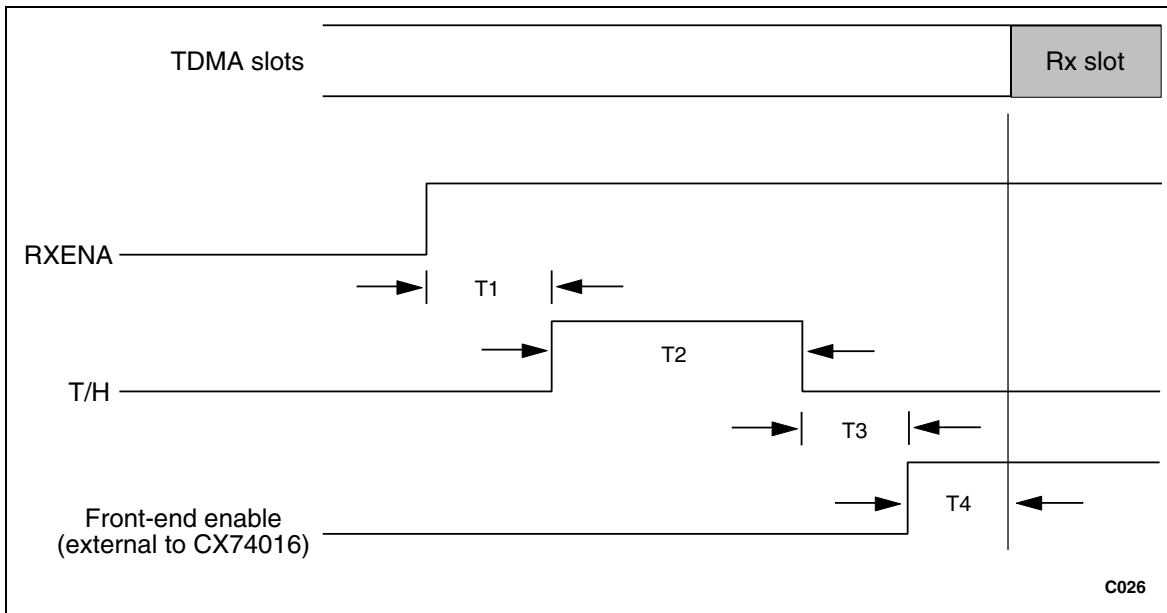
Figure 4. CX74016 Sample and Hold Timing Diagram

Table 2. Minimum Required DC Offset Calibration Time T2 and Droop Rate

Hold Capacitor (CTH1, CTH2)	22 nF	120 nF
Cold start	60 µsec	350 µsec
Frame-to-frame	10 µsec	60 µsec
Typical droop-rate (@ I/Q outputs)	1 mV/msec	0.17 mV/msec

The timing diagram for this calibration sequence in reference to the receive slot is shown in Figure 4 (the front-end mixer is assumed to be Conexant's RF212 dual-band, image reject downconverter). At first, the CX74016 receiver is turned on (RXENA is high). After time T1, the track and hold signal, T/H, places the DC compensation circuitry in the track mode for time T2. Then there is a settling time, T3, before the external front-end is turned on. Finally, the front-end must be turned on for time T4 before the receive slot.

Time T2 can vary from 10 µsec to 350 µsec. This duration is dependent on the value of the hold capacitors (CTH1 and

CTH2), and whether the calibration is done from frame to frame or from a cold start. This is tabulated in Table 2.

Because of on-chip loading currents, the hold capacitors (CTH1 and CTH2) slowly discharge causing the I and Q DC offset voltages to droop if the CX74016 remains uncalibrated for an extended period of time (the droop rate versus the hold capacitor is also shown in Table 2).

To rectify this voltage droop, it is recommended that recalibration occur before every receive slot (i.e., every 4.6 msec for GSM).
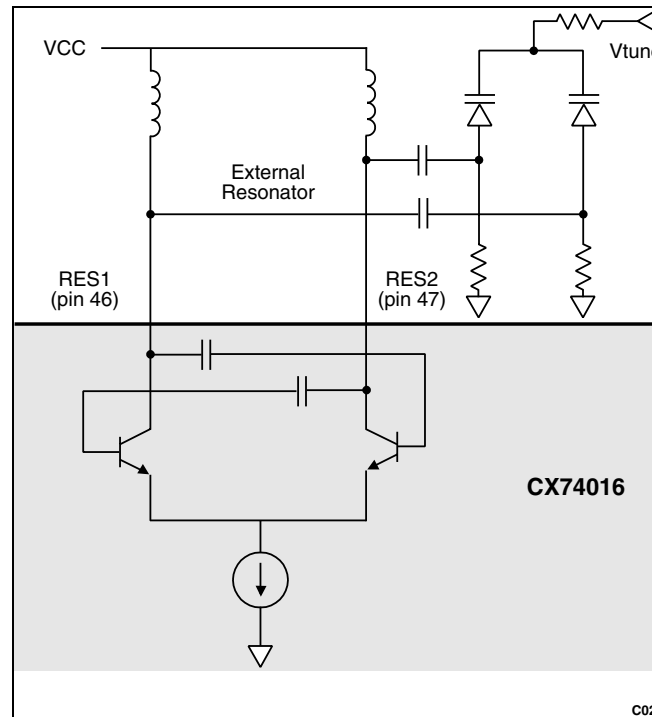
Figure 5. CX74016 Internal VCO

Synthesizer Section _____

Frequency Synthesizer. There are two frequency synthesizers on the chip, one primary and one auxiliary. The primary synthesizer provides frequencies from 500 MHz to 2 GHz. It consists of a 32/33 modulus prescaler, a 13-bit R counter, an 18-bit N counter, a phase detector with lock detection, and a charge pump. The auxiliary synthesizer, with frequency range from 50 MHz to 450 MHz, consists of an 8/9 modulus prescaler, a 13-bit R counter, a 16-bit N counter, a phase detector with lock detection, and a charge pump. Each synthesizer has four charge pump current settings for optimal performance.

On-Chip Oscillator with External Resonant Circuit. The on-chip VCO uses a fully differential architecture. This architecture inherently provides low even order harmonics, minimizing the phase variation of the phase shifters used to generate quadrature local oscillator signals. The architecture also provides better power supply rejection as well as superior immunity to common mode radiation as compared to single-ended designs. The immunity of the resonators minimizes the effect of pulling of the center frequency of the VCO due to the presence of a large signal in its spectral proximity.

The on-chip oscillator together with a few external components as resonant elements, form a VHF Voltage-Controlled Oscillator (VCO) (Figure 5 shows the VCO configuration). The differential VCO output is buffered and then fed to three dividers (Rx, Tx, and Sx). Each of the dividers have a selectable divide ratio of

either 2 or 4. The Rx and Tx dividers are both quadrature dividers that generate in-phase and quadrature-phase LOs.

The on-chip oscillator, with the on-chip auxiliary synthesizer, provides a complete VHF frequency synthesis for the Rx VHF LO and Tx VHF LO.

Three-Wire Bus Control Interface. The three-wire bus control allows the CX74016 to be optimized for any desired frequency plan. It also programs the two on-chip frequency synthesizers. To ensure that the data remains latched, one of the signals (TXENA, RXENA, or SXENA) must stay enabled.

When bit C0 is set to 1, it allows for divider selections in the translation loop, high-side/low-side injection for the image reject mixer, and the receive IF amplifiers' gain setting.

When bit C0 is set to 0, it programs the primary/auxiliary synthesizer, the R/N counter, charge pump polarity, charge pump output current, and prescaler setting.

Transmit Path _____

I/Q Modulator With IF Output Amplifier. The inputs to the I/Q modulator are differential I and Q baseband signals which are low-pass filtered and then applied to a pair of double-balanced mixers (see Figure 2). The outputs of the mixers are combined to produce a modulated signal which is then filtered externally and input through pins 8 and 9 (TXIFIN+ and TXIFIN–) to the reference divider in the translation loop.

Translation Loop Circuit. The translation loop circuit consists of a phase and frequency detector, a charge pump, a Tx RF input buffer, an LO input buffer, a mixer, two dividers, and a low pass filter.

The translation loop circuit, together with the external transmit VCO, external LO, and loop filter, form a Phase Locked Loop (PLL) with a mixer in the feedback loop. This PLL upconverts the modulated IF signal to the transmit frequency which then drives the final power amplifier. Since inherent bandpass filtering occurs in the PLL, the need for a post-Power Amplifier (PA) duplexer is removed.

This is the major advantage a translation loop approach has over the conventional upconversion scheme. The elimination of this duplexer reduces the loss in the transmit path which, in turn, reduces the required output level required from the final PA and, therefore, reduces the current consumption. Immediate benefits of this approach are increased handset talk time and standby time, and less component count.

The charge pump current can be programmed to be either 1 mA or 0.5 mA and the translation loop can also be programmed to allow for high side or low side injection of the first LO input with respect to the transmit RF.

Even greater flexibility in the transceiver frequency planning is possible because of the programmable dividers in the feedback and the reference paths.

Electrical and Mechanical Specifications _____

The absolute maximum ratings of the CX74016 are provided in Table 3, and the electrical specifications are provided in Table 4. Table 5, Table 6, and Table 7 detail the setting of the programmable operation modes.

Figure 6 illustrates the timing of the three-wire bus control signal. Figure 7 shows the 1 dB compression point graphs for the receiver. Figure 8 provides the package dimensions for the 72-pin device.

The CX74016 device has four metal ground paddles on the bottom of the LGA package. These paddles must be soldered to ground on the PCB. The PCB footprint design and soldering guidelines are described in the Conexant Application Note, "RF Land Grid Array Layout and Soldering Guidelines" (document #W205).

ESD Sensitivity

The CX74016 is a static-sensitive electronic device. Do not operate or store near strong electrostatic fields. Take proper ESD precautions.

Table 3. Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
Ambient Operating Temperature	−30	+85	°C
Storage Temperature	−50	+125	°C
Power Dissipation		600	mW
Supply Voltage (VCC)	0	4.5	V
Input Voltage Range	GND	VCC	V

Table 4. CX74016 Electrical Specifications (1 of 5)
(TA = 25 °C, VCC = 3.0 V, except where specified)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Receive IF Path						
Input impedance for the RXIF+ and RXIF− pins	Z_{IN}	Differential		500// 0.3		Ω pF
Input operating frequency	F_{IN}		70		450	MHz
Voltage gain	A_V A_V	F_{IN} = 400 MHz: High gain mode Low gain mode	57 −23	60 −20	63 −17	dB dB
Gain step (Note 1)	dA_V			2		dB
Gain step accuracy (Note 2)			−0.5		+0.5	dB
Single-sideband noise figure	NF NF	High gain mode Low gain mode		7 23		dB dB
Input 1 dB compression point (Note 3)	P_{1dB} P_{1dB}	High gain mode (60 dB) Low gain mode (−20 dB)		−75 −12		dBV dBV
IF filter pin impedance for the RXIFF+ and RXIFF− pins	Z_{IF}	Differential		300// 2		Ω pF
I/Q Demodulator						
I/Q amplitude imbalance					1	dB
I/Q phase imbalance			−4.5		+4.5	degrees
Noise figure	NF			15		dB
Output 1 dB compression point				−2		dBV
Baseband Filter						
Corner frequency (programmable)	F_C		50		150	kHz
Corner frequency variation	dF_C		−15		+15	%
Rejection		F_C = 105 kHz: @200 kHz @400 kHz @600 kHz	26	8 30 40		dB dB dB
Group delay		F_C = 105 kHz: DC to 100 kHz		3	5	μsec
Group delay variation		F_C = 105 kHz: DC to 100 kHz		300	500	nsec

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Table 4. CX74016 Electrical Specifications (2 of 5)
(TA = 25 °C, VCC = 3.0 V, except where specified)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Baseband Amplifier						
Voltage gain	Av			0 10 20 30		dB dB dB dB
Output amplitude		Av = 30 dB Av = 20 dB Av = 10 dB Av = 0 dB			2.5 1.8 1.0 0.4	Vp-p Vp-p Vp-p Vp-p
Output common mode voltage				1.35		V
Output offset voltage		With DC offset compensation			±5	mV
		Without DC offset compensation and Av = 0 dB			±100	mV
Output voltage droop/rise rate		With DC offset compensation and C_{TH} = 22 nF		1		mV/msec
Output impedance	Z_{OUT}	Differential		200		Ω
I/Q Modulator						
Input impedance	Z_{IN}	Differential @ 100 kHz		20		kΩ
Input signal level		Differential		1		Vp-p
Input common mode voltage range	V_{CM}		0.85	1.35	VCC – 1.35	V
Input offset voltage	V_{OS}			1	5	mV
Input frequency 3 dB bandwidth				10		MHz
Input common mode rejection ratio		F_{IN} = 100 kHz F_{IN} = 1 MHz		75 55		dB dB
Output operating frequency	F_{OUT}		70		425	MHz
Output impedance	Z_{OUT}	Differential @ 400 MHz		400// 3.1		Ω//pF
Output voltage	V_{OUT}		−20	−15		dBV
Output noise power	N_O	10 MHz offset		−130	−126	dBc/Hz
LO feedthrough				−45	−40	dBc
Sideband suppression			40	50		dBc
Spurious (Note 4)		@ 200 kHz offset @ 300 kHz offset		−70 −60	−40 −45	dBc dBc

Table 4. CX74016 Electrical Specifications (3 of 5)
(TA = 25 °C, VCC = 3.0 V, except where specified)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Translation Loop						
Transmit frequency (input from VCO)	f_{TX}		800		2000	MHz
LO input frequency	f_{LO}		800		2000	MHz
IF frequency	f_{IF} f_{IF}	With divide-by-2 With divide-by-1	70 70		425 300	MHz MHz
Transmit input power	P_{IN}	With external 50 Ω termination	−13	−10	−7	dBm
Transmit input impedance (at pin 68)	Z_{IN}	With pin 67 AC grounded		300// 0.3		Ω pF
LO input power with external 50 Ω termination	P_{IN}		−13	−10	−7	dBm
LO input impedance (at pin 65)	Z_{IN}	With pin 64 AC grounded		300// 0.3		Ω pF
Charge-pump output current	I_{OUT}	source/sink (CPOI=HIGH) source/sink (CPOI=LOW) high impedance		±1.0 ±0.5 0.02		mA mA mA
Transmit output zero crossing spurs (Note 5): 2X spurs 3X spurs 4X spurs 5X spurs			−62	−65 −70 −70 ≤−70		dBc dBc dBc dBc
Transmit output noise level (Note 5)		At 20 MHz offset from carrier		−165	−162	dBc/Hz
Device turn-on and lock time (with respect to enable input)		1 MHz loop bandwidth		30	100	μsec
VCO						
Operating frequency set by resonator	F_{VCO}		300		900	MHz
Tuning voltage range		Varactor ground referenced	0.3			V
		Varactor supply referenced			VCC − 0.3	V
Resonator pin impedance		Differential		10k// 0.4		Ω pF
Tuning sensitivity (Note 6)	K_{VCO}	F_{VCO} = 800 MHz		50		MHz/V
Phase noise (Note 6)		F_{VCO} = 800 MHz, 400 kHz offset, resonator Q = 20		−122		dBc/Hz

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Table 4. CX74016 Electrical Specifications (4 of 5)
(TA = 25 °C, VCC = 3.0 V, except where specified)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Synthesizer						
Input frequency (low frequency mode), Auxiliary PLL	$f_{INL(IF)}$		100		260	MHz
Input frequency (high frequency mode), Auxiliary PLL	$f_{INH(IF)}$		250		450	MHz
Input frequency (low frequency mode), Primary PLL	$f_{INL(RF)}$		500		1200	MHz
Input frequency (high frequency mode), Primary PLL	$f_{INH(RF)}$		500		2000	MHz
Reference frequency	f_{REF}		1		40	MHz
Reference input sensitivity	R_{IN}		500			mVpp
Phase detector frequency	f_{PD}		10		10000	kHz
Charge pump output impedance	Z_O			10		MΩ
Prescaler input sensitivity	P_{IN}		100			mVpp
Prescaler input impedance	Z_{IN}	@ 1 GHz		100		Ω
PLL contribution to phase jitter (N=5835)	Φ_{NMAIN}	Primary only; Fcomparison = 200 kHz, 10 kHz loop BW; integrated from 200 to 270,000 Hz		1.2		degrees RMS
PLL contribution to phase jitter (N=1680)	Φ_{NAUX}	Aux only; Fcomparison = 300 kHz, 10 kHz loop BW; integrated from 200 to 270,000 Hz		0.75		degrees RMS
Primary charge pump current, step 0	$I_{DOR,0}$	t = 25 °C	0.6	0.8	1.0	mA
Primary charge pump current, step 1	$I_{DOR,1}$	t = 25 °C	0.9	1.2	1.5	mA
Primary charge pump current, step 2	$I_{DOR,2}$	t = 25 °C	1.35	1.8	2.25	mA
Primary charge pump current, step 3	$I_{DOR,3}$	t = 25 °C	2.02	2.7	3.38	mA
Auxiliary charge pump current, step 0	$I_{DOI,0}$	t = 25 °C	0.4	0.5	0.67	mA
Auxiliary charge pump current, step 1	$I_{DOI,1}$	t = 25 °C	0.6	0.8	1.0	mA
Auxiliary charge pump current, step 2	$I_{DOI,2}$	t = 25 °C	0.9	1.2	1.5	mA
Auxiliary charge pump current, step 3	$I_{DOI,3}$	t = 25 °C	1.35	1.8	2.25	mA
Charge pump current relative step size (current change from any one step to next step in sequence)	I_{DOS}		40	50	60	%
Charge pump leakage current	I_{DOO}			0.1		nA
Charge pump output voltage compliance	V_{DO}		0.5		VCC – 0.5	V
Lock detect time constant	t_{LOCK}			500		μsec

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Table 4. CX74016 Electrical Specifications (5 of 5)
(TA = 25 °C, VCC = 3.0 V, except where specified)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Transceiver						

DC offset calibration timing (see Figure 4):
    T1
    T2 (see Table 2)
    T3
    T4 (assuming RF212 front-end mixer)
				40
				
				5
				20
						μsec
						μsec
						μsec
						μsec

Enable and control VIH	V_{IH}		$0.8 \times$ VCC			V
Enable and control VIL	V_{IL}				$0.2 \times$ VCC	V
Enable and control IIH	I_{IH}			20	60	μA
Enable and control IIL	I_{IL}		−10	−1	0	μA

Total supply current (Note 7):
    Rx mode
 	
    Tx mode
 	
    Synthesizer mode
	I_{CC}	SXENA = RXENA = on
		SXENA = TXENA = on
		SXENA = on
				63
				
				64
				
				28
						mA
						
						mA
						
						mA

Power supply range	VCC		2.7	3.0	3.6	V
Operating temperature range	T_A		−30	+25	+85	°C
3-Wire Control						
Data to clock setup time (Note 8)	t_{CS}		50			nsec
Data to clock hold time (Note 8)	t_{CH}		10			nsec
Clock pulse width high (Note 8)	t_{CWH}		50			nsec
Clock pulse width low (Note 8)	t_{CWL}		50			nsec
Clock to load enable setup time (Note 8)	t_{ES}		50			nsec
Load enable pulse width (Note 8)	t_{EW}		50			nsec
Load enable transition to clock start time	t_{LS}		50			nsec

Note 1: Gain steps are such that monotonicity is maintained throughout the entire IF gain range.

Note 2: Specified down to 2.8 V supply voltage. Slight degradation at temperature extremes for 2.7 V supply voltage.

Note 3: Refer to Figure 7 for the 1 dB compression point of the entire receiver chain, including the baseband gain section.

Note 4: For 1 Vp-p 100 kHz differential signals across I_{IN} and Q_{IN}.

Note 5: Using transmit VCO with similar characteristics as Murata MQE 550-902.

Note 6: Using varactors with similar characteristics as Alpha part SMV1234-004.

Note 7: The total voltage supply current for the Rx, Tx, and synthesizer modes increases by 1 mA if the VHF LO buffer is on.

Note 8: Refer to Figure 6.

Table 5. CX74016. Control Bits and Output States (1 of 2)

Block	C0	Bit	Function	Description
LO	1	S1	RX LO ÷2/÷4	Selects the division ratio for RX LO2 (0 = division ratio is 2; 1 = division ratio is 4)
		S2	SX LO2 ÷2/÷4	Selects the division ratio for SX LO2 (0 = division ratio is 2; 1 = division ratio is 4)
		S3	TX LO ÷2/÷4	Selects the division ratio for TX LO2 (0 = division ratio is 2; 1 = division ratio is 4)
TX	1	S4	TX IF ÷1/÷2	Selects the division ratio for TX IF (0 = division ratio is 1; 1 = division ratio is 2)
		S5	TX MIX OUT ÷1/÷2	Selects the division ratio for TX MIX output signal (0 = division ratio is 1; 1 = division ratio is 2)
		S6	TX LO Injection	Selects between high- and low-side injection of first LO input with respect to transmit RF (0 = low side, 1 = high side)
		S7	CP Output Current	Selects the TL loop CP output current (0 = output current is 0.5 mA; 1 = output current is 1 mA)
Receive	1	S8 S9 S10 S11 S12 S13 S14 S15 S16 S17 S!8	RX PGA1 RX PGB1 RX PGB2 RX PGB3 RX PGB4 RX PGC1 RX PGC2 RX PGC3 RX PGC4 RX PGD1 RX PGD2	Selects the RX IF/baseband gain (see Tables 6 and 7)
TRX	1	S19	Reserved	S19 bit may be programmed as "don't care."
		S20	Reserved	S20 bit may be programmed as "don't care."
		S21	VHF LO BUF	Selects the state of the LO buffer (1 = LO buffer on; 0 = LO buffer off). Needs to be "1" for correct operation.
		S22	VHF Prescaler	Select the state of the VHF prescaler (1 = on, 0 = off).
		S23	UHF Prescaler	Select the state of the UHF prescaler (1 = on, 0 = off). Set to "1" for normal operation.

Table 5. CX74016. Control Bits and Output States (2 of 2)

Block	C0	Bit	Function	Description
SX	0	S1	IF/RF	Selects one of the synthesizers, either the Auxiliary or Primary (1 = primary; 0 = auxiliary)
		S2	R/N	Selects the R counter or N counter register within the synthesizer. The N counter register also controls the phaser detector current and inversion (or phase comparison reference signal) (0 = N counter register; 1 = R counter register)
		S3	S2 = 0: Prescaler frequency response	Determines the maximum input frequency at which the prescaler will operate: S1 = 1 Primary: 0 = 1.2 GHz, 1 = 2.0 GHz S1 = 0 Auxiliary: 0 = 260 MHz, 1 = 450 MHz
			S2 = 1: Output invert	Controls polarity of charge pump output (0 = normal operation; 1 = inverted)
		S4	S2 = 0: Synth. power down	Powers down the synthesizers. Only the synthesizer indicated by S1 is affected (0 = normal operation; 1 = power down)
			S 2= 1: Test mode inhibit	Used to inhibit lock detect/test output (0 = lock detect/test output enable; 1 = lock detect/test output disable)
		S5 to S22	S2 = 0: N counter	This 18-bit value is loaded into the N counter latch. This value sets the cascaded division ratio of the prescaler and N counter (S22 = MSB, S5 = LSB). For the auxiliary N divider (16-bit), bits S21 and S22 are "don't care." The least significant bits (S5-S9 for primary N divider; S5-S7 for auxiliary N divider) set the prescaler counter.
		S5- S6	S2 = 1: Output current	These bits set the charge pump output current: S1 = 1 Primary: 00 = 0.8, 01 = 1.2, 10 = 1.8, 11 = 2.7 [mA] S1 = 0 Auxiliary: 00 = 0.5, 01 = 0.8, 10 = 1.2, 11 = 1.8 [mA]
		S7	S2 = 1: CP high impedance	Charge pump output. Only the charge pump output selected by the S1 bit is affected (0 = normal operation; 1 = high impedance)
		S8- S9	S2 = 1: Test mode	These bits select which signal to output at the lock detect/test pin (pin 36): 00 = (Lock detect of Aux) AND (lock detect of Primary) 01 = Output of R divider 10 = Output of N divider 11 = Output of lock detect Aux (S1=0) or Primary (S1=1)
		S10- S22	S2 = 1: R counter	These 13 bits set the reference divider value (S22 = MSB, S10 = LSB).

Table 6. Receive Baseband Gain

Gain (dB)	PGD	
	1	2
30	1	1
20	1	0
10	0	1
0	0	0

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Table 7. Receive IF Gain

Gain (dB)	PGA 1	PGB 1	PGB 2	PGB 3	PGB 4	PGC 1	PGC 2	PGC 3	PGC 4	Gain (dB)	PGA 1	PGB 1	PGB 2	PGB 3	PGB 4	PGC 1	PGC 2	PGC 3	PGC 4
60	1	1	1	1	1	1	1	1	1	18	0	0	1	0	0	1	1	1	1
58	1	1	1	1	0	1	1	1	1	16	0	0	0	1	1	1	1	1	1
56	1	1	1	0	1	1	1	1	1	14	0	0	0	1	0	1	1	1	1
54	1	1	1	0	0	1	1	1	1	12	0	0	0	0	1	1	1	1	1
52	1	1	0	1	1	1	1	1	1	10	0	0	0	0	0	1	1	1	1
50	1	1	0	1	0	1	1	1	1	8	0	0	0	0	0	1	1	1	0
48	1	1	0	0	1	1	1	1	1	6	0	0	0	0	0	1	1	0	1
46	1	1	0	0	0	1	1	1	1	4	0	0	0	0	0	1	1	0	0
44	1	0	1	1	1	1	1	1	1	2	0	0	0	0	0	1	0	1	1
42	1	0	1	1	0	1	1	1	1	0	0	0	0	0	0	1	0	1	0
40	1	0	1	0	1	1	1	1	1	–2	0	0	0	0	0	1	0	0	1
38	1	0	1	0	0	1	1	1	1	–4	0	0	0	0	0	1	0	0	0
36	1	0	0	1	1	1	1	1	1	–6	0	0	0	0	0	0	1	1	1
34	1	0	0	1	0	1	1	1	1	–8	0	0	0	0	0	0	1	1	0
32	1	0	0	0	1	1	1	1	1	–10	0	0	0	0	0	0	1	0	1
30	1	0	0	0	0	1	1	1	1	–12	0	0	0	0	0	0	1	0	0
28	0	1	0	0	1	1	1	1	1	–14	0	0	0	0	0	0	0	1	1
26	0	1	0	0	0	1	1	1	1	–16	0	0	0	0	0	0	0	1	0
24	0	0	1	1	1	1	1	1	1	–18	0	0	0	0	0	0	0	0	1
22	0	0	1	1	0	1	1	1	1	–20	0	0	0	0	0	0	0	0	0
20	0	0	1	0	1	1	1	1	1										
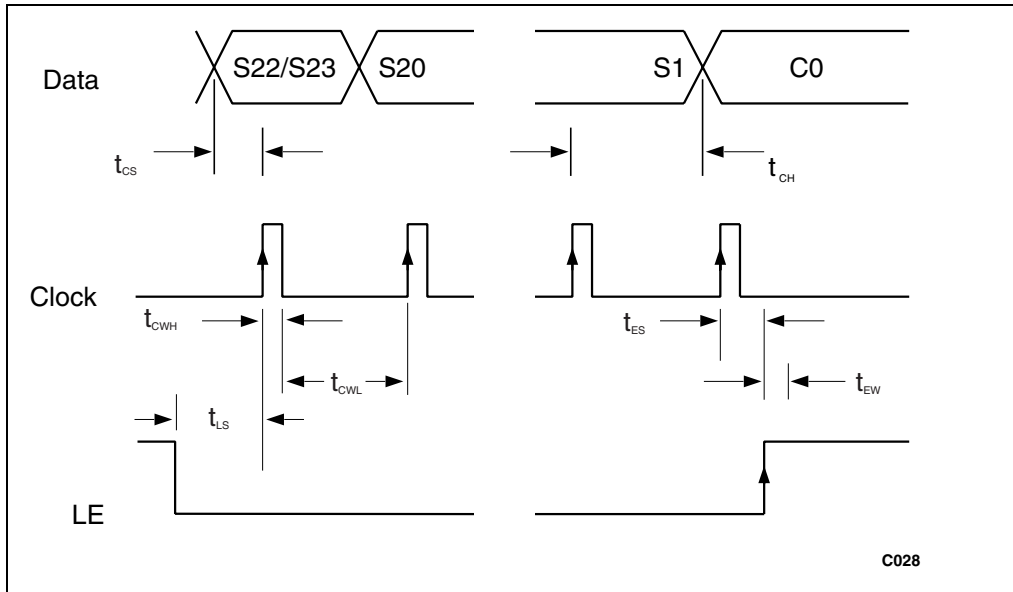
Figure 6. CX74016 Timing Diagram
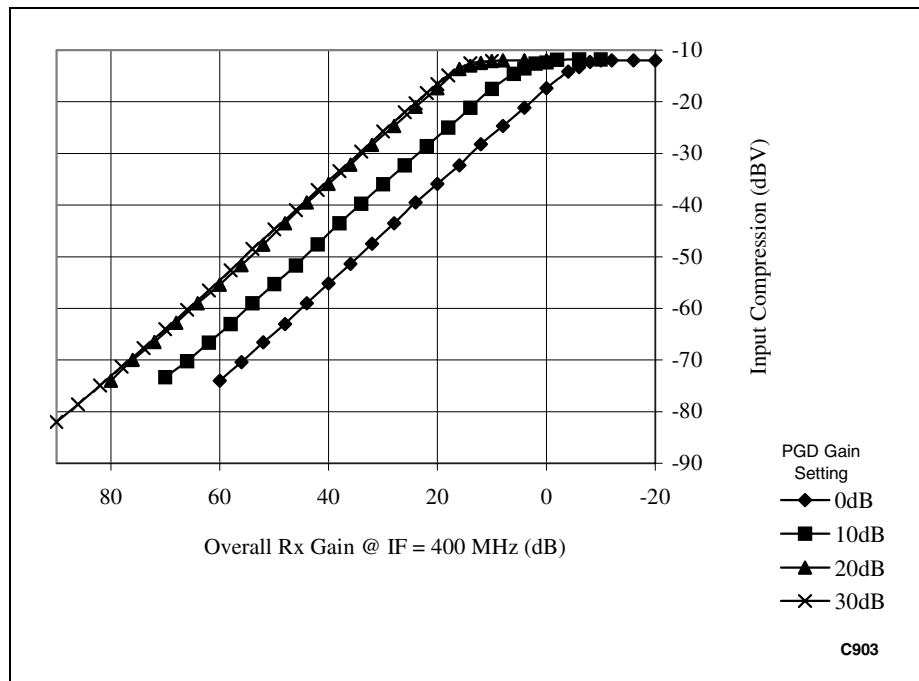
Figure 7. Receiver Input Compression Graph

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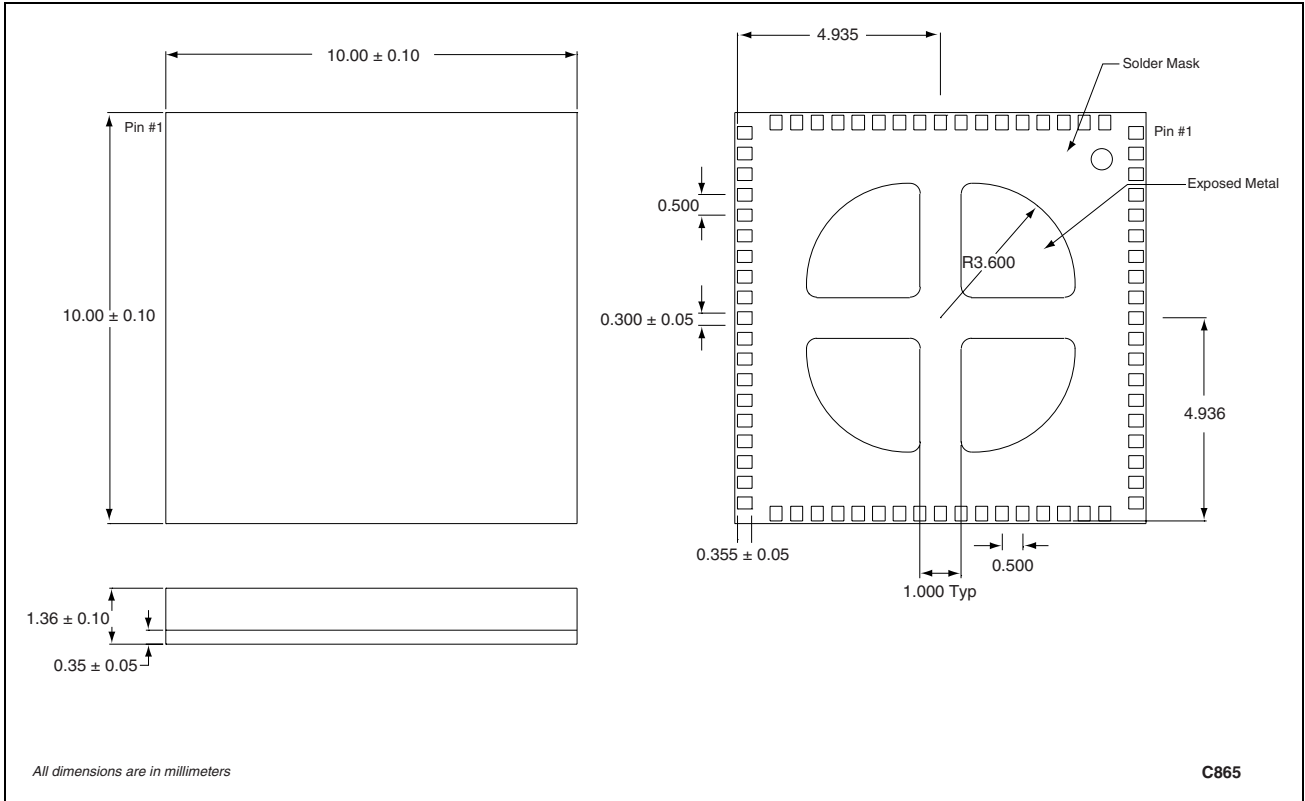
Figure 8. CX74016 Package Dimensions – 72-Pin LGA

Ordering Information

Model Name	Manufacturing Part Number	Product Revision
CX74016	CX74016	

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