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Timing, Reading the AC Characteristics

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1 Reading the AC Characteristics

Besides the power supply, the basis of a microprocessor or -controller is the internal clock system, called CPU Clock for the C16x-family. All actions, whether they are internal or external at the pins, are based on this CPU Clock. That means, each signal is triggered by a specific clock edge.

This is of course also true for the external bus timing. Each change of an external signal is triggered by a specific internal clock edge of the CPU Clock. To illustrate this relationship, one could draw a so-called *nominal* timing diagram of the external bus. Figure 1 shows such a *nominal* timing diagram for the case of a multiplexed bus. One can see the internal clock and the bus signals generated by each specific clock edge. This nominal diagram does not take into account any delays introduced through internal gates and wires, etc., or rise and fall times of the signal transitions.

Figure 1: Multiplexed Bus, Nominal Timing
CPU Clock = f1

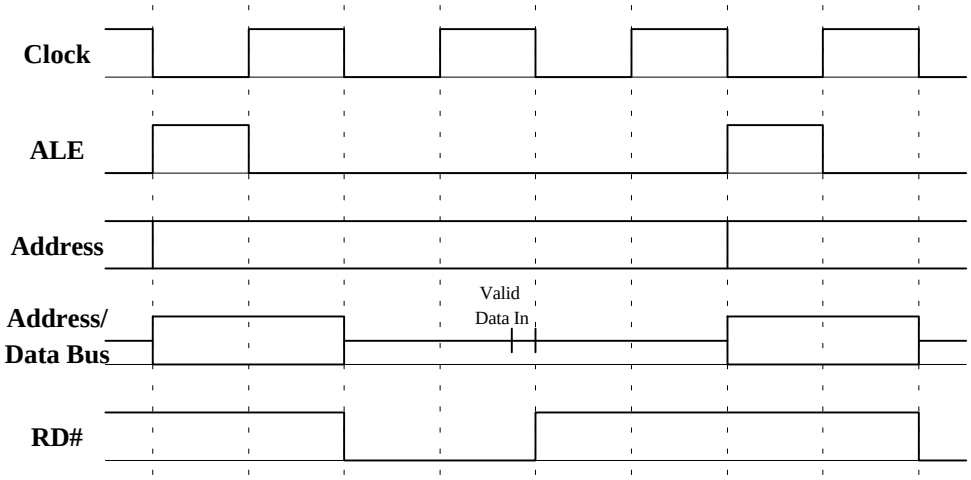

Figure 1:
Multiplexed Bus, Nominal Timing - CPU Clock = f1

The vertical lines in the diagram represent the internal clock phases, the TCL's. The diagram shows the sequence of the signals, their triggering clock edge and their duration counted in TCLs. This fundamental timing does not change with varying clock frequencies. Figure 2 shows the same relation for another clock frequency, only the scale has changed.

This nominal timing can help very much when analyzing and calculating timing relations which are not explicitly given in the AC-Characteristics of the respective Data Sheets. One can for instance easily see that a specific signal is nominally generated one or more TCLs after another signal, although the worst case calculation taken from different timing parameters of the Data Sheet would show an overlapping of these signals (however, such calculations are not allowed; an example is given at the end of this document).

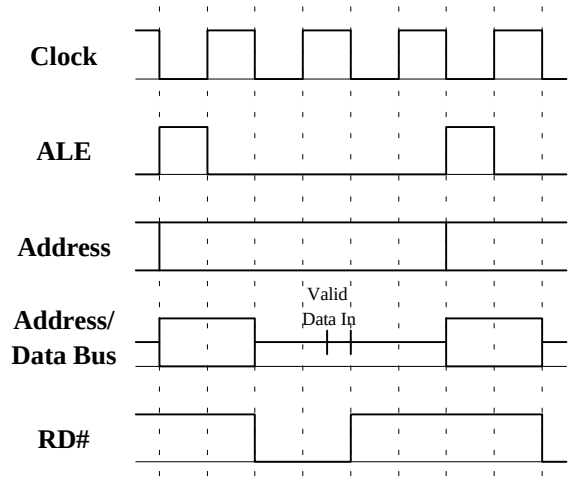

Figure 2:
Multiplexed Bus, Nominal Timing - CPU Clock = f2

But where to get the right information without the nominal timing? The answer is, it's in the Data Sheet! The most interesting columns in the AC-Characteristics of the Data Sheets are not the ones with the precalculated values for the maximum frequency of e.g. 20MHz, but the ones which are titled 'Variable Timing'. In these columns each AC-parameter is given in the format

x * TCL - y

If the term '- y' part is omitted in these formulas, one gets the nominal timing of a signal. The following examples will illustrate this: The ALE signal is specified in the Data Sheet with t5 = TCL - 10 [ns] (the unit [ns] will be omitted in the following). When the '- 10' is omitted, the formula states that the nominal length of ALE is t5 = TCL. The diagram in Figure 1 proves this relation. The specification for the RD# or WR# low time is t12 = 2TCL - 15. Thus, the nominal duration of these signals is 2TCL, which is also reflected in Figure 1. The sequence of the ALE and the RD#/WR# signals is given by t8 = TCL - 10. In a verbal description, one could express the nominal timing as 'the duration of the ALE signal is one TCL; one TCL after the deactivation of ALE the RD# or WR# signal is generated for the duration of 2 TCL'.

For a full interpretation of the AC-Characteristics one should always use the nominal timing (expressed through the TCLs), the verbal description of the parameter (gives additional information on the sequence of signals, e.g. 'ALE falling edge to RD# or WR#'), and the waveform drawings.

In reality, of course, there never exists a microcontroller with such a nominal timing. There are delays introduced on the way from the original clock synchronous generation of a signal to the external pins. These delays are due to logic gates, wire capacitance and

inductance, such that a signal is normally appearing at the pin some nanoseconds later that generated internally. In addition, these delays are very dependant on the power supply voltage and the temperature. Gate delays are also affected by technology and production line variations. Taking this into account, it is easy to understand that signals arrive at the pins with a significant time skew in relation to the internal clocks. And it also becomes clear that signals, although generated internally with exactly the same clock edge, may appear at the pins with different delays.

The values given in the Data Sheets must take all these variations into account in order for the manufacturer to guarantee reliable parameters over the full life span of a component. Therefore, the '-y' part of the timing formula is chosen such that on one hand an economical reasonable amount of good components (the yield) can be produced, and that on the other hand the timing requirements for the external components are acceptable. In addition, in order to reduce testing time (and therefore costs) in most cases only one limit for a timing parameter is given in the data sheet. This is normally the value really required by a system designer.

Now it is easy to understand how the formulas in the 'Variable Timing' column of the data sheets are generated. The 'x*TCL' part represents the basic nominal timing which is frequency dependent, while the '-y' part represents the variations caused by gate delays, operating conditions, etc. This part is frequency independent.

A short example will demonstrate this. The 'ALE High Time' is specified in the data sheet with 1TCL-10. This means that the nominal duration of the ALE signal is one TCL (i.e. 25ns @ 20MHz or 30ns@ 16.67MHz CPU Clock), under typical conditions (e.g. room temperature, 5.0V VCC, etc.) this value normally will be met. A possible variation of the ALE duration is expressed through the fixed, frequency independent time of 10ns. This time takes into account possible different delays of the rising or falling edge of ALE in relation to the internal triggering clock edges. In addition, the rise and fall times of the ALE edges must be considered. They are influenced by the internal output buffer structure and the external loading which both may result in differnt rise and fall times. Note that the parameters in the data sheet are given for a maximum capacitive loading of 100pF for the bus related signals.

Another important fact is that the timing is specified for TTL levels. Both TTL levels are specified at voltages below 0.5*VCC. However, the levels generated by the controller are in reality near GND for a low level and near VCC for a high level. When a signal changes from low to high it will reach the TTL high level after a voltage shift of ca. 2V. However, when a signal switches from high to low, a voltage transition of ca. 4V must be made. It is obvious that this would take more time than for the low to high transition. In addition, the TTL level at which certain timings are evaluated can be different for different signals. For example, the parameter t8 (ALE falling edge to WR#) is measured from the point where the falling edge of ALE has reached the TTL low level until the point where the falling edge of the write signal leaves the TTL high level (until this point the write signal is recognized by external components as surely being high). The parameter t12 (WR# low time), however, is measured from the point where the falling edge of the write signal has reached the TTL low level, until the rising edge of this signal leaves the TTL low level again (this is the time during which the write signal is surely recognized as low by external components). Any other timings related to the rising edge of the write signal are related to

the point where the write signal has reached the TTL high level (write signal is surely recognized as being high). One can see that these different evaluation points can cause an additional delay which must be taken into account in the '-y' part of the calculation formula.

Figure 3 illustrates the possible delays of a signal compared to the internal timing. Delay d1 is caused by internal gate delays. The time d2 is measured from the internal timing until the signal leaves the TTL low level, while d3 is the time when the signal reaches the TTL high level. For the falling edge, d4 is the time for the signal to start the transition from high to low. The signal will leave the TTL high level after the delay d5, and will finally reach the TTL low level after the time d6.

Figure 3: Possible Delays of a Signal

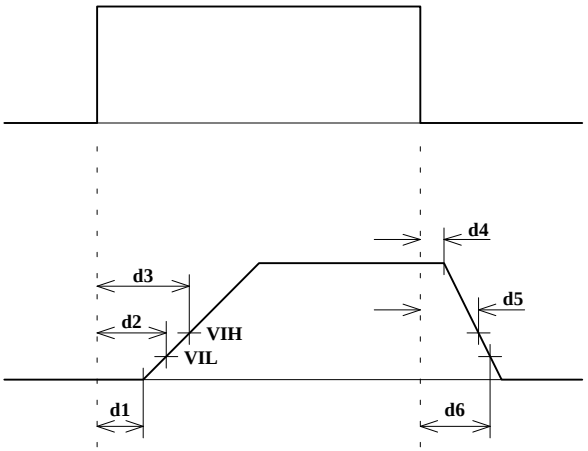

Figure 3:
Possible Delays of a Signal

Now it is clear that every signal generated internally by a specific clock edge always appears at the pin a certain delay after the internal clock edge; it can of course never change before this clock edge. Thus, the real timing of a controller which can be seen at the pins is delayed in time compared to the internal clocks. Figure 4 shows this fact by a shift to right of the external bus signals. In addition, the rise and fall times of the signals are taken into account. In the data sheets, of course this real timing at the pins of the controller must be specified, and all possible delays must be considered.

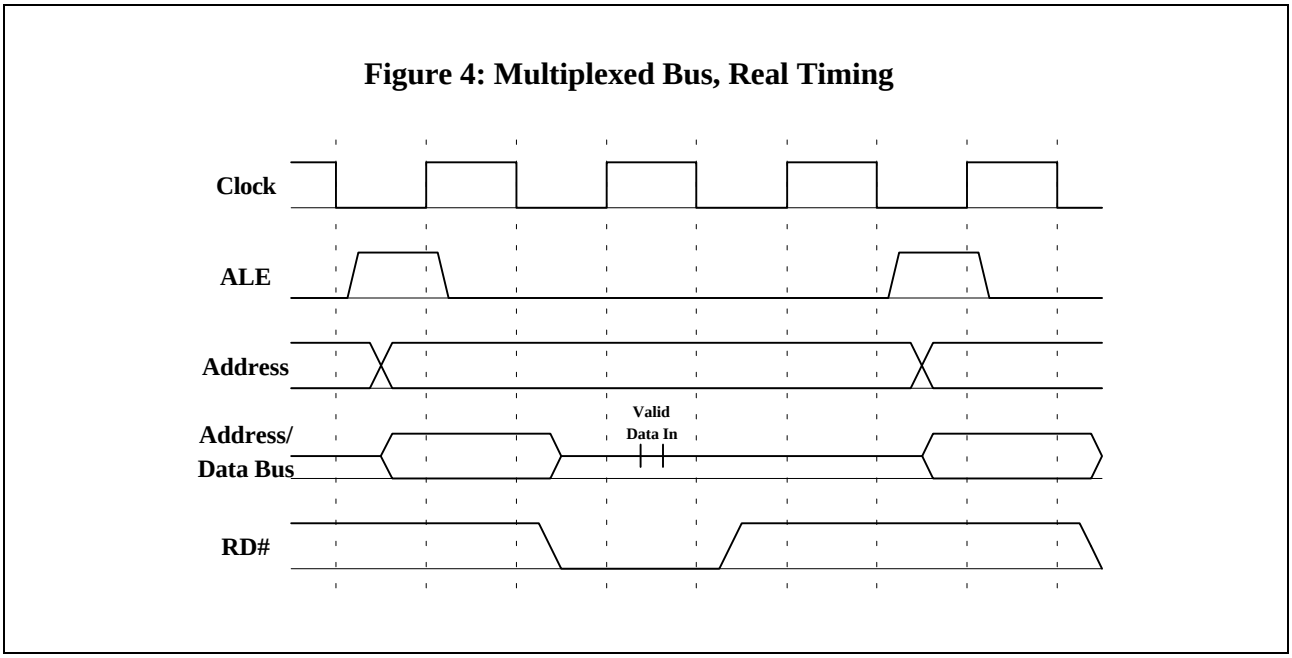

Figure 4:
Multiplexed Bus, Real Timing

As shown above, all signals which are generated by the controller and output at the pins are delayed in relation to the internal timing. But what is the situation for signals which the controller requires from the external world?

The most important signal from the external world is an instruction read from an external memory. In order to process this information, the controller must latch this byte or word internally; and this, naturally, is done with an internal clock. Any latch needs a setup time of the data input before the clock edge. In addition, the instruction arrived at the pins of the controller has to pass some gates from the pin to the internal latch. Thus, the signal delays for data input into the controller now act in the opposite direction: The data must be present at the pins some gate delays plus the latch setup time earlier than the internal latching clock edge. This is also shown in Figure 4, the 'Valid Data In' point is shifted to the left compared to the nominal timing shown in Figure 1.

This shows, why in the data sheets the timings referring to 'Valid Data In' are more limited than other parameters, their 'y' value is greater. As an example, the parameter 'RD# to Valid data In' is discussed in the following. For an ideal nominal timing, without even a setup time for the latch, the time from the falling edge of RD# until the data is latched internally is 2TCL (see Figure 1). The clock edge for the internal latch is a fixed time point, but due to the delay 'y1' of the RD# signal at the pin, the time is shortened to 2TCL-y1. In addition, the external data requires a delay 'y2' to go from the pin to the internal latch. Considering now the data setup time 'y3' for the latch, one can see that the time 'RD# to Valid Data In' must be specified to 2TCL-y = 2TCL-y1-y2-y3.

When designing a system, even more delays must be considered here as shown in Figure 5. The data sheet parameters are specified for the signals at the pins of the controller. What now must be taken into account are the delays of the signals from the controller

pins to the memory, and back from the memory to the pins of the controller. In this path, delays can be caused by signal wiring, capacitances, or other components such as decoders or data drivers. These delays will additionally limit the time for the memory to provide the valid data. Thus, it is not enough for a system designer to only look at the data sheet parameters of the controller for an evaluation of the required memory speed. Any value here is stated without consideration of any additional delays in the system, since these can only be determined and controlled by the user.

Figure 5: Output, System, and Input Delays

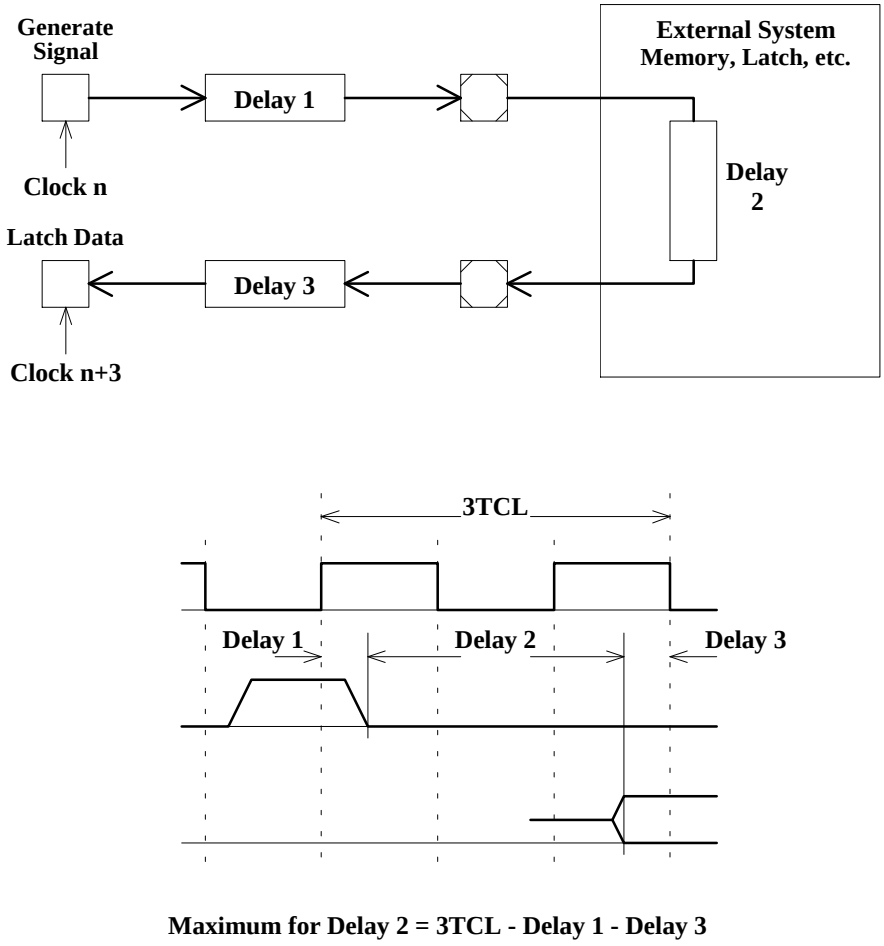

Figure 5:
Output, System an Input Delays

Now back to the timing of the controller. As mentioned before, in most cases only one limit is given for a timing parameter in the data sheet, either the maximum or the minimum time. The given limits are the values which are normally required to design a system. For instance, one will nearly always find a specification for a minimum time of the write pulse required by a memory, but there is no limit for the maximum time the write signal is allowed to be low. Thus, in the data sheet of the controller, only the minimum time is specified. Since all parameters given in the data sheet must be guaranteed, and therefore normally must be measured, any additional parameters would increase the testing time and the costs of the component. In order to operate economically, a tradeoff must always be made between the necessity of a parameter and the additional costs for it.

From the nominal timing, in nearly all cases the ‘missing’ limit of a signal timing can be evaluated. As an example, the ‘RD# Low Time’ is only specified as a minimum time of 2TCL-10ns. The nominal activation is 2TCL, and one can now expect that the maximum duration will not be much more than these 2TCL. Here one can make the following considerations: First, it is very obvious that a signal, which is nominally generated for the duration of 2TCL will not last 3 or 4TCL. The second consideration is an analysis of the given values. The specified worst case minimum time of 2TCL-10ns covers the case where the falling edge of the RD# signal comes very late, while the rising edge comes very early. Any other case would result in a greater time as specified. If both edges would have exactly the same delay (TTL levels and possible different rise and fall times are disregarded in this context), the RD# low time would result exactly to 2TCL (but the signal is shifted by a certain delay compared to the internal timing). The remaining case is the one where the falling edge comes very early, but the rising edge comes very late. Assuming the same delay of 10ns here as for the first case, would give a maximum low time for the RD# signal of 2TCL+10ns. Of course, this can only be used for an estimation of the maximum time, but taking signal delays of about 10ns to 15ns will in most cases give reasonable results.

Similar considerations should be made when interpreting the timing relationship between different signals. As an example, the relationship between ALE, RD# and WR# for the case of a demultiplexed bus without read/write delay (and without any waitstates) is analyzed. The parameter t9 (ALE falling edge to RD#, WR#) is specified to -10ns. The falling edge of ALE and the falling edge of RD# or WR# are generated by the same internal clock edge. Since no signal can change before its triggering clock edge, the specified worst case situation can only happen if the RD# or WR# signal has a very small delay and comes close after the internal clock edge. But the ALE signal has an additional delay of 10ns and therefore comes later than RD# or WR# by a maximum time of 10ns. At the end of the bus cycle, the parameter t26 (ALE rising edge after RD#, WR#) is also specified with -10ns. Again, all signals are generated by the same internal clock edge. Thus, the specified worst case must be the one where ALE comes very early, while the RD# or WR# signal has an additional delay of 10ns compared to the ALE signal. It is obviously very unlikely, that for sequential bus cycles (which can be considered to have the same operating conditions in terms of temperature, VCC, etc.) both worst case timings are in effect, which means that the rising edge of ALE is coming very early, but the falling edge comes very late. This would result in an ALE high time of more than one TCL. If now the specified minimum high time for ALE of TCL-10ns is taken, one can see that it is not possible to fit these values together. The result is, that each value given in the data sheet represents the specific worst case value for the specific timing relationship given by this parameter. For one relationship the worst case might be a high temperature and a low voltage, for the other relationship the worst case is the opposite condition, a low temperature and a high voltage.

Conclusion: It does not make sense to add or subtract different data sheet parameters in order to calculate signal relations not explicitly given in the data sheet. Furthermore, one should never take the precalculated values given in the data sheet column for a specific frequency, but always try to find signal relations by using the nominal timing parameters in the column ‘Variable Timing’ and perform the considerations explained above.