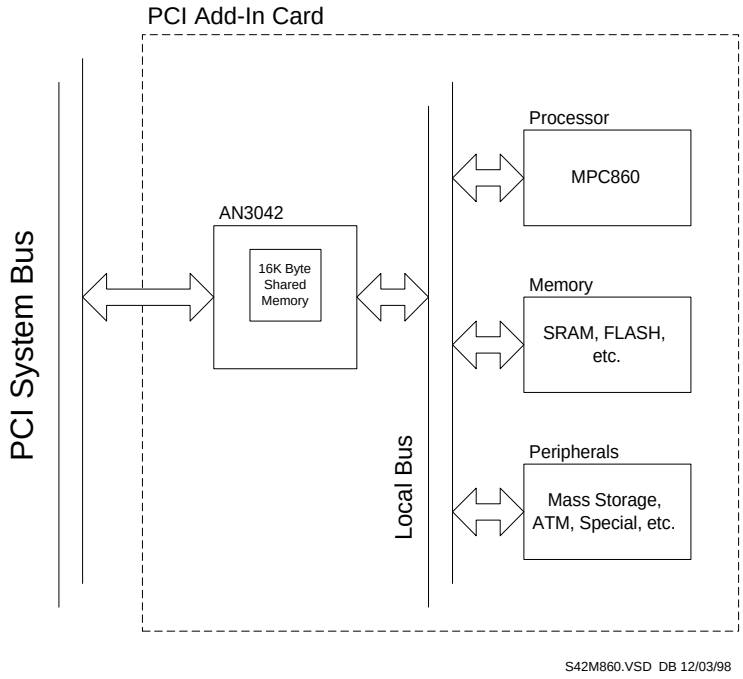
Overview

The AN3042Q interfaces directly to the TI MPC860 PowerQUICC processor. The interface described in this application note connects a 32-bit, 40 MHz MPC860 to the AN3042Q.

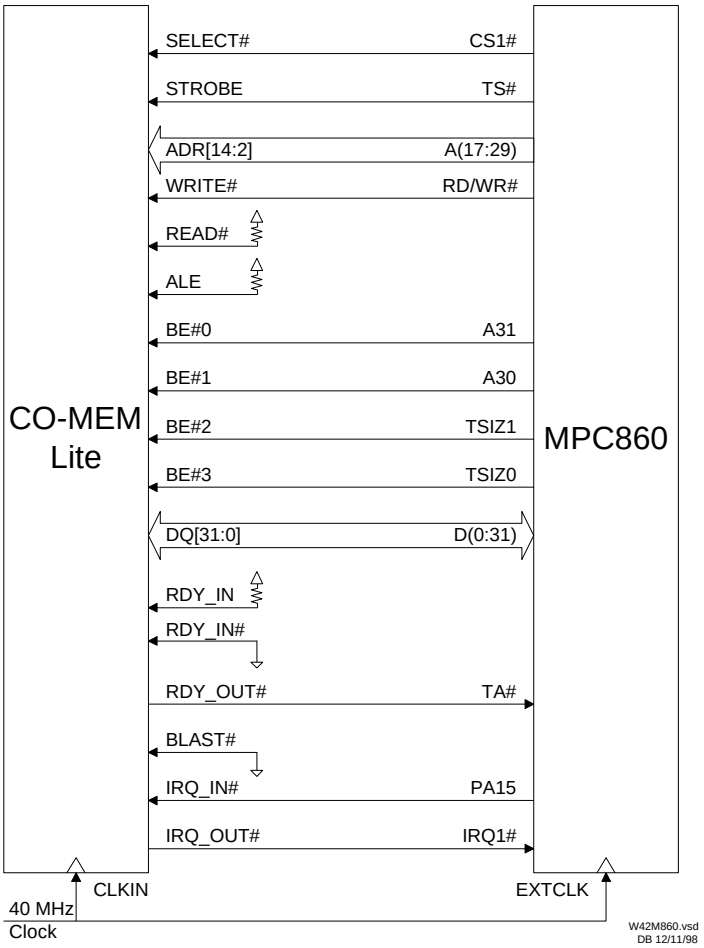
System Block Diagram

The AN3042Q connects the MPC860 to the PCI system bus.



Wiring Diagram

Wiring the AN3042Q to the MPC860 is simple. The interrupt connections in the diagram are not required for the bus interface; they are only included for illustrative purposes. Note that the MPC860 signal naming convention is that least significant bits have the higher bit numbers. For instance, the least significant data bit of a 32-bit bus is D31 and the most significant bit is D0. The AN3042Q signal naming convention is consistent with that of the PCI bus and other little endian conventions. To maintain proper significance in bit ordering, the signals are connected as shown in the diagram. For example the MPC860 data bit 31 is connected to the AN3042Q data bit 0. The addresses are wired in the same way.



AN3042Q Configuration Programming

The AN3042Q Local Bus Configuration register must be programmed to support the MPC860 external bus architecture. This includes a setting to implement byte enable decoding for the big endian MPC860 format. The decoding is performed on the AN3042Q BE# lines. The configuration register may be loaded either at power-up from a PROM via the I2C interface or from the PCI system host. The value for the register is:

LBUSCFG = 0x0B50

The value given for the LBUSCFG is the default setting for the AN3042Q. Therefore, if no other power-up loading via the I2C interface PROM is needed, then the configuration PROM may be eliminated.

Timing

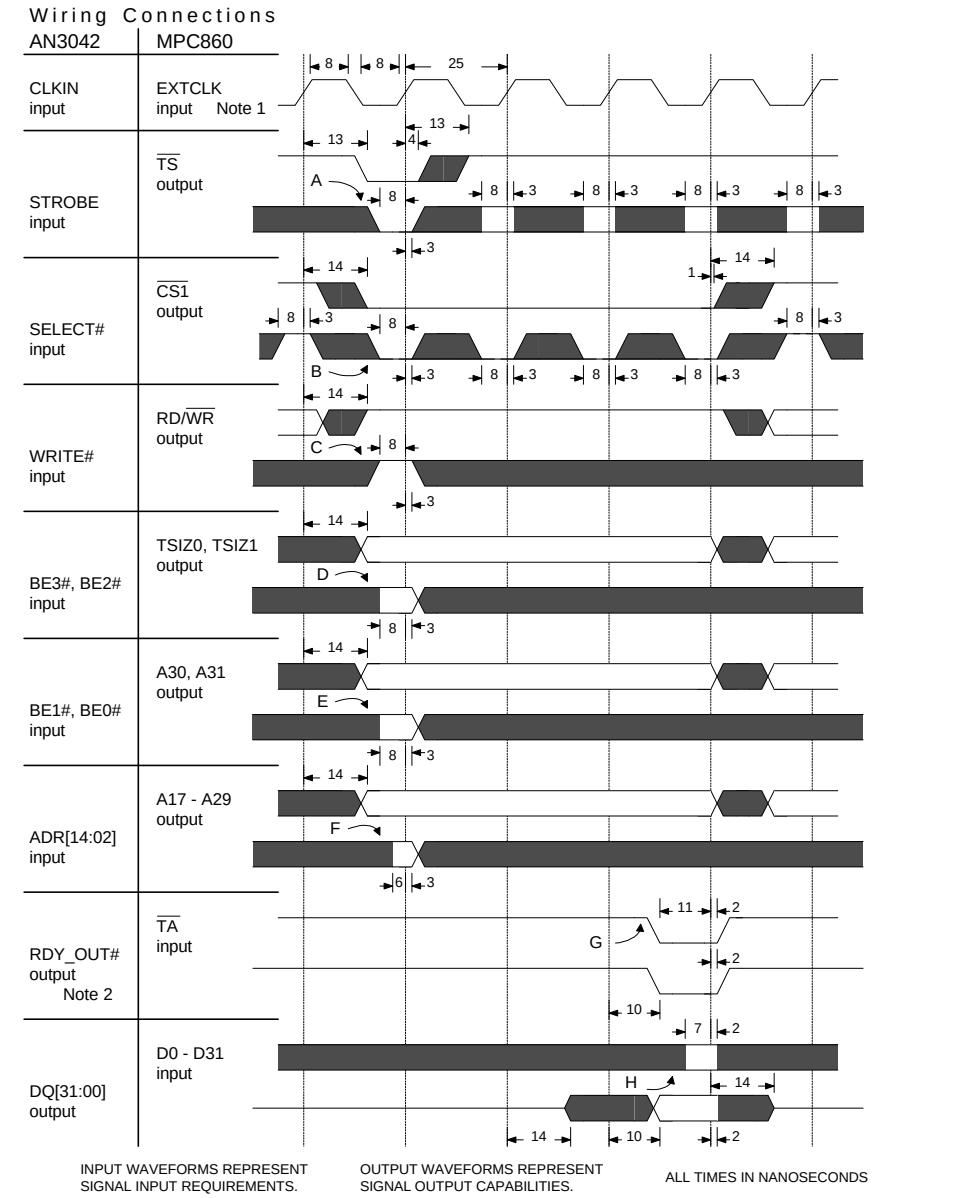
This section includes timing diagrams for the processor bus interface between the MPC860 and the AN3042Q. The interface is based on a 40 MHz MPC860 component.

The timing diagrams show waveforms organized in pairs. One member of the pair is the signal name of the AN3042Q and the other member is signal name of the MPC860. As shown in the Wiring Diagram, these signals are directly wired together. The intention of the timing diagrams is to show that the two components have compatible timing. The waveforms for the output signals illustrate the signals' characteristics and the waveforms for the input signals illustrate the signals' input requirements. In this way, both component specifications can be viewed together. After the diagrams, a summary of timing margin for each signal pair is provided.

Explanation and key to reading timing diagrams --

- Timing data are taken from the MPC860 and AN3042Q specifications; see References.
- Timing numbers are in nanoseconds and worst case commercial environment.
- Clock pulse widths and clock cycle time are minimum values.
- Where relevant, maximum data valid output timing is shown to support setup calculations.
- Output waveform timing represents signal output characteristics and capabilities.
- Where relevant, minimum data input setup timing is shown to support setup calculations.
- Input waveform timing represents signal input requirements.

The following is the timing diagram for MPC860 read access to the AN3042Q.



NOTES --

1 MPC860 bus interface timing is related to its CLKOUT signal output. A phase lock loop within the MPC860 keeps the phase skew between its EXTCLK input and CLKOUT output at +- 0.9 nsec. That value is factored into this timing diagram. The minimum high and low times for the AN3042Q CLKIN input are shown.

2 Wait states occur when the AN3042Q delays assertion of RDY_OUT# to later cycles. Zero wait states are illustrated here.

LETTERS A through H are references for the timing margin summary list. See text in Timing section.

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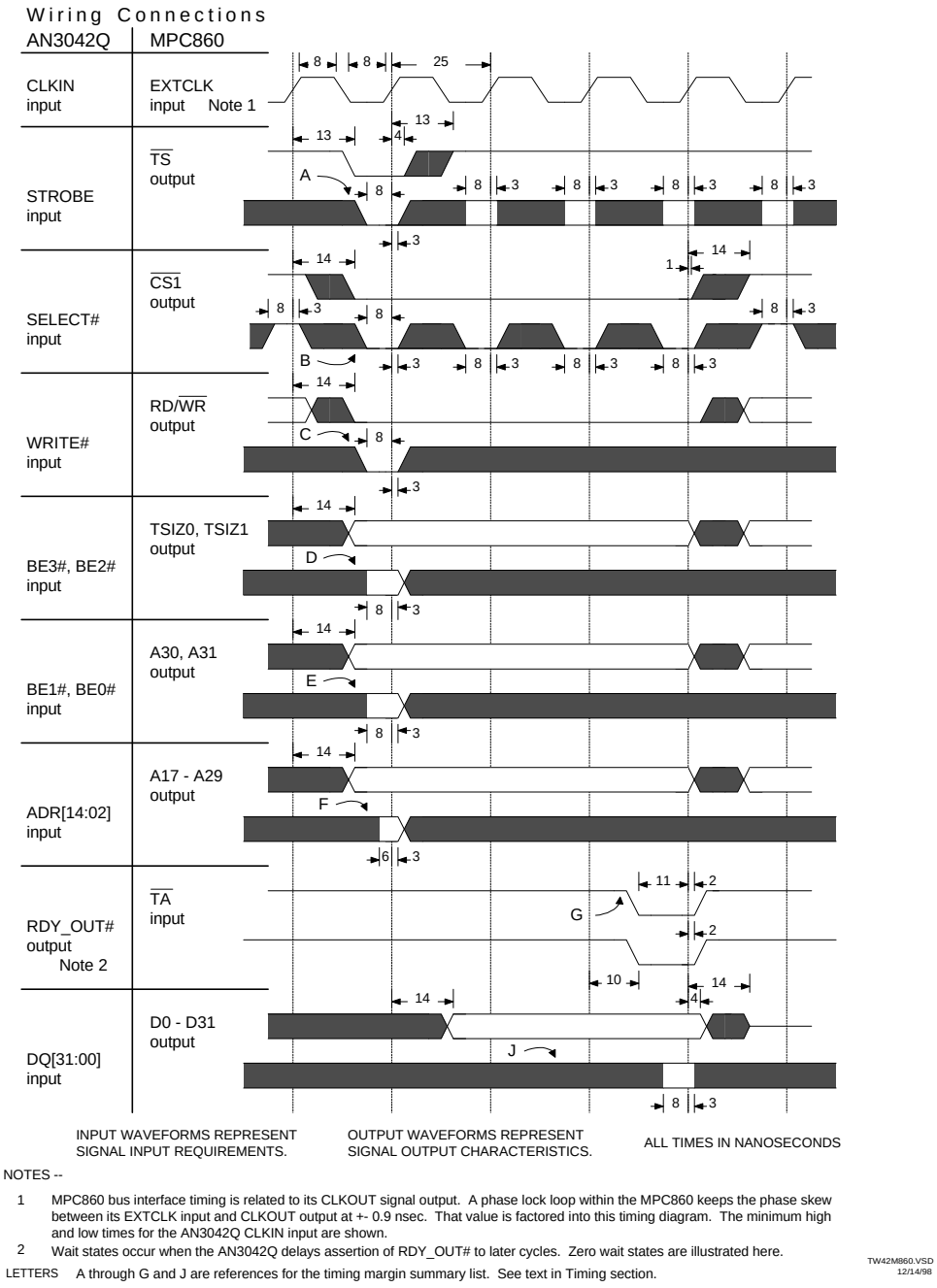
The following is the timing diagram for MPC860 write access to the AN3042Q.



From the two diagrams, timing margin for a MPC860 to AN3042 bus interconnect can be extracted. The timing shown is worst case commercial environment. Loading beyond the specification, signal line lengths, and other environmental constraints beyond commercial worst case can use this margin and maintain a compatible interface. Identifying letters are shown on the two timing diagrams.

Read and Write Access to the AN3042

A	AN3042 STROBE input setup	4 nsec
B	AN3042 SELECT# input setup	3 nsec
C	AN3042 WRITE# input setup	3 nsec
D	AN3042 BE3#, BE2# input setup	3 nsec
E	AN3042 BE1#, BE0# input setup	3 nsec
F	AN3042 ADR[14:02] input setup	5 nsec

G	MPC860 TA# input setup	4 nsec
Data Bus for Read Access to the AN3042		
H	MPC860 D0-D31 input setup	8 nsec
Data Bus for Write Access to the AN3042		
J	AN3042 DQ[31:00] input setup	53 nsec (output stable across cycles)

Performance

Throughput between the MPC860 and the shared memory of the AN3042Q is 32 MB/sec. Access to the AN3042Q Operation Registers or FIFO may incur wait states during concurrent accesses by the PCI bus.

AN3042Q mastered DMA bursting from the AN3042Q shared memory to system host memory has been measured to be approximately 120MB/sec on an unloaded PCI bus. Anchor Chips Incorporated has application notes concerning DMA operation and PCI bursting that can provide more insight into AN3042Q performance for particular environments.

References

Specifications used by this application note are listed below.

CO-MEM Lite, AN3042Q Integrated Circuit Technical Reference Manual, Version 1.1, October 19, 1998, Anchor Chips Incorporated.
MPC860 PowerQUICC User's Guide, Revision 1, July 1998, MPC860UM/AD, Motorola, Incorporated.
Errata to MPC860 PowerQUICC User's Guide Rev 1, September 30, 1998, Motorola, Incorporated.
MPC860 Rev 1.1 Specification, Section 21 MPC Electrical Characteristics, Motorola Semiconductor Products Sector.

Additional component literature may be downloaded from web sites at Anchor Chips Incorporated and Motorola Incorporated. The two main sites are listed below.

Anchor Chips PCI Developer's Home	http://www.anchorchips.com/pcidev/
Motorola Netcomm Publications	http://www.mot.com/SPS/RISC/netcomm/docs/pubs/

The PCI 2.1 specification may be purchased from the PCI Special Interest Group (SIG) or other sources. The web site for the PCI SIG is:

PCI SIG Home Page	http://www.pcisig.com/

Some related Anchor Chips Incorporated application notes are listed below. These documents may be downloaded from the Anchor Chips PCI Developer's Home.

How to doDMA
PCI Bus Mastering for System Performance