

2SC4112

2018A

NPN/PNP Epitaxial Planar Silicon Transistors

2SA1581

Switching Applications (with Bias Resistance)

(CP)

Applications

- Switching circuit, inverter circuit, interface circuit, driver circuit

Features

- On-chip bias resistance ($R_1=2.2\text{kohms}$, $R_2=\infty$)
- Small-sized package (CP)

(): 2SA1581

Absolute Maximum Ratings at $T_a=25^\circ\text{C}$

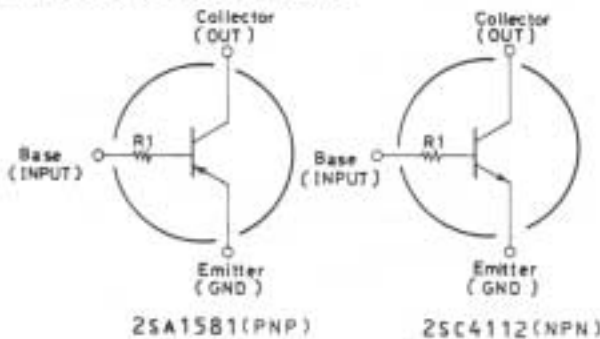
			unit
Collector to Base Voltage	V_{CBO}	(-)50	V
Collector to Emitter Voltage	V_{CEO}	(-)50	V
Emitter to Base Voltage	V_{EBO}	(-)5	V
Collector Current	I_C	(-)100	mA
Peak Collector Current	i_{cp}	(-)200	mA
Collector Dissipation	P_C	200	mW
Junction Temperature	T_j	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Electrical Characteristics at $T_a=25^\circ\text{C}$

			min	typ	max	unit
Collector Cutoff Current	I_{CBO}	$V_{CB}=(-)40\text{V}, I_E=0$			(-)0.1	μA
Emitter Cutoff Current	I_{EBO}	$V_{EB}=(-)5\text{V}, I_C=0$			(-)0.1	μA
DC Current Gain	h_{FE}	$V_{CE}=(-)5\text{V}, I_C=(-)10\text{mA}$	100			
Gain-Bandwidth Product	f_T	$V_{CE}=(-)10\text{V}, I_C=(-)5\text{mA}$		250 (200)		MHz
Output Capacitance	C_{ob}	$V_{CB}=(-)10\text{V}, f=1\text{MHz}$		3.5 (5.3)		pF
C-E Saturation Voltage	$V_{CE(sat)}$	$I_C=(-)10\text{mA}, I_B=(-)0.5\text{mA}$		(-)0.1	(-)0.3	V
C-B Breakdown Voltage	$V_{(BR)CBO}$	$I_C=(-)10\mu\text{A}, I_E=0$	(-)50			V
C-E Breakdown Voltage	$V_{(BR)CEO}$	$I_C=(-)100\mu\text{A}, R_{BE}=\infty$	(-)50			V
Input OFF-State Voltage	$V_{I(off)}$	$V_{CE}=(-)5\text{V}, I_C=(-)100\mu\text{A}$	(-)0.4	(-)0.55	(-)0.8	V
Input ON-State Voltage	$V_{I(on)}$	$V_{CE}=(-)0.2\text{V}, I_C=(-)10\text{mA}$	(-)0.6	(-)0.8	(-)1.5	V
Input Resistance	R_1		1.5	2.2	2.9	kohm

Marking on device 2SA1581:VL, 2SC4112:DT

Electrical Connection



Case Outline 2018A

(unit:mm)

