WT8811/WT8811S

Specification

Ver 0.92

09/09/2003

1. Features

Analog RGB Input Support

- Support up to 140MSPS cover rate (SXGA @75HZ) for WT8811S
- Support up to 110MSPS cover rate (XGA @75HZ) for WT8811
- 0.5V to 1.0V analog input range
- Support Midscale clamping for HDTV applciation
- Support Sync-On-Green (SOG) and composite sync modes

Digital Input Support

- 8bit YUV 4:2:2 Video input support
- Built-in YUV to RGB color space converter

High Quality Scaling Engine

- Fully programmable zoom ratios
- Independent Horizontal/Vertical scale
- High quality scalering down capability
- Advanced de-interlacing algorithm for digital YUV video
- Enhanced sharpness filter for better text support
- Spatial color dithering algorithm (random mode or fuzzy mode) to 16.7 million color
- Digital Brightness/Contrast adjustment
- Support horizontal non-linear scaling for 4:3 images display on 16:9 TFT panel.

Output Panel Support

- Single (18/24) or Dual (36/48) pixel output
- Support Multiple TFT LCD Panel
- Support VGA/SVGA/XGA/SXGA display resolution
- Support Panel output data R/B swap.
- Support Spread-Spectrum for reduced EMI

Build-in Programmable Panel Timing Controller (TCON)

- Direct connect to commercial row/column driver IC
- Support dual bus dual port, single bus single/dual port configurations
- Independent data swapping of even/odd pixels, red and blue pixels, and MSB and LSB

RSDS Display Interface

- Single (18/24) or Dual (36/48) pixel output
- Support RSDS differential output N/P swap.

OSD and Gamma Correction Support

- Fully programmable OSD Engine
- Downloadable font storage for internal OSD
- Support 384 plus 128 Multi-Color fonts
- User programmable 10-bit Gamma table
- Support sRGB for color management

On-chip Micro-controller

- Requires no external micro-controller
- 32 general purpose inputs/outputs (GPIO) available
- Build in 64k flash memory for program and 32k flash memory for OSD font
- In System Programming (ISP)
- Watch dog timer.
- Input X'tal frequency from 14.318MHz to 27MHz

Display Synchronization

- Advanced Input mode detection
- Automatic Input Edge Adjustment
- Automatic Input Phase Calibration

Low System Cost Solution

- Plug and Display, support VGA mode up to 1280x1024 @ 75Hz
- 2-wire I^2C serial interface for EEPROM and Micro-controller
- Glue less interface to external TMDS chip
- Power Management support

Electrical/Physical Specification

- 3.3V pad power supply with 5V I/O tolerant, 2.5V core power supply
- 208 pin PQFP Package

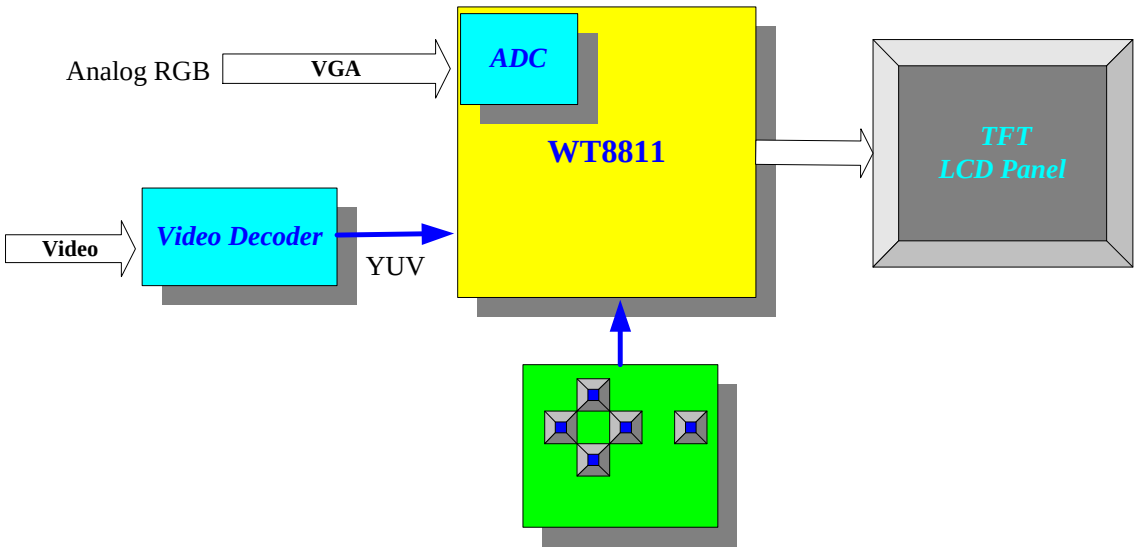
2. Overview

The WT8811 LCD (Liquid Crystal Display) Monitor Controller is an input format converter for the TFT-LCD Panels or LCD-TV applications. It accepts analog RGB signals from PC, YUV from digital video decoder or digital RGB graphics from PanelLink TMDS receiver and transforms these signals to TFT-LCD panel to display. The WT8811 performs image scaling on 24bit RGB or YUV data stream and feeds these scaled pixels to the output LCD panel. When displaying the image, instead of using external memory chips for scaling and temporary storage, the chip is using embedded line buffers. This chip also embedded MCU and flash memory such that the total system cost can be kept to minimum.

In order to provide the plug-n-display, the chip also performs functions like automatic input mode detection and automatic phase calibration. This is designed to keep the sampling clock of ADC is synchronized with the incoming data so that the final image in the LCD panel is free of distortion. The chip also provides the circuitry for contrast / brightness adjustment and gamma tables for intensity correction.

Figure 1 shows a system configuration for the chip.

WT8811 System Block Diagram



3. Signal Definitions

3.1 Pin Listing & Description

Symbol	Pin No	I/O	Description
PAD_RST	1	I	System Reset Signal (Active Low)
GPIO29	2	I/O	General Purpose Input/Output Bit 29
GPIO30	3	I/O	General Purpose Input/Output Bit 30
GPIO31	4	I/O	General Purpose Input/Output Bit 31
NC	5		N.C.
NC	6		N.C.
NC	7		N.C.
NC	8		N.C.
NC	9		N.C.
NC	10		N.C.
NC	11		N.C.
NC	12		N.C.
NC	13		N.C.
NC	14		N.C.
NC	15		N.C.
NC	16		N.C.
NC	17		N.C.
NC	18		N.C.
NC	19		N.C.
NC	20		N.C.
NC	21		N.C.
GND.dg	22	G	Ground for Digital Guard-ring
VDD.dg	23	P	Power for Digital Guard-ring
VDD.ag	24	P	Power for Analog Guard-ring
GND.ag	25	G	Ground for Analog Guard-ring
AVDD	26	P	ADC 2.5V Power Supply
AVSS	27	G	ADC Ground
AVDD	28	P	ADC 2.5V Power Supply
AVSS	29	G	ADC Ground
RAIN	30	I	Analog Input for Red Channel
AVSS	31	G	ADC Ground
AVDD	32	P	ADC 2.5V Power Supply
AVSS	33	G	ADC Ground
SOGIN	34	I	Input for Sync-on-Green
GAIN	35	I	Analog Input for Green Channel
AVSS	36	G	ADC Ground
AVDD	37	P	ADC 2.5V Power Supply
AVSS	38	G	ADC Ground
MID	39		Internal Midscale Voltage Bypass
Vref	40		Internal Reference Bypass
AVSS	41	G	ADC Ground
AVDD	42	P	ADC 2.5V Power Supply
AVDD	43	P	ADC 2.5V Power Supply

AVSS	44	G	ADC Ground
NC	45		N.C.
BAIN	46	I	Analog Input for Blue Channel
AVSS	47	G	ADC Ground
AVDD	48	P	ADC 2.5V Power Supply
AVSS	49	G	ADC Ground
APVDD	50	P	ADC 2.5V PLL Power Supply
XTAL	51	I	X'tal Osc Input (14.318MHZ ~ 27MHZ)
APVSS	52	G	ADC PLL Ground
APVDD	53	P	ADC 2.5V PLL Power Supply
CKEXT	54	I	External Clock Input
PVSS	55	G	PLL Ground
PVDD	56	P	PLL 2.5V Power
PVSS	57	G	PLL Ground
PVDD	58	P	PLL 2.5V Power
FILTVCO2	59		External Filter connection for VCO2
FILTVCO1	60		External Filter connection for VCO1
AGnd	61	G	System Analog Ground
AVdd	62	P	System Analog 2.5V Power Supply
DGnd	63	G	System Analog Ground
DVdd	64	P	System Analog 2.5V Power Supply
HSYNC	65	I	Horizontal Sync Input
VSYNC	66	I	Vertical Sync Input
V25	67	P	System 2.5V Power Supply
VSS	68	G	System Ground
GPIO0/ SYNC0	69	I	General Purpose Input/Output Bit 0/ Reference Fig.1 ~ Fig.7
GPIO1/ SYNC1	70	I	General Purpose Input/Output Bit 1/ Reference Fig.1 ~ Fig.7
GPIO2/ SYNC2	71	I	General Purpose Input/Output Bit 2/ Reference Fig.1 ~ Fig.7
GPIO3/ SYNC3	72	I	General Purpose Input/Output Bit 3/ Reference Fig.1 ~ Fig.7
GPIO4/ SYNC4	73	I	General Purpose Input/Output Bit 4/ Reference Fig.1 ~ Fig.7
GPIO5/ SYNC5	74	I	General Purpose Input/Output Bit 5/ Reference Fig.1 ~ Fig.7
GPIO6/ SYNC6	75	I	General Purpose Input/Output Bit 6/ Reference Fig.1 ~ Fig.7
GPIO7/ SYNC7	76	I	General Purpose Input/Output Bit 7/ Reference Fig.1 ~ Fig.7
Video_in0	77	I	Digital Video Format Input Bit0
Video_in1	78	I	Digital Video Format Input Bit1
Video_in2	79	I	Digital Video Format Input Bit2
Video_in3	80	I	Digital Video Format Input Bit3
Video_in4	81	I	Digital Video Format Input Bit4
Video_in5	82	I	Digital Video Format Input Bit5
Video_in6	83	I	Digital Video Format Input Bit6
Video_in7	84	I	Digital Video Format Input Bit7
TCON15	85	O	Timing Controller Output Bit 15
TCON14	86	O	Timing Controller Output Bit 14

TCON13	87	O	Timing Controller Output Bit 13
TCON12	88	O	Timing Controller Output Bit 12
TCON11	89	O	Timing Controller Output Bit 11
TCON10	90	O	Timing Controller Output Bit 10
TCON9	91	O	Timing Controller Output Bit 9
TCON8	92	O	Timing Controller Output Bit 8
VD33	93	P	System 3.3V Power Supply
TCON7	94	O	Timing Controller Output Bit 7
TCON6	95	O	Timing Controller Output Bit 6
TCON5	96	O	Timing Controller Output Bit 5
TCON4	97	O	Timing Controller Output Bit 4
TCON3	98	O	Timing Controller Output Bit 3
TCON2	99	O	Timing Controller Output Bit 2
TCON1	100	O	Timing Controller Output Bit 1
TCON0	101	O	Timing Controller Output Bit 0
VD33	102	P	System 3.3V Power Supply
VSS	103	G	System Ground
GPIO21/ PWM0	104	I/O	General Purpose Input/Output Bit 21 Pulse Width Modulation Output 0
GPIO22/ PWM1	105	I/O	General Purpose Input/Output Bit 22 Pulse Width Modulation Output 1
GPIO23/ PWM2	106	I/O	General Purpose Input/Output Bit 23 Pulse Width Modulation Output 2
GPIO24/ PWM3	107	I/O	General Purpose Input/Output Bit 24 Pulse Width Modulation Output 3
GPIO25/ RS232_TXD/ I2C_SCL	108	I/O	General Purpose Input/Output Bit 25/ RS232 TXD/ I2C SCL Signal
GPIO26/ RS232_RXD/ I2C_SDA	109	I/O	General Purpose Input/Output Bit 26/ RS232 RXD/ I2C SDA Signal
V25	110	P	System 2.5V Power Supply
VSS	111	G	System Ground
VSS	112	G	System Ground
VD33	113	P	System 3.3V Power Supply
GPIO27	114	I/O	General Purpose Input/Output Bit 27
GPIO28	115	I/O	General Purpose Input/Output Bit 28
VD33	116	P	System 3.3V Power
PANEL_R0/ R0P	117	O	Panel Red Output Data Bit 0/ Positive RSDS Differential Data from R0
PANEL_R1/ R0N	118	O	Panel Red Output Data Bit 1/ Negative RSDS Differential Data from R0
PANEL_R2/ R1P	119	O	Panel Red Output Data Bit 2 / Positive RSDS Differential Data from R1
PANEL_R3/ R1N	120	O	Panel Red Output Data Bit 3/ Negative RSDS Differential Data from R1
PANEL_R4/ R2P	121	O	Panel Red Output Data Bit 4/ Positive RSDS Differential Data from R2
PANEL_R5/ R2N	122	O	Panel Red Output Data Bit 5/ Negative RSDS Differential Data from R2
PANEL_R6/	123	O	Panel Red Output Data Bit 6/

R3P			Positive RSDS Differential Data from R3
PANEL_R7/ R3N	124	O	Panel Red Output Data Bit 7/ Negative RSDS Differential Data from R3
VSS	125	G	System Ground
VD33	126	P	System 3.3V Power Supply
PANEL_G0/ G0P	127	O	Panel Green Output Data Bit 0/ Positive RSDS Differential Data from G0
PANEL_G1/ G0N	128	O	Panel Green Output Data Bit 1/ Negative RSDS Differential Data from G0
PANEL_G2/ G1P	129	O	Panel Green Output Data Bit 2/ Positive RSDS Differential Data from G1
PANEL_G3/ G1N	130	O	Panel Green Output Data Bit 3/ Negative RSDS Differential Data from G1
PANEL_G4/ G2P	131	O	Panel Green Output Data Bit 4/ Positive RSDS Differential Data from G2
PANEL_G5/ G2N	132	O	Panel Green Output Data Bit 5/ Negative RSDS Differential Data from G2
PANEL_G6/ G3P	133	O	Panel Green Output Data Bit 6/ Positive RSDS Differential Data from G3
PANEL_G7/ G3N	134	O	Panel Green Output Data Bit 7/ Negative RSDS Differential Data from G3
VSS	135	G	System Ground
VD33	136	P	System 3.3V Power Supply
PANEL_B0/ B0P	137	O	Panel Blue Output Data Bit 0/ Positive RSDS Differential Data from B0
PANEL_B1/ B0N	138	O	Panel Blue Output Data Bit 1/ Negative RSDS Differential Data from B0
PANEL_B2/ B1P	139	O	Panel Blue Output Data Bit 2/ Positive RSDS Differential Data from B1
PANEL_B3/ B1N	140	O	Panel Blue Output Data Bit 3/ Negative RSDS Differential Data from B1
PANEL_B4/ B2P	141	O	Panel Blue Output Data Bit 4/ Positive RSDS Differential Data from B2
PANEL_B5/ B2N	142	O	Panel Blue Output Data Bit 5/ Negative RSDS Differential Data from B2
PANEL_B6/ B3P	143	O	Panel Blue Output Data Bit 6/ Positive RSDS Differential Data from B3
PANEL_B7/ B3N	144	O	Panel Blue Output Data Bit 7/ Negative RSDS Differential Data from B3
VSS	145	G	System Ground
VD33	146	P	System 3.3V Power Supply
PDE/ PCK0P	147	O	Panel Data Enable/ Positive RSDS Differential Data from PCK0
PVS/ PCK0N	148	O	Panel Vertical Sync/ Negative RSDS Differential Data from PCK0
VSS	149	G	System Ground
VSS	150	G	System Ground
Vr	151		RSDS Reference Bias
V25	152	P	System 2.5V Power Supply
PHS/ PCK1P	153	O	Panel Horizontal Sync/ Positive RSDS Differential Data from PCK1

PCK/ PCK1N	154	O	Panel Clock/ Negative RSDS Differential Data from PCK1
V25	155	P	System 2.5V Power Supply
VSS	156	G	System Ground
VD33	157	P	System 3.3V Power Supply
PANEL_R8/ R4P	158	O	Panel Red Output Data Bit 8/ Positive RSDS Differential Data from R4
PANEL_R9/ R4N	159	O	Panel Red Output Data Bit 9/ Negative RSDS Differential Data from R4
PANEL_R10/ R5P	160	O	Panel Red Output Data Bit 10/ Positive RSDS Differential Data from R5
PANEL_R11/ R5N	161	O	Panel Red Output Data Bit 11/ Negative RSDS Differential Data from R5
PANEL_R12/ R6P	162	O	Panel Red Output Data Bit 12/ Positive RSDS Differential Data from R6
PANEL_R13/ R6N	163	O	Panel Red Output Data Bit 13/ Negative RSDS Differential Data from R6
PANEL_R14/ R7P	164	O	Panel Red Output Data Bit 14/ Positive RSDS Differential Data from R7
PANEL_R15/ R7N	165	O	Panel Red Output Data Bit 15/ Negative RSDS Differential Data from R7
VSS	166	G	System Ground
VD33	167	P	System 3.3V Power Supply
PANEL_G8/ G4P	168	O	Panel Green Output Data Bit 8/ Positive RSDS Differential Data from G4
PANEL_G9/ G4N	169	O	Panel Green Output Data Bit 9/ Negative RSDS Differential Data from G4
PANEL_G10/ G5P	170	O	Panel Green Output Data Bit 10/ Positive RSDS Differential Data from G5
PANEL_G11/ G5N	171	O	Panel Green Output Data Bit 11/ Negative RSDS Differential Data from G5
PANEL_G12/ G6P	172	O	Panel Green Output Data Bit 12/ Positive RSDS Differential Data from G6
PANEL_G13/ G6N	173	O	Panel Green Output Data Bit 13/ Negative RSDS Differential Data from G6
PANEL_G14/ G7P	174	O	Panel Green Output Data Bit 14/ Positive RSDS Differential Data from G7
PANEL_G15/ G7N	175	O	Panel Green Output Data Bit 15/ Negative RSDS Differential Data from G7
VSS	176	G	System Ground
VD33	177	P	System 3.3V Power Supply
PANEL_B8/ B4P	178	O	Panel Blue Output Data Bit 8/ Positive RSDS Differential Data from B4
PANEL_B9/ B4N	179	O	Panel Blue Output Data Bit 9/ Negative RSDS Differential Data from B4
PANEL_B10/ B5P	180	O	Panel Blue Output Data Bit 10/ Positive RSDS Differential Data from B5
PANEL_B11/ B5N	181	O	Panel Blue Output Data Bit 11/ Negative RSDS Differential Data from B5
PANEL_B12/ B6P	182	O	Panel Blue Output Data Bit 12/ Positive RSDS Differential Data from B6

PANEL_B13/ B6N	183	O	Panel Blue Output Data Bit 13/ Negative RSDS Differential Data from B6
PANEL_B14/ B7P	184	O	Panel Blue Output Data Bit 14/ Positive RSDS Differential Data from B7
PANEL_B15/ B7N	185	O	Panel Blue Output Data Bit 15/ Negative RSDS Differential Data from B7
VSS	186	G	System Ground
V25	187	P	System 2.5V Power Supply
VSS	188	G	System Ground
DDC_SCL/ RS232_TXD	189	I	DDC I2C Bus Clock Input, also as ISP I2C Bus Clock Input/ RS232 TXD
DDC_SDA/ RS232_RXD	190	I/O	DDC I2C Bus Data Output, also as ISP I2C Bus Data Input/Output/ RS232 RXD
CLK_I	191		For Testing
MODE0	192		For Testing
MODE1	193		For Testing
VSS	194	G	System Ground
VD33	195	P	System 3.3V Power Supply
GPIO16/ OSD_R	196	I/O	General Purpose Input/Output Bit 16/ External OSD Red Signal
GPIO17/ OSD_G	197	I/O	General Purpose Input/Output Bit 17/ External OSD Green Signal
GPIO18/ OSD_B	198	I/O	General Purpose Input/Output Bit 18/ External OSD Blue Signal
GPIO19/ OSD_I	199	I/O	General Purpose Input/Output Bit 19/ External OSD Intensity Signal
GPIO20/ OSD_FB	200	I/O	General Purpose Input/Output Bit 20/ Overlay Enable From External OSD Chip
GPIO8/ INT0	201	I/O	General Purpose Input/Output Bit 8/ External Interrupt INT1 [0]
GPIO9/ INT1	202	I/O	General Purpose Input/Output Bit 9/ External Interrupt INT1 [1]
GPIO10/ INT2	203	I/O	General Purpose Input/Output Bit 10/ External Interrupt INT1 [2]
GPIO11/ INT3	204	I/O	General Purpose Input/Output Bit 11/ External Interrupt INT1 [3]
GPIO12/ INT4	205	I/O	General Purpose Input/Output Bit 12/ External Interrupt INT1 [4]
GPIO13/ INT5	206	I/O	General Purpose Input/Output Bit 13/ External Interrupt INT1 [5]
GPIO14/ INT6	207	I/O	General Purpose Input/Output Bit 14/ External Interrupt INT1 [6]
GPIO15/ INT7	208	I/O	General Purpose Input/Output Bit 15/ External Interrupt INT1 [7]

Note: All input pins have internal pull down (100K)

3.2 Pin Diagram