

TC74AC109P, TC74AC109F, TC74AC109FN

DUAL J - \bar{K} FLIP FLOP WITH PRESET AND CLEAR

The TC74AC109 is an advanced high speed CMOS DUAL J- \bar{K} FLIP FLOP fabricated with silicon gate and double-layer metal wiring C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

In accordance with the logic level given J and \bar{K} input this device changes state on positive going transition of the clock pulse. $\overline{\text{CLEAR}}$ and $\overline{\text{PRESET}}$ are independent of the clock and accomplished by a low logic level on the corresponding input. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES :

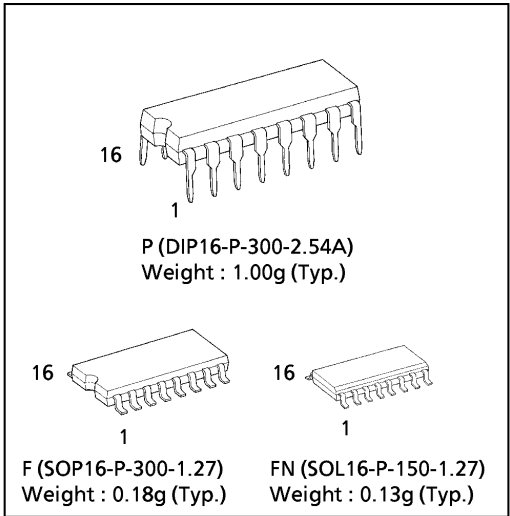
- High Speed..... $f_{\text{MAX}} = 200\text{MHz}$ (typ.)
at $V_{\text{CC}} = 5\text{V}$
- Low Power Dissipation..... $I_{\text{CC}} = 4\mu\text{A}(\text{Max.})$ at $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{\text{NIH}} = V_{\text{NIL}} = 28\% V_{\text{CC}}$ (Min.)
- Symmetrical Output Impedance... $|I_{\text{OH}}| = I_{\text{OL}} = 24\text{mA}(\text{Min.})$
Capability of driving 50 Ω transmission lines.
- Balanced Propagation Delays..... $t_{\text{PLH}} \approx t_{\text{PHL}}$
- Wide Operating Voltage Range... $V_{\text{CC}}(\text{opr}) = 2\text{V} \sim 5.5\text{V}$
- Pin and Function Compatible with 74F109

TRUTH TABLE

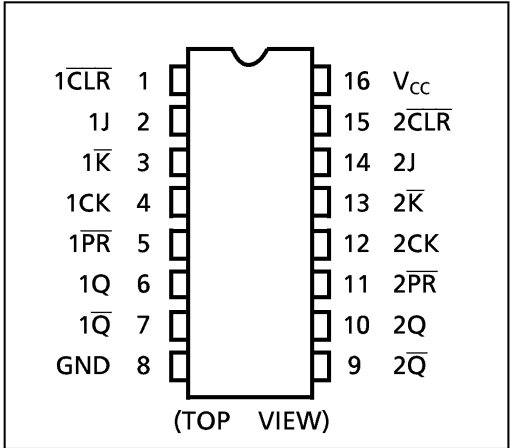
| INPUTS | | | | | OUTPUTS | | FUNCTION |
|--------|----|---|-----------|--------------|-------------|-------------|-----------|
| CLR | PR | J | \bar{K} | CK | Q | \bar{Q} | |
| L | H | X | X | X | L | H | CLEAR |
| H | L | X | X | X | H | L | PRESET |
| L | L | X | X | X | H | H | |
| H | H | L | H | \uparrow | Q_n | \bar{Q}_n | NO CHANGE |
| H | H | L | L | \uparrow | L | H | |
| H | H | H | H | \uparrow | H | L | |
| H | H | H | L | \uparrow | \bar{Q}_n | Q_n | TOGGLE |
| H | H | X | X | \downarrow | Q_n | \bar{Q}_n | NO CHANGE |

X : Don't Care

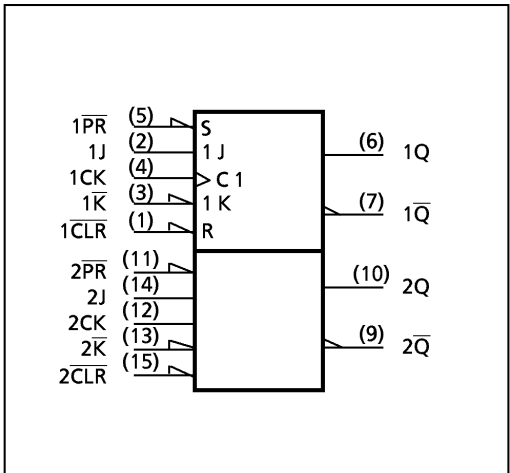
(Note) The JEDEC SOP (FN) is not available in Japan.



PIN ASSIGNMENT



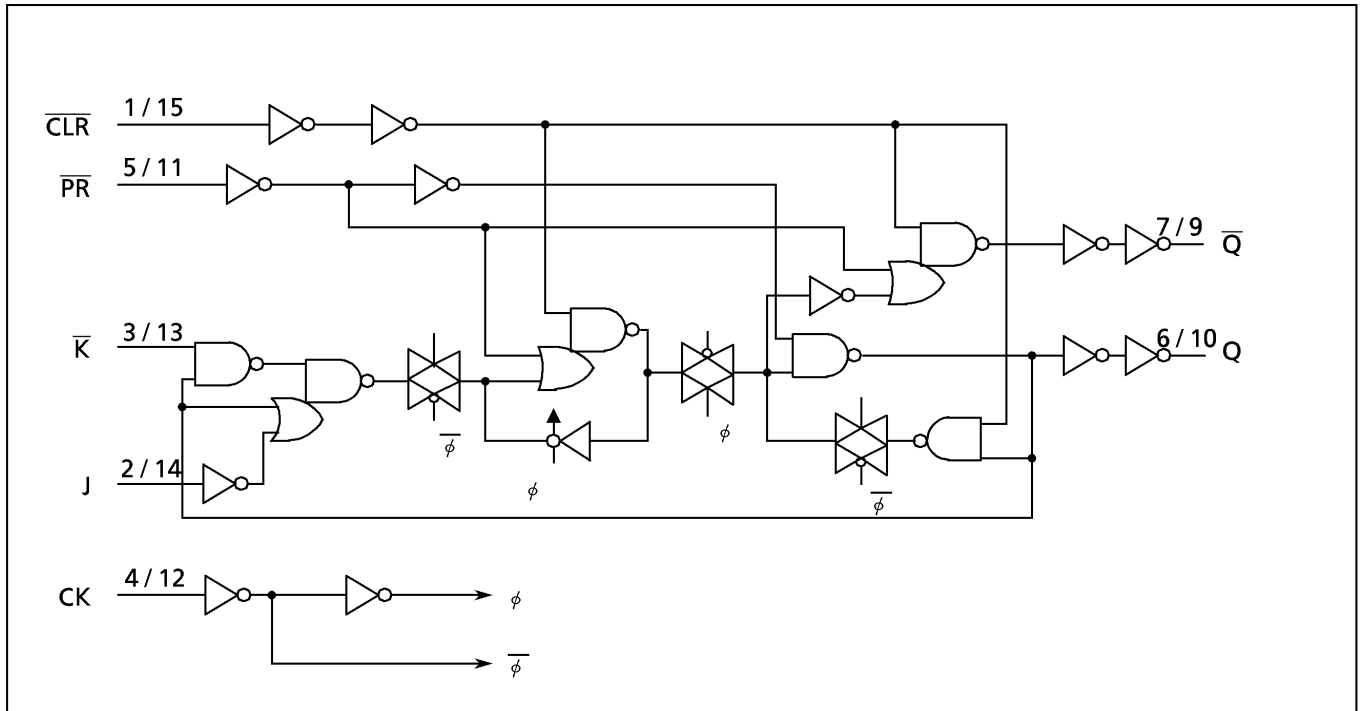
IEC LOGIC SYMBOL



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SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | VALUE | UNIT |
|-----------------------------|-----------|------------------------|-------------|
| Supply Voltage Range | V_{CC} | -0.5~7.0 | V |
| DC Input Voltage | V_{IN} | -0.5~ $V_{CC} + 0.5$ | V |
| DC Output Voltage | V_{OUT} | -0.5~ $V_{CC} + 0.5$ | V |
| Input Diode Current | I_{IK} | ± 20 | mA |
| Output Diode Current | I_{OK} | ± 50 | mA |
| DC Output Current | I_{OUT} | ± 50 | mA |
| DC V_{CC} /Ground Current | I_{CC} | ± 100 | mA |
| Power Dissipation | P_D | 500 (DIP)* / 180 (SOP) | mW |
| Storage Temperature | T_{stg} | -65~150 | $^{\circ}C$ |

*500mW in the range of $T_a = -40^{\circ}C \sim 65^{\circ}C$. From $T_a = 65^{\circ}C$ to $85^{\circ}C$ a derating factor of $-10mW/^{\circ}C$ should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | VALUE | UNIT |
|--------------------------|-----------|---|-------------|
| Supply Voltage | V_{CC} | 2.0~5.5 | V |
| Input Voltage | V_{IN} | 0~ V_{CC} | V |
| Output Voltage | V_{OUT} | 0~ V_{CC} | V |
| Operating Temperature | T_{opr} | -40~85 | $^{\circ}C$ |
| Input Rise and Fall Time | dt/dV | 0~100 ($V_{CC} = 3.3 \pm 0.3V$) 0~20 ($V_{CC} = 5 \pm 0.5V$) | ns/V |

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- The information contained herein is subject to change without notice.

DC ELECTRICAL CHARACTERISTICS

| PARAMETER | SYMBOL | TEST CONDITION | V _{CC} (V) | Ta = 25°C | | | Ta = -40~85°C | | UNIT | |
|--------------------------------|-----------------|---|--------------------------|----------------------|-------------|----------------------|----------------------|----------------------|------|---|
| | | | | MIN. | TYP. | MAX. | MIN. | MAX. | | |
| High - Level Input Voltage | V _{IH} | | 2.0 3.0 5.5 | 1.50 2.10 3.85 | — — — | — — — | 1.50 2.10 3.85 | — — — | V | |
| Low - Level Input Voltage | V _{IL} | | 2.0 3.0 5.5 | — — — | — — — | 0.50 0.90 1.65 | — — — | 0.50 0.90 1.65 | V | |
| High - Level Output Voltage | V _{OH} | V _{IN} = V _{IH} or V _{IL} | I _{OH} = -50μA | 2.0 | 1.9 | 2.0 | — | 1.9 | — | V |
| | | | | 3.0 | 2.9 | 3.0 | — | 2.9 | — | |
| | | | | 4.5 | 4.4 | 4.5 | — | 4.4 | — | |
| | | | | 3.0 | 2.58 | — | — | 2.48 | — | |
| | | | I _{OH} = -4mA | 4.5 | 3.94 | — | — | 3.80 | — | |
| | | | I _{OH} = -24mA | 5.5 | — | — | — | 3.85 | — | |
| | | | I _{OH} = -75mA* | | | | | | | |
| Low - Level Output Voltage | V _{OL} | V _{IN} = V _{IH} or V _{IL} | I _{OL} = 50μA | 2.0 | — | 0.0 | 0.1 | — | 0.1 | V |
| | | | | 3.0 | — | 0.0 | 0.1 | — | 0.1 | |
| | | | | 4.5 | — | 0.0 | 0.1 | — | 0.1 | |
| | | | | 3.0 | — | — | 0.36 | — | 0.44 | |
| | | | I _{OL} = 12mA | 4.5 | — | — | 0.36 | — | 0.44 | |
| | | | I _{OL} = 24mA | 5.5 | — | — | — | — | 1.65 | |
| | | | I _{OL} = 75mA* | | | | | | | |
| Input Leakage Current | I _{IN} | V _{IN} = V _{CC} or GND | 5.5 | — | — | ±0.1 | — | ±1.0 | μA | |
| Quiescent Supply Current | I _{CC} | V _{IN} = V _{CC} or GND | 5.5 | — | — | 4.0 | — | 40.0 | | |

* : This spec indicates the capability of driving 50Ω transmission lines.

One output should be tested at a time for a 10ms maximum duration.

TIMING REQUIREMENTS (Input t_r = t_f = 3ns)

| PARAMETER | SYMBOL | TEST CONDITION | Ta = 25°C | | Ta = -40~85°C | | UNIT |
|-----------------------------------|--|----------------|---------------------|-------|---------------|----|------|
| | | | V _{CC} (V) | LIMIT | LIMIT | | |
| Minimum Pulse Width (CK) | t _W (L) t _W (H) | | 3.3 ± 0.3 | 8.0 | 8.0 | ns | |
| | | | 5.0 ± 0.5 | 5.0 | 5.0 | | |
| Minimum Pulse Width (CLR, PR) | t _W (L) | | 3.3 ± 0.3 | 7.0 | 7.0 | | |
| | | | 5.0 ± 0.5 | 5.0 | 5.0 | | |
| Minimum Set - up Time | t _s | | 3.3 ± 0.3 | 9.0 | 9.0 | | |
| | | | 5.0 ± 0.5 | 5.0 | 5.0 | | |
| Minimum Hold Time | t _h | | 3.3 ± 0.3 | 0.0 | 0.0 | | |
| | | | 5.0 ± 0.5 | 0.0 | 0.0 | | |
| Minimum Removal Time (CLR, PR) | t _{rem} | | 3.3 ± 0.3 | 3.0 | 3.0 | | |
| | | | 5.0 ± 0.5 | 2.0 | 2.0 | | |

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, $R_L = 500\ \Omega$, Input $t_r = t_f = 3\text{ns}$)

| PARAMETER | SYMBOL | TEST CONDITION | Ta = 25°C | | | Ta = -40~85°C | | UNIT | |
|--|--------------------------------------|----------------|---------------------|------|------|---------------|------|------|------|
| | | | V _{CC} (V) | MIN. | TYP. | MAX. | MIN. | | MAX. |
| Propagation Delay Time (CK-Q, \bar{Q}) | t _{pLH} t _{pHL} | | 3.3 ± 0.3 | — | 8.2 | 13.9 | 1.0 | 16.0 | ns |
| | | | 5.0 ± 0.5 | — | 6.1 | 8.7 | 1.0 | 10.0 | |
| Propagation Delay Time ($\bar{\text{CLR}}$, $\bar{\text{PR}}$ -Q, \bar{Q}) | t _{pLH} t _{pHL} | | 3.3 ± 0.3 | — | 8.5 | 14.4 | 1.0 | 16.6 | ns |
| | | | 5.0 ± 0.5 | — | 6.4 | 9.1 | 1.0 | 10.5 | |
| Maximum Clock Frequency | f _{MAX} | | 3.3 ± 0.3 | 55 | 120 | — | 55 | — | MHz |
| | | | 5.0 ± 0.5 | 100 | 160 | — | 100 | — | |
| Input Capacitance | C _{IN} | | | — | 5 | 10 | — | 10 | pF |
| Power Dissipation Capacitance | C _{PD} (1) | | | — | 82 | — | — | — | |

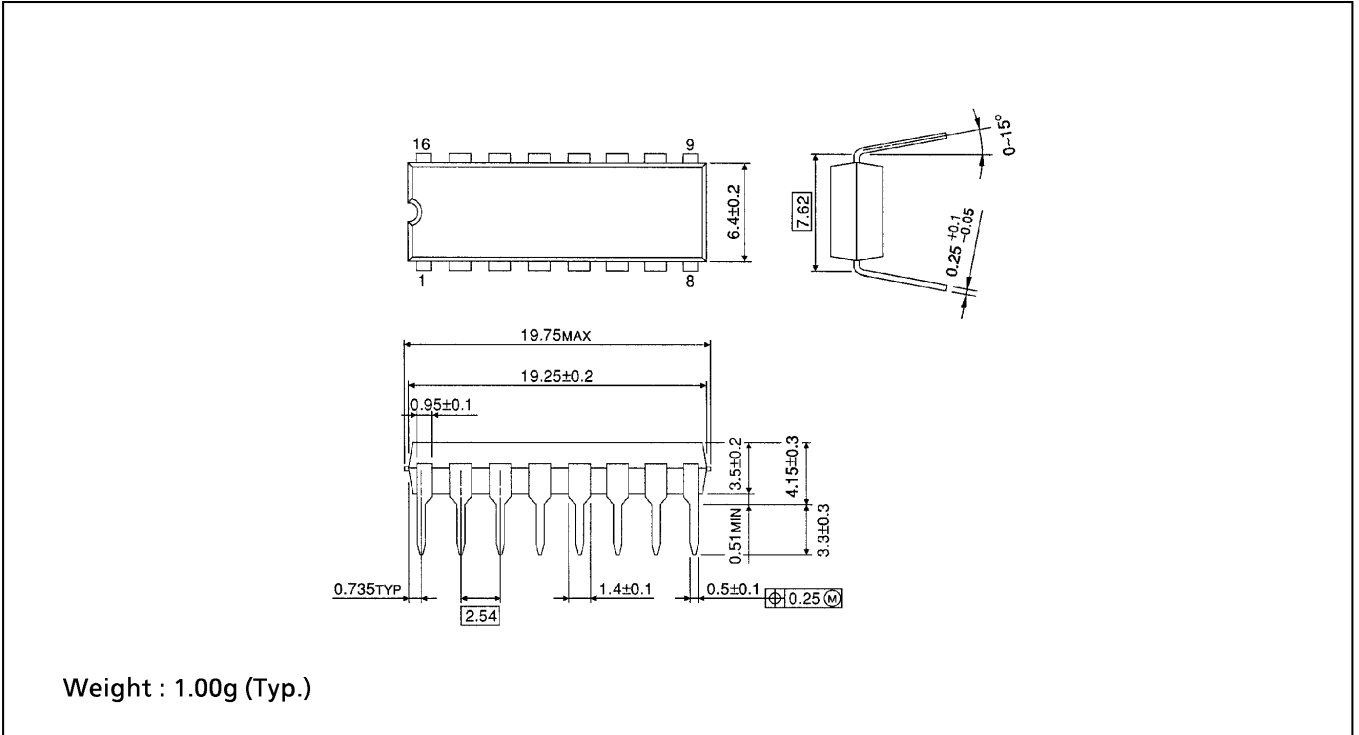
Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr.}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per F/F)}$$

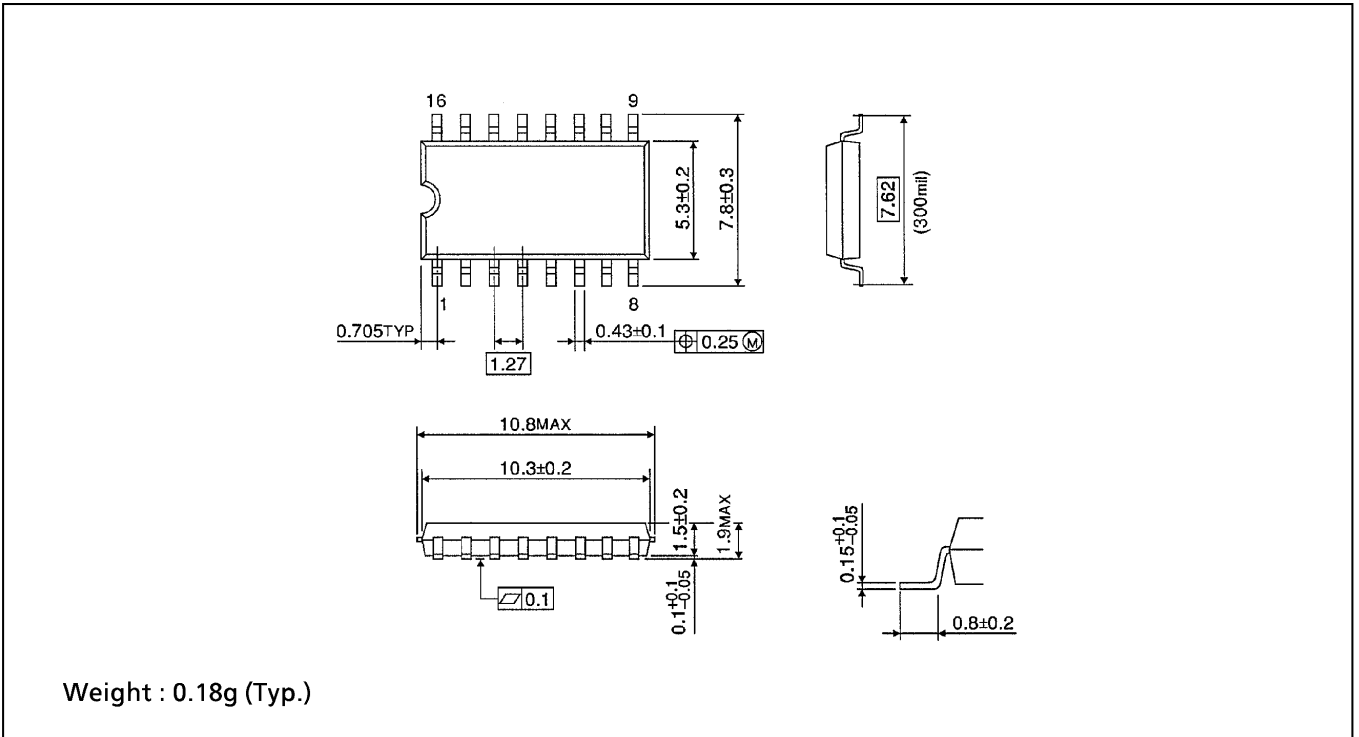
DIP 16PIN OUTLINE DRAWING (DIP16-P-300-2.54A)

Unit in mm



SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27)

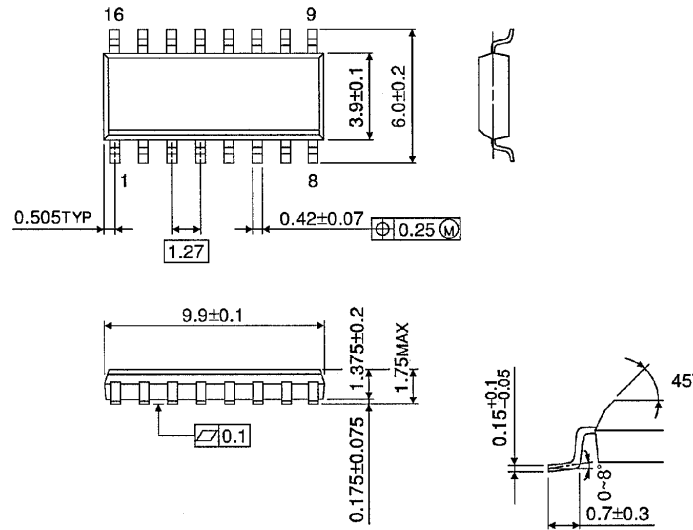
Unit in mm



SOP 16PIN (150mil BODY) OUTLINE DRAWING (SOL16-P-150 -1.27)

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)