

FEATURES

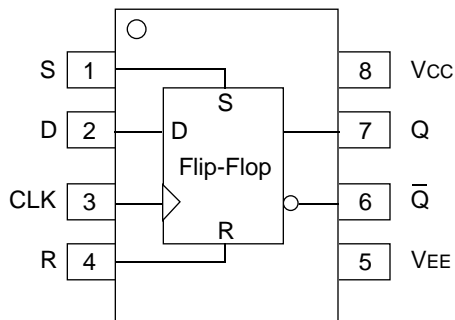
- 475ps propagation delay
- 2.8GHz toggle frequency
- Internal 75KΩ input pull-down resistors
- Available in 8-pin SOIC package

DESCRIPTION

The SY10/100EL31 are D flip-flops with set and reset. The devices are functionally equivalent to the E131 devices, with higher performance capabilities. With propagation delays and output transition times significantly faster than the E131, the EL31 is ideally suited for those applications which require the ultimate in AC performance.

Both the set and reset inputs are asynchronous, level triggered signals. Data enters the master portion of the flip-flop when the clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock.

PIN CONFIGURATION/BLOCK DIAGRAM



**SOIC
TOP VIEW**

PIN NAMES

Pin	Function
D	Data Inputs
Q	Data Outputs
S	Set
R	Reset
CLK	Clock Input

TRUTH TABLE⁽¹⁾

D	S	R	CLK	Q
L	L	L	Z	L
H	L	L	Z	H
X	H	L	X	H
X	L	H	X	L
X	H	H	X	Undef

NOTE:

1. Z = LOW-to-HIGH transition.

DC ELECTRICAL CHARACTERISTICS

VEE = VEE (Min.) to VEE (Max.); VCC = GND

Symbol	Parameter	TA = -40°C			TA = 0°C			TA = +25°C			TA = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
IEE	Power Supply Current													mA
	10EL	—	27	32	18	27	32	18	27	32	18	27	32	
	100EL	—	27	32	18	27	32	18	27	32	21	31	37	
VEE	Power Supply Voltage													V
	10EL	-4.75	-5.2	-5.5	-4.75	-5.2	-5.5	-4.75	-5.2	-5.5	-4.75	-5.2	-5.5	
	100EL	-4.20	-4.5	-5.5	-4.20	-4.5	-5.5	-4.20	-4.5	-5.5	-4.20	-4.5	-5.5	
I _{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	—	—	150	μA

AC ELECTRICAL CHARACTERISTICS

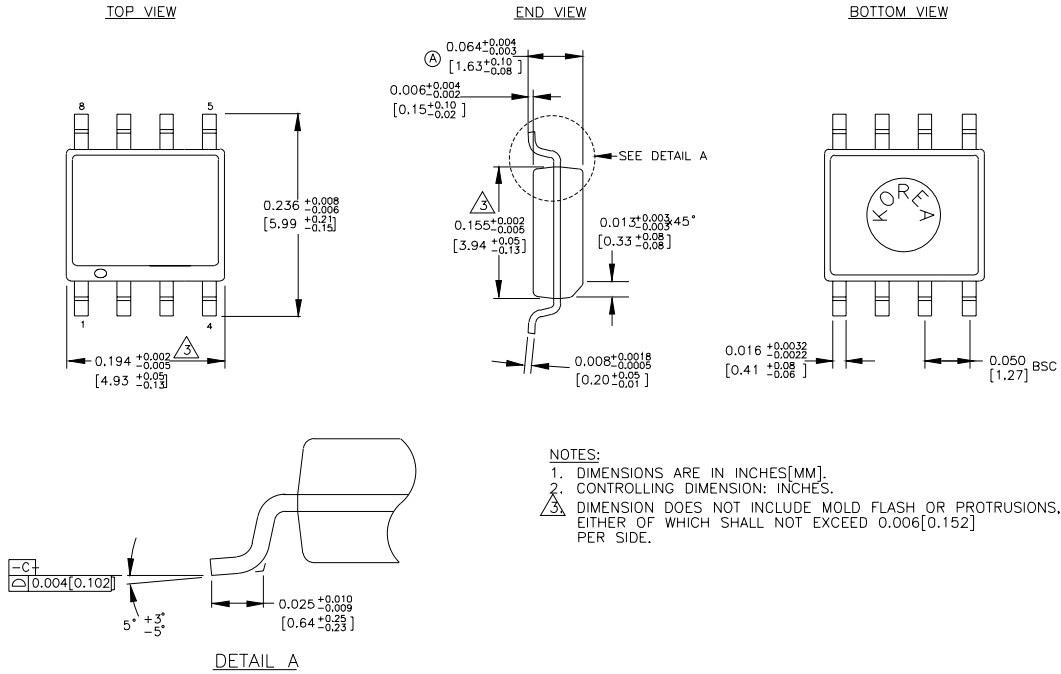
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		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
f _{MAX}	Maximum Toggle Frequency	20	2.5	—	2.2	2.8	—	2.2	2.8	—	2.2	2.8	—	GHz
t _{PLH} t _{PHL}	Propagation Delay to Output													ps
	CLK S, R	315 295	465 455	630 630	365 345	465 455	580 580	375 355	475 465	590 590	430 400	530 510	645 645	
t _S	Set-up Time	150	0	—	150	0	—	150	0	—	150	0	—	ps
t _H	Hold Time	250	100	—	250	100	—	250	100	—	250	100	—	ps
t _{RR}	Set/Reset Recovery	400	200	—	400	200	—	400	200	—	400	200	—	ps
t _{PW}	Minimum Pulse Width CLK, Set, Reset	400	—	—	400	—	—	400	—	—	400	—	—	ps
t _r t _f	Output Rise/Fall Times Q (20% to 80%)	100	225	350	100	225	350	100	225	350	100	225	350	ps

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10EL31ZC	Z8-1	Commercial
SY10EL31ZCTR	Z8-1	Commercial
SY100EL31ZC	Z8-1	Commercial
SY100EL31ZCTR	Z8-1	Commercial

8 LEAD SOIC .150" WIDE (Z8-1)



NOTES:
 1. DIMENSIONS ARE IN INCHES[MM].
 2. CONTROLLING DIMENSION: INCHES.
 3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.006[0.152] PER SIDE.

Rev. 03

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