

PHD24N03LT

N-channel enhancement mode field-effect transistor

Rev. 02 — 27 July 2000

Product specification

1. Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™¹ technology.

Product availability:

PHD24N03LT in SOT428 (D-PAK).

2. Features

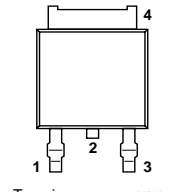
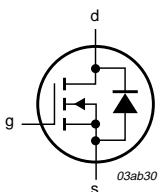
- TrenchMOS™ technology
- Low on-state resistance
- Avalanche ruggedness rated
- Logic level compatible
- Surface mount package.

3. Applications

- DC to DC converter
- High speed, low resistance switch

4. Pinning information

Table 1: Pinning - SOT428, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)	 <p>Top view MBK091 SOT428 (D-PAK)</p>	 <p>N-channel MOSFET 03ab30</p>
2	drain (d) [1]		
3	source (s)		
4	mounting base, connected to drain (d)		

[1] It is not possible to make connection to pin 2 of the SOT428 package.

1. TrenchMOS is a trademark of Royal Philips Electronics.

5. Quick reference data

Table 2: Quick reference data

Symbol	Parameter	Conditions	Typ	Max	Unit
V_{DS}	drain-source voltage (DC)	$T_j = 25$ to 175 °C	–	30	V
I_D	drain current (DC)	$T_{mb} = 25$ °C; $V_{GS} = 10$ V	–	20	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C	–	37.5	W
T_j	junction temperature		–	175	°C
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 10$ A	28	50	mΩ
		$V_{GS} = 5$ V; $I_D = 10$ A	38	56	mΩ

6. Limiting values

Table 3: Limiting values

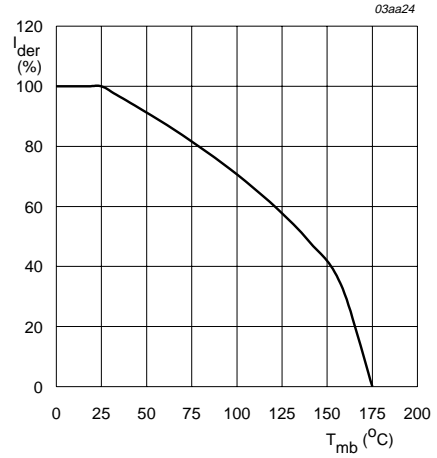
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$T_j = 25$ to 175 °C	–	30	V
V_{DGR}	drain-gate voltage (DC)	$T_j = 25$ to 175 °C; $R_{GS} = 20$ kΩ	–	30	V
V_{GS}	gate-source voltage (DC)		–	±15	V
V_{GSM}	peak gate-source voltage	$t_p \leq 50$ μs; pulsed; duty cycle = 25%	–	±20	V
I_D	drain current (DC)	$T_{mb} = 25$ °C; $V_{GS} = 10$ V; Figure 2 and 3	–	20	A
		$T_{mb} = 100$ °C; $V_{GS} = 10$ V; Figure 2	–	14	A
I_{DM}	peak drain current	$T_{mb} = 25$ °C; pulsed; $t_p \leq 10$ μs; Figure 3	–	80	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; Figure 1	–	37.5	W
T_{stg}	storage temperature		–55	+175	°C
T_j	operating junction temperature		–55	+175	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	$T_{mb} = 25$ °C	–	20	A
I_{SM}	peak source (diode forward) current	$T_{mb} = 25$ °C; pulsed; $t_p \leq 10$ μs	–	80	A
Avalanche ruggedness limiting values					
E_{AS}	non-repetitive avalanche energy	unclamped inductive load; $I_D = 19$ A; $t_p = 0.2$ ms; $V_{DD} \leq 15$ V; $R_{GS} = 50$ Ω; $V_{GS} = 5$ V; starting $T_j = 25$ °C; Figure 4	–	74	mJ
I_{AS}	non-repetitive avalanche current	unclamped inductive load; $V_{DD} \leq 15$ V; $R_{GS} = 50$ Ω; $V_{GS} = 5$ V; Figure 4	–	20	A



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

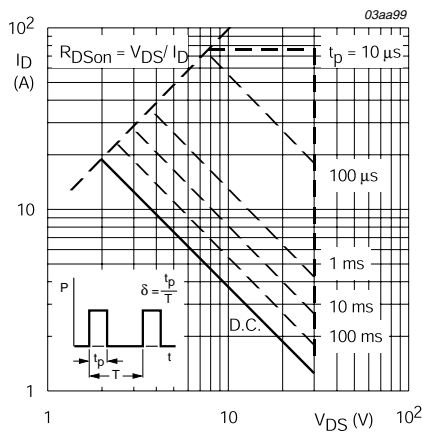
Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$V_{GS} \geq 5 \text{ V}$$

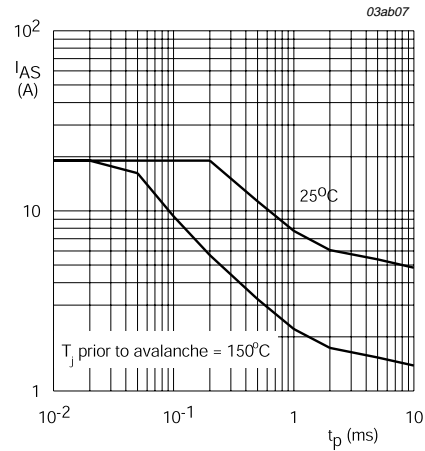
$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



$T_{mb} = 25^{\circ}C$; I_{DM} is single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.



Unclamped inductive load; $V_{DD} \leq 15 \text{ V}$; $R_{GS} = 50 \Omega$; $V_{GS} = 5 \text{ V}$; starting $T_j = 25^{\circ}C$ and $150^{\circ}C$.

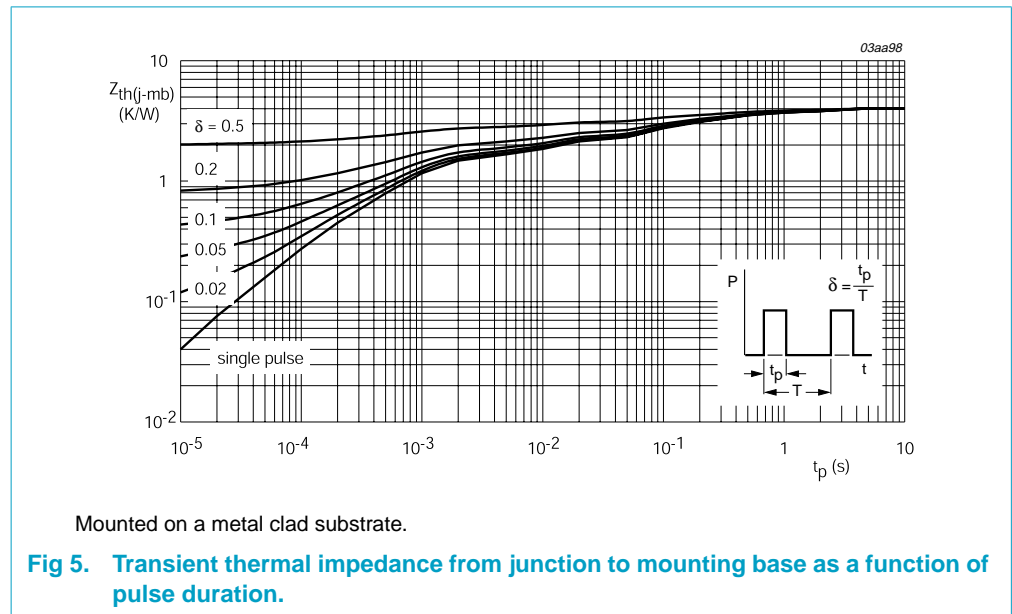
Fig 4. Non-repetitive avalanche ruggedness current as a function of pulse duration.

7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	mounted on a metal clad substrate; Figure 5	4	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed circuit board; minimum footprint	50	K/W

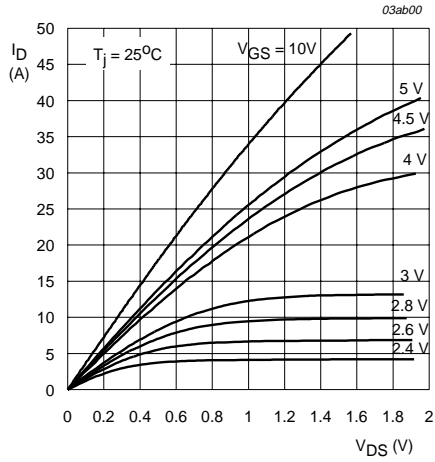
7.1 Transient thermal impedance



8. Characteristics

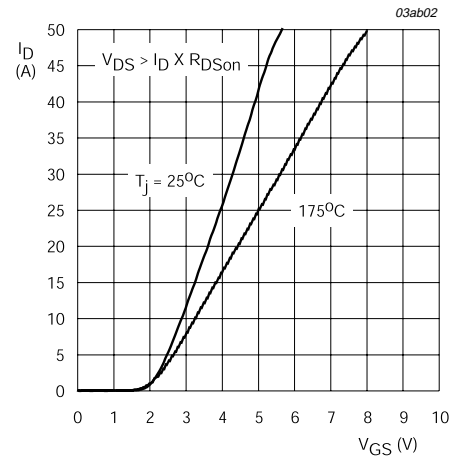
Table 5: Characteristics
T_j = 25 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V				
		T _j = 25 °C	30	40	–	V
		T _j = –55 °C	27	–	–	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; Figure 10				
		T _j = 25 °C	1	1.5	2	V
		T _j = 175 °C	0.5	–	–	V
		T _j = –55 °C	–	–	2.3	V
I _{DSS}	drain-source leakage current	V _{DS} = 30 V; V _{GS} = 0 V				
		T _j = 25 °C	–	0.05	10	μA
		T _j = 175 °C	–	5.0	500	μA
I _{GSS}	gate-source leakage current	V _{GS} = ±10 V; V _{DS} = 0 V	–	10	100	nA
R _{DS(on)}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 10 A; Figure 8 and 9				
		T _j = 25 °C	–	28	50	mΩ
		V _{GS} = 5 V; I _D = 10 A; Figure 8 and 9				
		T _j = 25 °C	–	38	56	mΩ
		T _j = 175 °C	–	70	104	mΩ
Dynamic characteristics						
g _{fs}	forward transconductance	V _{DS} = 10 V; I _D = 10 A; Figure 12	–	13	–	S
Q _{g(tot)}	total gate charge	I _D = 20 A; V _{DS} = 15 V;	–	10	–	nC
Q _{gs}	gate-source charge	V _{GS} = 5 V; Figure 15	–	2.7	–	nC
Q _{gd}	gate-drain (Miller) charge		–	5.7	–	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V;	–	460	–	pF
C _{oss}	output capacitance	f = 1 MHz; Figure 13	–	143	–	pF
C _{rss}	reverse transfer capacitance		–	107	–	pF
t _{d(on)}	turn-on delay time	V _{DD} = 15 V; R _D = 0.75 Ω;	–	18	–	ns
t _r	turn-off rise time	V _{GS} = 5 V; R _G = 10 Ω	–	130	–	ns
t _{d(off)}	turn-off delay time		–	22	–	ns
t _f	turn-off fall time		–	45	–	ns
Source-drain diode						
V _{SD}	source-drain (diode forward) voltage	I _S = 10 A; V _{GS} = 0 V; Figure 14	–	0.95	1.5	V
t _{rr}	reverse recovery time	I _S = 10 A;	–	65	–	ns
Q _r	recovered charge	di _S /dt = –100 A/μs; V _{GS} = 0 V; V _{DS} = 25 V	–	75	–	nC



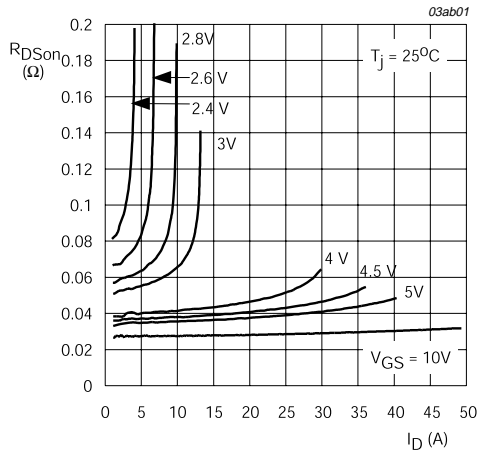
$T_j = 25^\circ\text{C}$

Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values.



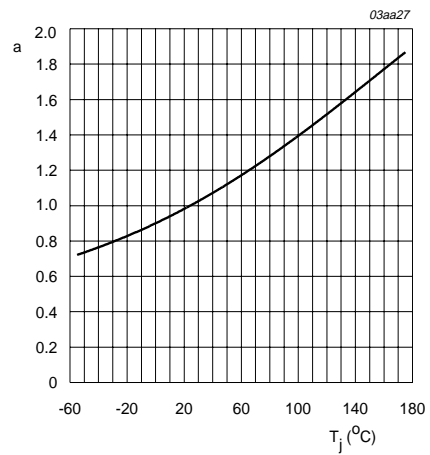
$T_j = 25^\circ\text{C}$ and 175°C ; $V_{DS} > I_D \times R_{DSon}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



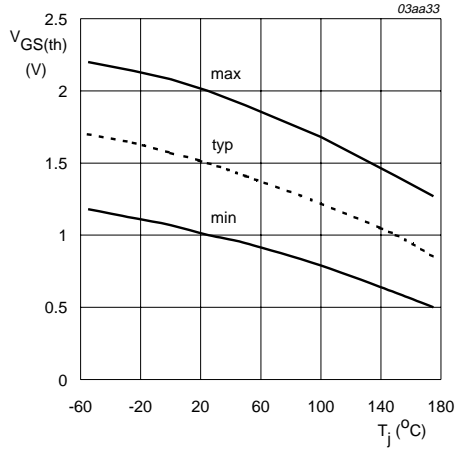
$T_j = 25^\circ\text{C}$

Fig 8. Drain-source on-state resistance as a function of drain current; typical values.



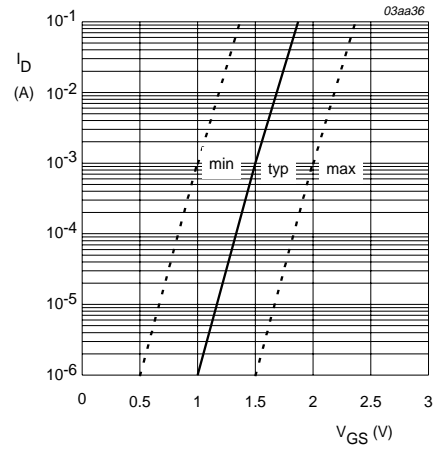
$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig 9. Normalized drain-source on-state resistance factor as a function of junction temperature.



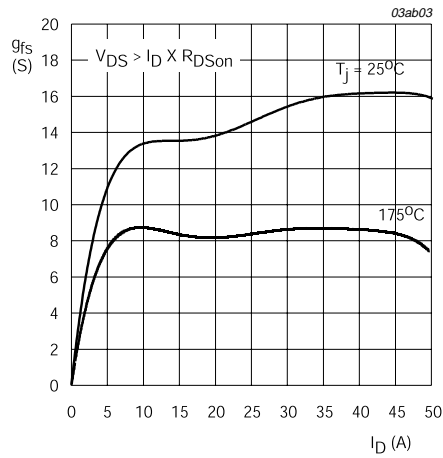
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 10. Gate-source threshold voltage as a function of junction temperature.



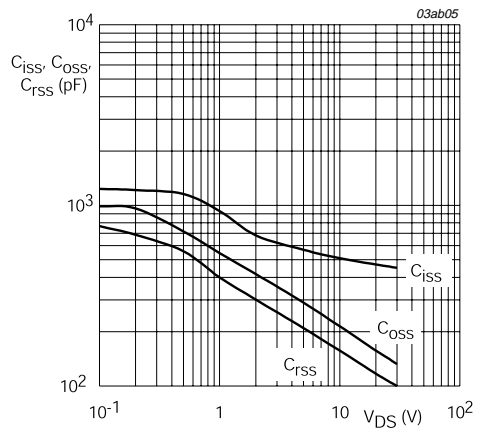
$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = 5 \text{ V}$

Fig 11. Sub-threshold drain current as a function of gate-source voltage.



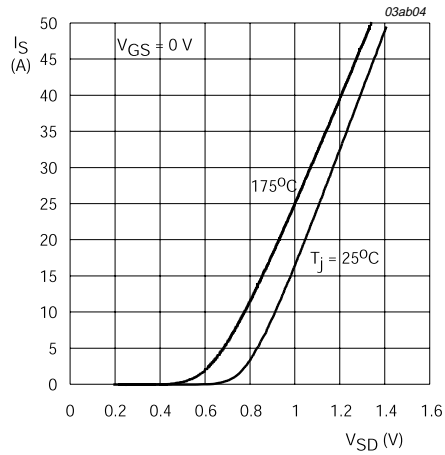
$T_j = 25 \text{ }^\circ\text{C}$ and $175 \text{ }^\circ\text{C}; V_{DS} > I_D \times R_{DSon}$

Fig 12. Forward transconductance as a function of drain current; typical values.



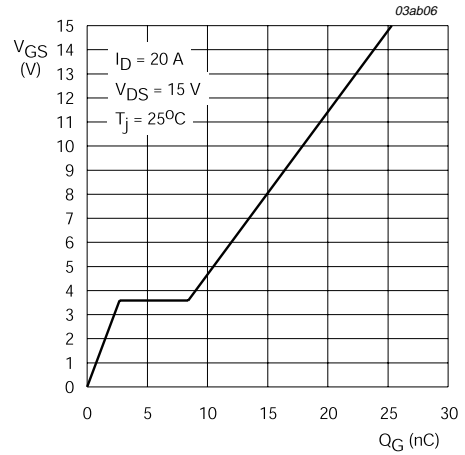
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25^\circ\text{C}$ and 175°C ; $V_{GS} = 0$ V

Fig 14. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



$I_D = 20$ A; $V_{DS} = 15$ V

Fig 15. Gate-source voltage as a function of gate charge; typical values.

9. Package outline

Plastic single-ended surface mounted package (Philips version of D-PAK); 3 leads (one lead cropped)

SOT428

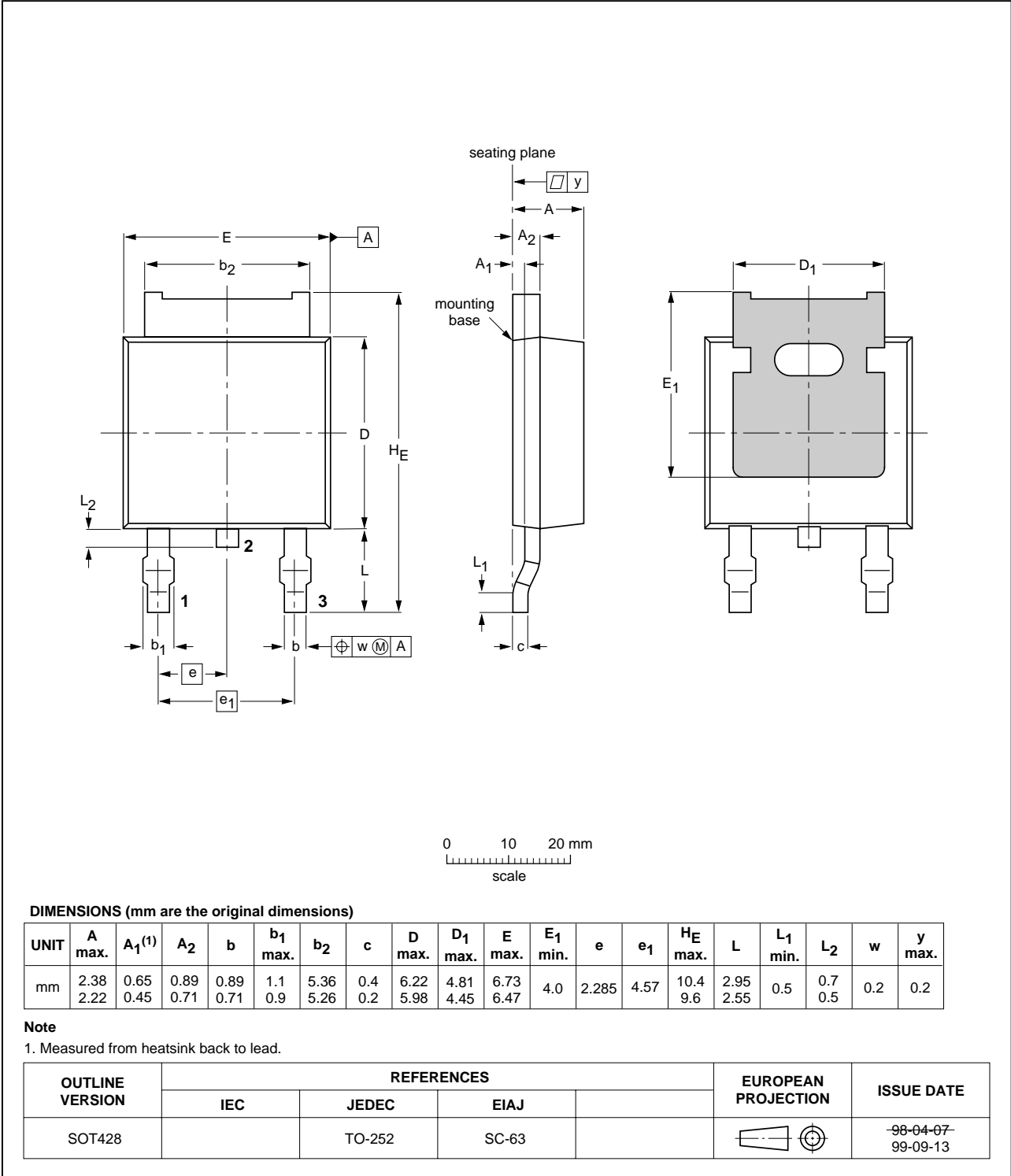


Fig 16. SOT428 (D-PAK).

10. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
02	20000727	-	Product specification; second version; supersedes PHD24N03LT_1 of 991201.
01	19991201	-	Product specification; initial version.

11. Data sheet status

Datasheet status	Product status	Definition ^[1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

12. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Argentina: see South America

Australia: Tel. +61 2 9704 8141, Fax. +61 2 9704 8139

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Belarus: Tel. +375 17 220 0733, Fax. +375 17 220 0773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Tel. +359 268 9211, Fax. +359 268 9102

Canada: Tel. +1 800 234 7381

China/Hong Kong: Tel. +852 2 319 7888, Fax. +852 2 319 7700

Colombia: see South America

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Denmark: Tel. +45 3 288 2636, Fax. +45 3 157 0044

Finland: Tel. +358 961 5800, Fax. +358 96 158 0920

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Ireland: Tel. +353 17 64 0000, Fax. +353 17 64 0200

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Malaysia: Tel. +60 37 50 5214, Fax. +60 37 57 4880

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For all other countries apply to: Philips Semiconductors,
Marketing Communications,
Building BE, P.O. Box 218, 5600 MD EINDHOVEN,
The Netherlands, Fax. +31 40 272 4825

Netherlands: Tel. +31 40 278 2785, Fax. +31 40 278 8399

New Zealand: Tel. +64 98 49 4160, Fax. +64 98 49 7811

Norway: Tel. +47 22 74 8000, Fax. +47 22 74 8341

Philippines: Tel. +63 28 16 6380, Fax. +63 28 17 3474

Poland: Tel. +48 22 5710 000, Fax. +48 22 5710 001

Portugal: see Spain

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Russia: Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Tel. +65 350 2538, Fax. +65 251 6500

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South Africa: Tel. +27 11 471 5401, Fax. +27 11 471 5398

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Taiwan: Tel. +886 22 134 2451, Fax. +886 22 134 2874

Thailand: Tel. +66 23 61 7910, Fax. +66 23 98 3447

Turkey: Tel. +90 216 522 1500, Fax. +90 216 522 1813

Ukraine: Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Tel. +44 208 730 5000, Fax. +44 208 754 8421

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Contents

1 Description 1

2 Features 1

3 Applications 1

4 Pinning information 1

5 Quick reference data 2

6 Limiting values 2

7 Thermal characteristics 4

7.1 Transient thermal impedance 4

8 Characteristics 5

9 Package outline 9

10 Revision history 10

11 Data sheet status 11

12 Definitions 11

13 Disclaimers 11



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