MN3111H

Vertical Driver LSI for Video Camera CCD Area Image Sensor

■ Overview

The MN3111H is a vertical driver LSI for a two-dimensional interline CCD image sensor. It features a built-in power supply circuit that, in conjunction with such external components as four booster capacitors, six voltage stabilization capacitors, eight Schottky barrier diodes, and two Zener diodes, produces stabilized +15.0V and –10.0V power supplies from a +5.0V input and HD pulses.

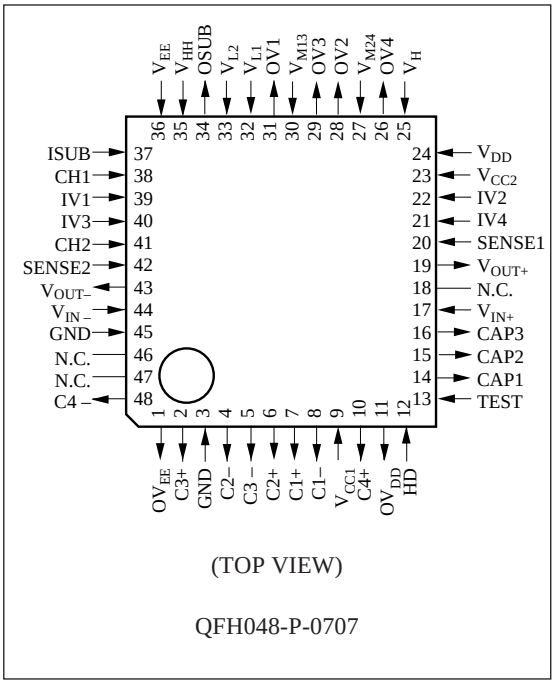
■ Features

- Single 5 volt power supply

■ Applications

- Video cameras

■ Pin Assignment



(TOP VIEW)

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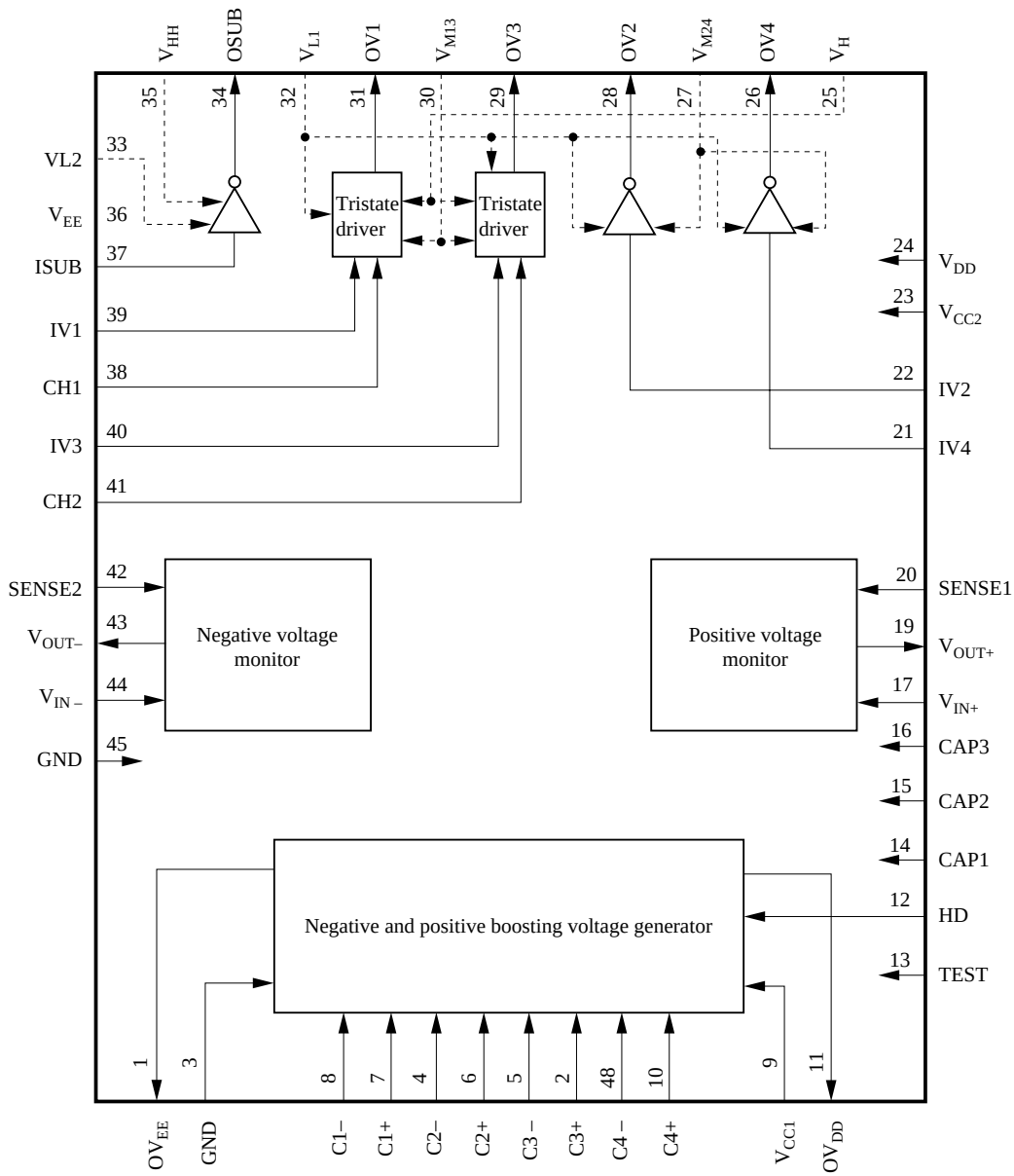
■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	Pin Name	I/O	Function Description
9 23	V_{CC1} V_{CC2}	"H" level power supply for input block	I	"H" level input for 5 volt circuits
3 45	GND	"L" level power supply for input block	I	"L" level input for 5 volt circuits
25	V_H	"H" level power supply for vertical driver	I	"H" level input for high-voltage circuits
35	V_{HH}	"H" level power supply for SUB driver	I	"H" level input for high-voltage circuits
30 27	V_{M13} V_{M24}	"M" level power supply for vertical driver	I	"M" level input for high-voltage circuits
32	V_{L1}	"L" level power supply for vertical driver	I	"L" level input for high-voltage circuits
33	V_{L2}	"L" level power supply for SUB driver	I	"L" level input for high-voltage circuits
24	V_{DD}	Driver power supply 1	I	"H" level for high-voltage circuits
36	V_{EE}	Driver power supply 2	I	"L" level for high-voltage circuits
17	V_{IN+}	Voltage input for positive voltage monitor	I	Voltage input pin for positive voltage monitor
44	V_{IN-}	Voltage input for negative voltage monitor	I	Voltage input pin for negative voltage monitor
13	TEST	Test input	I	Test pin (Keep this pin at "H" level.)
12	HD	HD pulse input	I	HD pulse input pin
22	IV2	Transfer pulse input	I	Charge transfer pulse input pin
21	IV4	Transfer pulse input	I	Charge transfer pulse input pin
39	IV1	Transfer pulse input	I	Charge transfer pulse input pin
40	IV3	Transfer pulse input	I	Charge transfer pulse input pin
38	CH1	Charge pulse input	I	Charge readout pulse input pin
41	CH2	Charge pulse input	I	Charge readout pulse input pin
37	ISUB	SUB pulse input	I	Unwanted charge rejection pulse input pin
20	SENSE1	Positive voltage monitor sensing input	I	Positive voltage monitor control sensing pin (Leave this pin open.)
42	SENSE2	Negative voltage monitor sensing input	I	Negative voltage monitor control sensing pin (Leave this pin open.)
7 8	C1+ C1–	C1 connection	O	Booster block voltage charging capacitor connection pins
6 4	C2+ C2–	C2 connection	O	Booster block voltage charging capacitor connection pins
2 5	C3+ C3 –	C3 connection	O	Booster block voltage charging capacitor connection pins
10 48	C4+ C4 –	C4 connection	O	Booster block voltage charging capacitor connection pins

■ Pin Descriptions (continued)

Pin No.	Symbol	Pin Name	I/O	Function Description
11	OV_{DD}	Booster block positive voltage output	O	Booster block positive voltage output pin
1	OV_{EE}	Booster block negative voltage output	O	Booster block negative voltage output pin
19	V_{OUT+}	Positive regulated voltage output	O	Positive voltage monitor output pin (Leave this pin open.)
43	V_{OUT-}	Negative regulated voltage output	O	Negative voltage monitor output pin (Leave this pin open.)
26	OV4	Binary transfer pulse output	O	Binary (V_{M24}, V_{L1}) transfer pulse output pin
28	OV2	Binary transfer pulse output	O	Binary (V_{M24}, V_{L1}) transfer pulse output pin
29	OV3	Tristate transfer pulse output	O	Tristate (V_H, V_{M13}, V_{L1}) transfer pulse output pin
31	OV1	Tristate transfer pulse output	O	Tristate (V_H, V_{M13}, V_{L1}) transfer pulse output pin
34	OSUB	SUB pulse output	O	Unwanted charge (V_{HH}, V_{L2}) rejection pulse input pin
14 15 16	CAP1 CAP2 CAP3	Stabilizing capacitor connection	O	Pins for connecting capacitors for internal voltage stabilization circuits
18 46 47	N.C.	No connection	—	

■ Functional Description

Binary transfer pulses (vertical driver block)

IV2 IV4	OV2 OV4
H	L
L	M

Tristate transfer pulses (vertical driver block)

CH1 CH2	IV1 IV3	OV1 OV3
H	H	L
	L	M
L	H	L
	L	H

*1 IV1, IV2, IV3, IV4, CH1, CH2

H: V_{CC}

L: GND

OV1, OV2, OV3, OV4

H: V_H

M: V_{M13} , or V_{M24}

L: V_{L1}

Unwanted charge rejection pulses (SUB driver block)

ISUB	OSUB
H	L
L	H

*1 ISUB

H: V_{CC}

L: GND

OSUB

H: V_{HH}

L: V_{L2}

■ Electrical Characteristics

(1) DC characteristics

V_{HH}=V_H=15.0V, V_{M13}=V_{M24}=1.0V, GND=0.0V,

V_{CC1}=V_{CC2}=5.0V (=V_{CC}), V_{L1}=–7.0V, V_{L2}=–10.0V, Ta=+25˚C

Parameter	Symbol	Test conditions	min	typ	max	Unit
Quiescent supply current	I_{DDST}	V_I=GND, V_{CC}			4	mA
Operating supply current	I_{DDDYN}	V_I=GND, V_{CC}			11	mA
Power supply output pins	OV_{DD}, OV_{EE}					
Positive voltage stabilization circuit output voltage	V_{REG+}	V_I=GND, V_{CC}, I_O=7mA	14.5	15.0	15.5	V
Negative voltage stabilization circuit output voltage	V_{REG-}	V_I=GND, V_{CC}, I_O=–2mA	–10.5	–10.0	–9.5	V
Input pins	IV1, IV2, IV3, IV4, CH1, CH2, ISUB, HD					
"H" level voltage	V_{IH}		3.5		V_{CC}	V
"L" level voltage	V_{IL}		GND		1.5	V
Input leak current	I_{LI}	V_I=0 to 5V			±1	µA
Output pins 1 (Binary output)	OV2, OV4					
Output voltage "M" level	V_{OM1}	V_I=GND, V_{CC}, I_{OM1}=–1mA	0.9		V_{M24}	V
Output voltage "L" level	V_{OL1}	V_I=GND, V_{CC}, I_{OL1}=1mA	V_{L1}		–6.9	V
Output on resistance "M" level	R_{ONM1}	I_{OM1}=–50mA			40	Ω
Output on resistance "L" level	R_{ONL1}	I_{OL1}=50mA			40	Ω
Output pins 2 (Tristate output)	OV1, OV3					
Output voltage "H" level	V_{OH2}	V_I=GND, V_{CC}, I_{OH2}= –1mA	14.9		V_H	V
Output voltage "M" level	V_{OM2}	V_I=GND, V_{CC}, I_{OM2}=–1mA	0.9		V_{M13}	V
Output voltage "L" level	V_{OL2}	V_I=GND, V_{CC}, I_{OL2}=1mA	V_{L1}		–6.9	V
Output on resistance "H" level	R_{ONH2}	I_{OH2}=–50mA			50	Ω
Output on resistance "M" level	R_{ONM2}	I_{OM2}=±50mA			40	Ω
Output on resistance "L" level	R_{ONL2}	I_{OL2}=50mA			40	Ω
Output pin 3 (SUB output)	OSUB					
Output voltage "H" level	V_{OHH3}	V_I=GND, V_{CC}, I_{OHH3}=–1mA	14.9		V_{HH}	V
Output voltage "L" level	V_{OL3}	V_I=GND, V_{CC}, I_{OL3}=1mA	V_{L2}		–9.9	V
Output on resistance "H" level	R_{ONHH3}	I_{ONHH3}=–50mA			50	Ω
Output on resistance "L" level	R_{ONL3}	I_{ONL3}=50mA			40	Ω

(2) AC characteristics

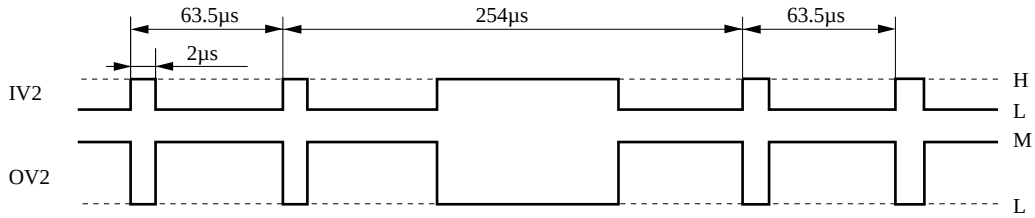
$V_{HH}=V_H=15.0V$, $V_{M13}=V_{M24}=1.0V$, GND=0.0V,

$V_{CC1}=V_{CC2}=5.0V$ ($=V_{CC}$), $V_{L1}=-7.0V$, $V_{L2}=-10.0V$, Ta=+25˚C

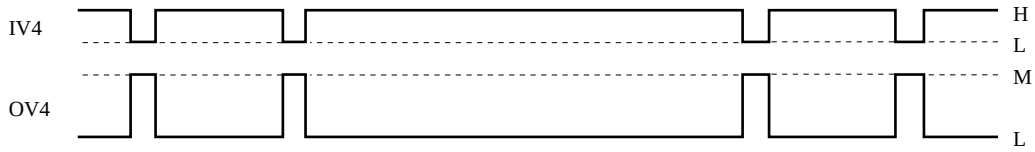
Parameter	Symbol	Test conditions	min	typ	max	Unit
Output pins 1 (Binary output)	OV2, OV4					
Transmission delay	t_{PLM} t_{PML}	No load From "L" level to "M" level		100	200	ns
Rise time Fall time	t_{TLM} t_{TML}			200	300	ns
Output pins 2 (Tristate output)	OV1, OV3					
Transmission delay	t_{PLM} t_{PML}	No load From "L" level to "M" level		100	200	ns
Transmission delay	t_{PMH} t_{PHM}	No load From "M" level to "H" level		200	400	ns
Rise time Fall time	t_{TLM} t_{TML}			200	300	ns
Rise time Fall time	t_{TMH} t_{THM}			200	300	ns
Output pin 3 (SUB output)	OSUB					
Transmission delay	t_{PLHH} t_{PHHL}	No load From "L" level to "H" level		100	200	ns
Rise time Fall time	t_{TLHH} t_{THHL}			200	300	ns

■ Timing Chart

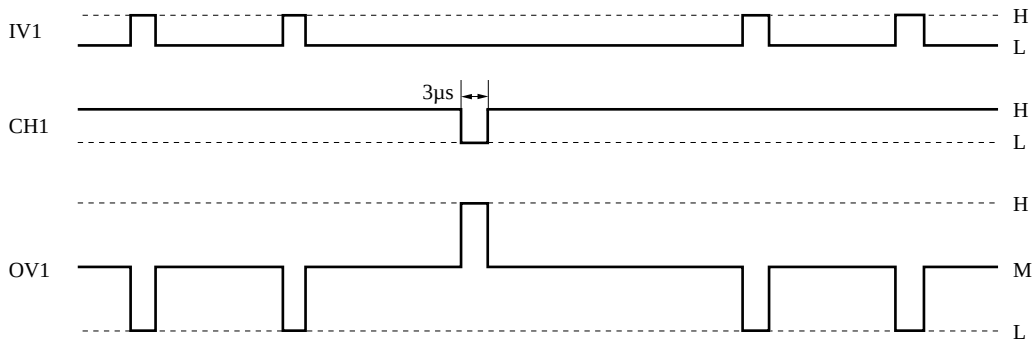
1. Binary transfer pulses



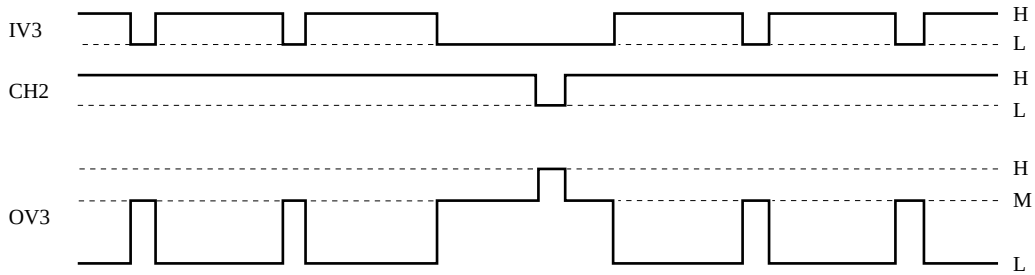
2. Binary transfer pulses



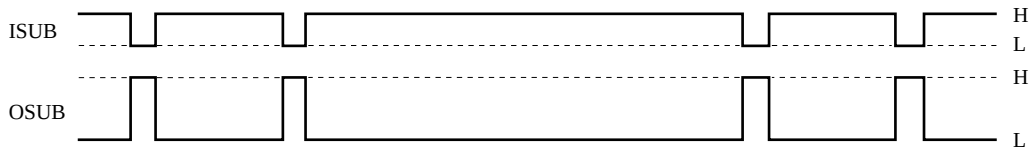
3. Tristate transfer pulses



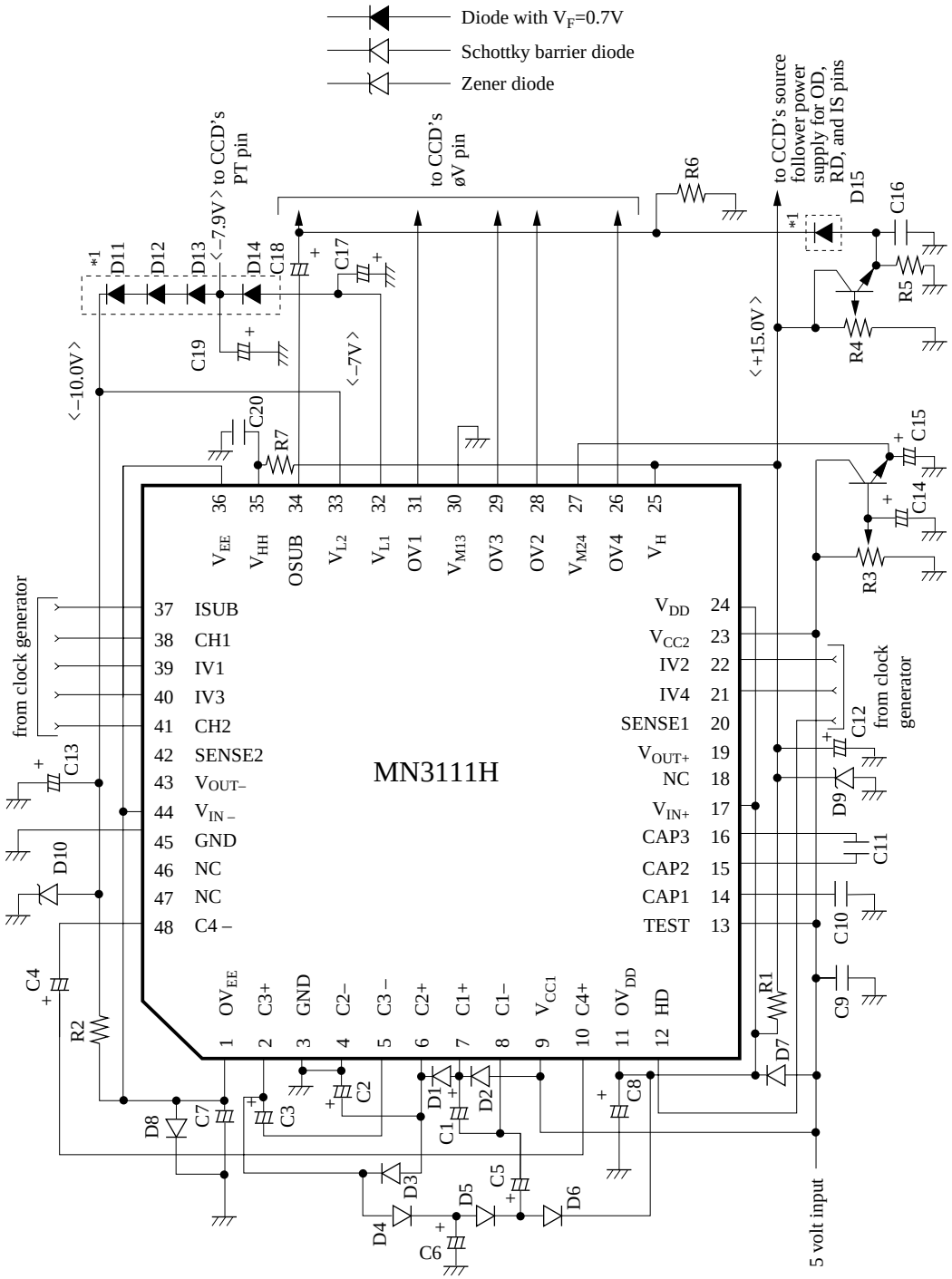
4. Tristate transfer pulses



5. SUB pulses



■ Application Circuit Example



The booster circuit's electrolytic capacitors must have little impedance fluctuation at low temperatures.

Note *1: These diodes must have a V_F of 0.7 V. All other diodes, except the Zener diodes, must be Schottky barrier diodes (MA723).

■ Package Dimensions (Unit: mm)

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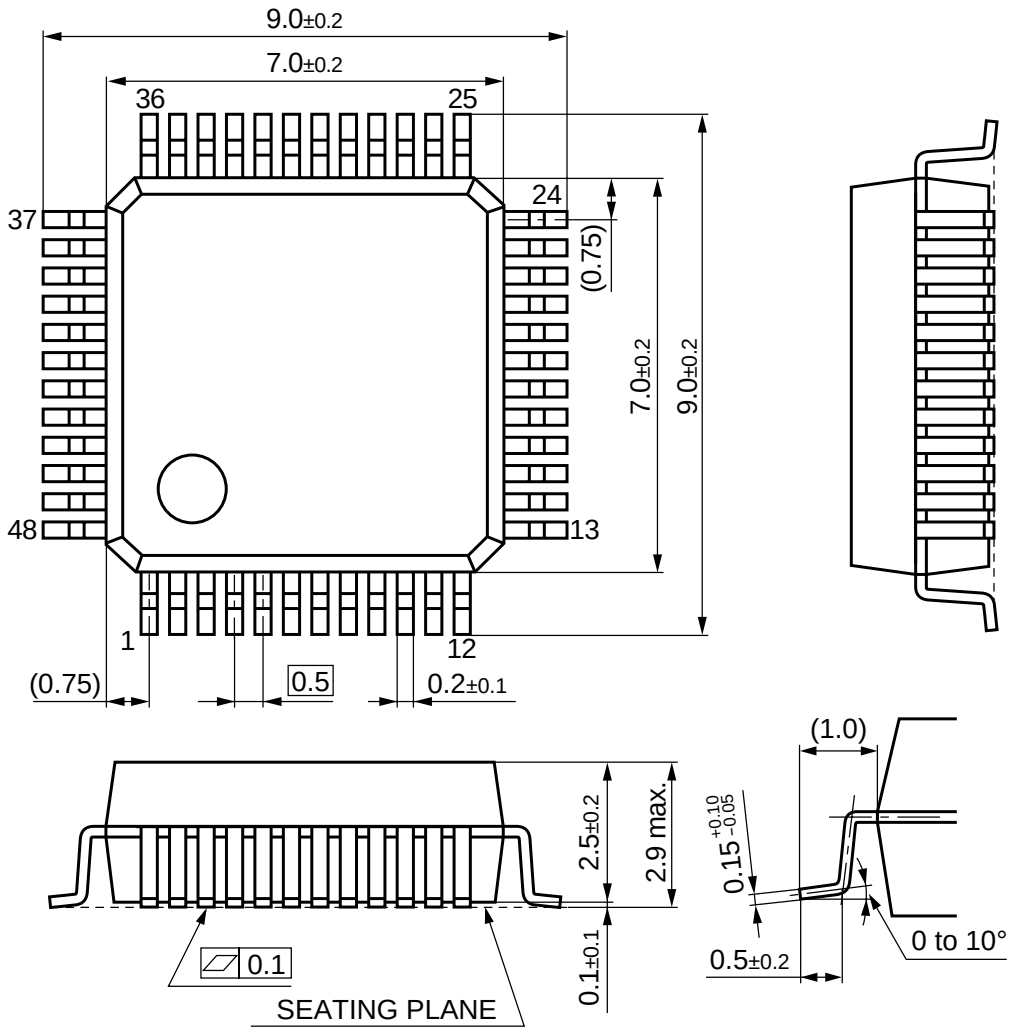


■ Usage Notes

External components

1. This product requires eight Schottky barrier diodes and two Zener diodes.

   We recommend the following components.

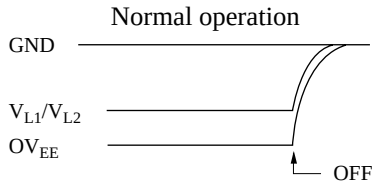
Schottky barrier diodes:	MA723 or equivalents
Zener diodes:	MA1150-M, MA8150-M (for positive regulated voltage) or equivalents
	MA1100-M, MA8100-M (for negative regulated voltage) or equivalents

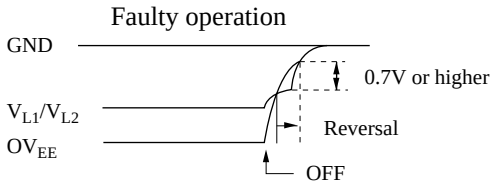
Ta=25˚C

Component	Model number	Typical characteristics	Notes
Schottky barrier diodes	MA723	I_F =200mA, $V_F \leq 0.55$V	
Zener diodes	MA1150-M MA8150-M	I_Z=5mA, 14.6V ≤ V_Z ≤ 15.35V	for positive regulated voltage
	MA1100-M MA8100-M	I_Z=5mA, 9.75V ≤ V_Z ≤ 10.25V	for negative regulated voltage

The MN3111H will not operate properly if the components do not satisfy the above specifications.

2. Always use the specified components for peripheral circuits so as to ensure that OV_{EE} and V_L do not reverse potentials when the power is turned off.





As the above sketch illustrates, allowing OV_{EE} to exceed V_{L1} and V_{L2} by more than 0.7 V produces the risk of applying a forward bias to the PN junction, turning on the parasitic transistor, and generating an overcurrent that produces latch-up.

If this phenomenon arises, increase the size of capacitor C7 or decrease the size of capacitor C13 to increase the OV_{EE} time constant.

(See the sample application circuit for the locations of C7 and C13.)

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