Ordering number: EN 5550

CMOS LSI

LC86P4164

8-bit Single Chip Microcontroller

Overview

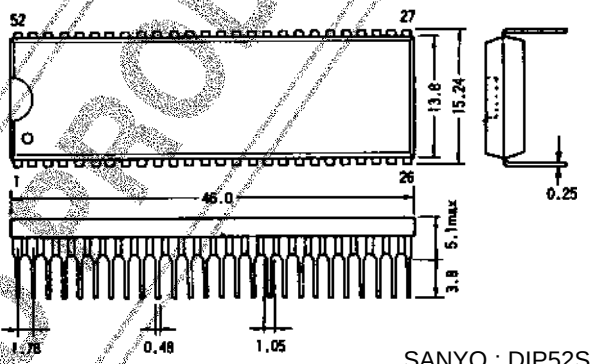
The LC86P4164 is a CMOS 8-bit single chip microcontroller with one-time PROM for the LC864100 series.
This microcontroller has the function and the pin description of the LC864100 series mask ROM version, and the 64K-byte PROM. It is suitable for developing programs.

Package Dimensions

unit : mm

3128-DIP52S

[LC86P4164]



SANYO : DIP52S

Features

(1) Option switching by PROM data
The option function of the LC864100 series can be specified by the PROM data.
The functions of the trial pieces can be evaluated using the mass production board.
(2) Internal PROM capacity : 65512 bytes (for program data)
: 8192 × 12 bits (for character data)
(3) Internal RAM capacity : 384 bytes

Mask ROM version	PROM capacity	RAM capacity
LC864164	65512 bytes	384 bytes
LC864156	57344 bytes	384 bytes
LC864148	49152 bytes	384 bytes
LC864140	40960 bytes	384 bytes
LC864132	32768 bytes	384 bytes
LC864124	24576 bytes	384 bytes
LC864120	20480 bytes	384 bytes
LC864116	16384 bytes	384 bytes
LC864112	12288 bytes	384 bytes

(4) Operating supply voltage : 4.5 V to 5.5 V
(5) Instruction cycle time : 1.0 µs to 30 µs
(6) Operating temperature : –30°C to +70°C
(7) The pin and the package compatible with the LC864100 series mask ROM devices
(8) Applicable mask ROM version : LC864164/LC864156/LC864148/LC864140/LC864132
LC864124/LC864120/LC864116/LC864112
(9) Factory shipment : DIP52S

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Usage Notes

The LC86P4164 is provided for the first release and small shipping of the LC864100 series.
At using, take notice of the followings.

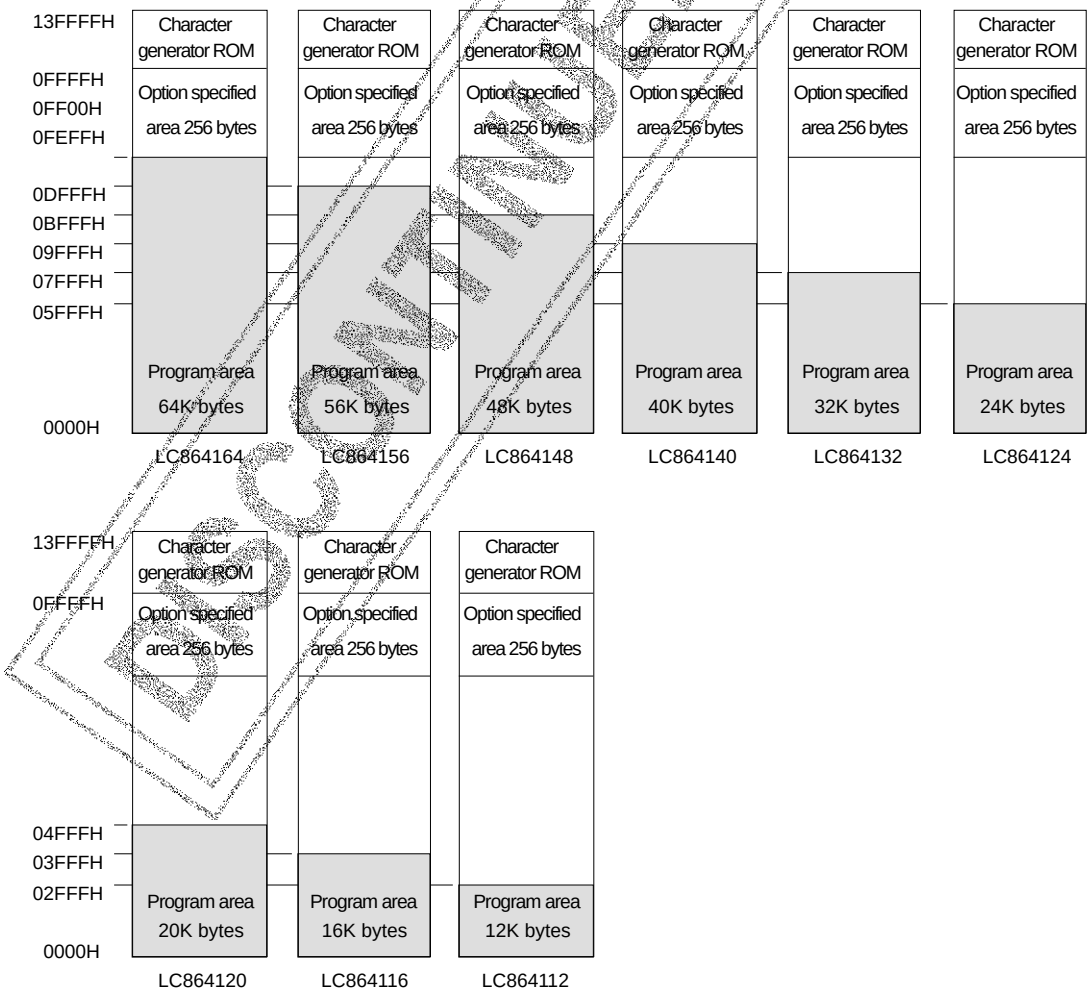
(1) Differences between the LC86P4164 and the LC864100 series

Item	LC86P4164	LC864164/56/48/40/32/24/20/16/12
Operation after reset releasing	The option is specified by degrees until 3 ms after going to a 'H' level to the reset terminal. The program is executed from 00H of the program counter.	The program is executed from 00H of the program counter immediately after going to a 'H' level to the reset terminal.
Operating supply voltage range (V_{DD})	4.5 V to 6.0 V	4.5 V to 6.0 V
Operating temperature range (Topr)	–30 to +70°C	–30 to +70°C
Power dissipation	Refer to 'electrical characteristics' on the semiconductor news.	

The LC86P4164 uses the program memory area of 256 bytes from FF00H to FFFFH to select the options.

(2) Option
The option data is created by the option specified program "SU86K.EXE". The created option data is linked to the program area by the linkage loader "L86K.EXE".

(3) ROM space
The LC86P4164 and LC864100 series use the program memory area of 256 bytes from FF00H to FFFFH to select options.
The program memory has 65280 bytes from 0000H to FEFFH.



How to use

(1) Create a programming data for LC86P4164
Programming data for EPROM of the LC86P4164 is required.
Debugged evaluation file (EVA file) must be converted to an INTEL-HEX formatted file (HEX file) with file converter program, SU86K.EXE. The HEX file is used as the programming data for the LC86P4164.

(2) How to program for the PROM
The LC86P4164 can be programmed by the EPROM programmer with attachment; W86EP4164D.

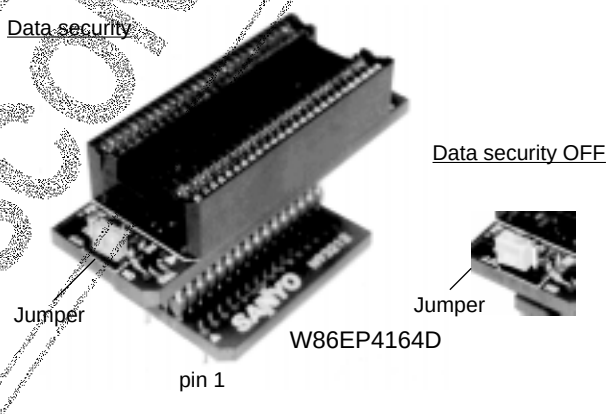
- Recommended EPROM programmer

Manufacturer	EPROM progammer
Advantest	R4945, R4944
Andou	AF-9704
AVAL	PKW-1100, PKW-3000
Minato electoronics	MODEL 1890A

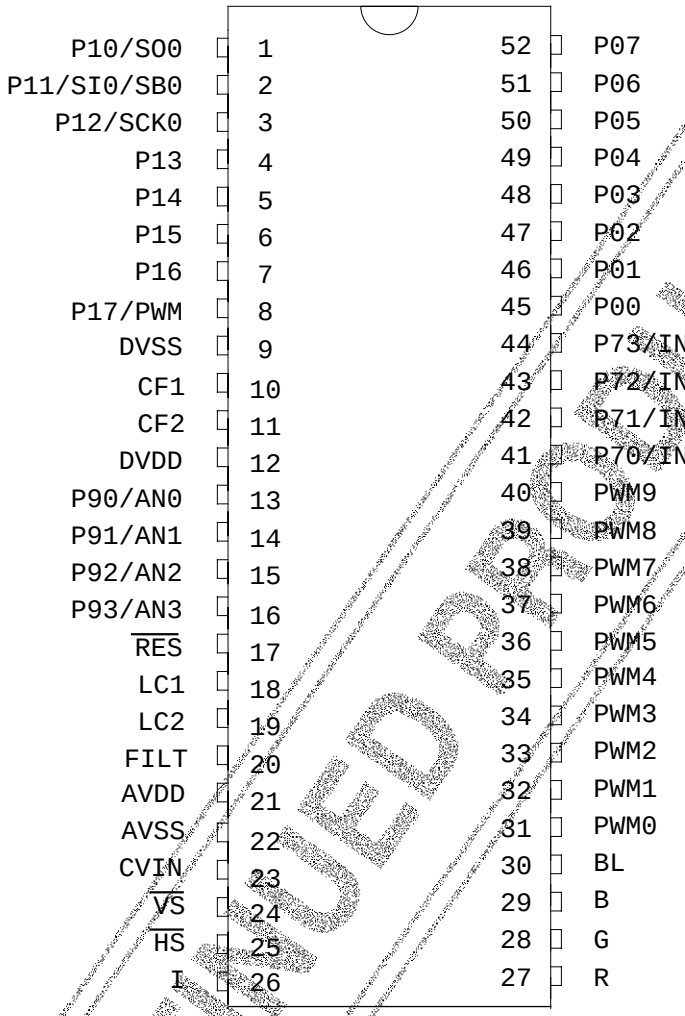
- "27010 (Vpp=12.5V) Intel high speed programming" mode should be adopted. The address must be set to "0 to 13FFFH" and a jumper (DASEC) must be set to 'OFF' at programming.

(3) How to use the data security function
"Data security" is the function to disable the EPROM data from being read out.
The following is the procedure in order to execute the data security function.
1. Set 'ON' the jumper of attachment.
2. Program again. Then the EPROM programmer displays an error. The error means that the data security functions normally. It is not a trouble of the EPROM programmer or the LSI.

Notes
- Data security is not executed when the data of all address have 'FF' at the procedure 2 above.
- Data security cannot be executed by programming the sequential operation "BLANK=>PROGRAM=>VERIFY" at procedure 2 above.
- Set the jumper to 'OFF' after executing the data security.

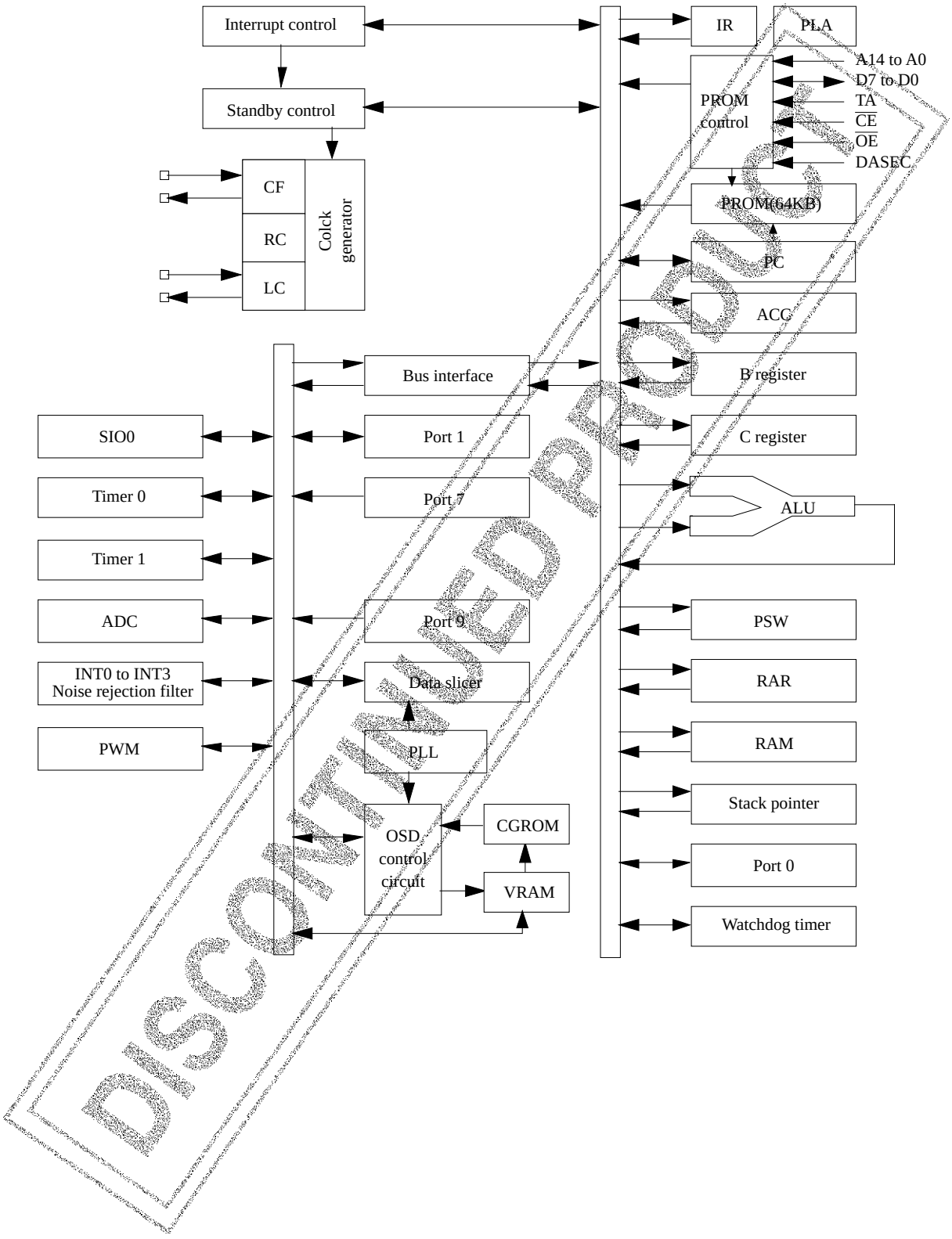


Pin Assignment



Top view

System Block Diagram



Pin Description

Pin name	Pin No.	I/O	Function description	Option	PROM mode
DVSS	9	—	Negative power supply for digital circuit		
CF1	10	I	Input terminal for ceramic resonator		
CF2	11	O	Output terminal for ceramic resonator		
DVDD	12	—	Positive power supply for digital circuit		
$\overline{RES}$	17	I	Reset terminal		
LC1	18	I	LC oscillation circuit input terminal		
LC2	19	O	LC oscillation circuit output terminal		
FILT	20	O	Filter terminal for PLL		
AVDD	21	—	Positive power supply for analog circuit		
AVSS	22	—	Negative power supply for analog circuit		
CVIN	23	I	Video signal input terminal		
$\overline{VS}$	24	I	Vertical synchronization signal input terminal		
$\overline{HS}$	25	I	Horizontal synchronization signal input terminal		
I	26	O	Image intensity control output		
R	27	O	Red (R) output terminal of RGB image output		A4 (*1)
G	28	O	Green (G) output terminal of RGB image output		A5 (*1)
B	29	O	Blue (B) output terminal of RGB image output		A6 (*1)
BL	30	O	Fast blanking control signal Switch TV image signal and caption/ OSD image signal		A7 (*1)
PWM0 to PWM9	31 to 40	O	PWM0 to PWM9 output terminal 15V withstand		PWM0 to PWM8 : A8 to A16 (*1) PWM9 : "L" fixed
Port 0 P00 to P07	45 to 52	I/O	8-bit Input/output port Input/output can be specified in nibble unit HOLD release input Interrupt input	Pull-up resistor Provided/not provided (in bit units) Output Format CMOS/Nch-OD (in bit units)	
Port 1 P10 to P17	1 to 8	I/O	8-bit Input/output port Input/output can be specified in bit unit. Other functions P10 SIO0 data output P11 SIO0 data input /bus input/output P12 SIO0 clock input/output P17 Timer 1 (PWM) output	Output Format CMOS/Nch-OD (in bit unit)	D0 to D7 (*2)

Continued on next page.

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<table>
<tr><th>Pin name</th><th>Pin No.</th><th>I/O</th><th>Function Description</th><th>Option</th><th>PROM mode</th></tr>
<tr><td>Port 7
P70
P71 to P73</td><td>
41
42 to 44</td><td>
I/O
I</td><td>4-bit input port
Other functions
P70 : INT0 input/HOLD release input/ Nch-transistor output for watchdog timer
P71 : INT1 input/HOLD release input
P72 : INT2 input/timer 0 event input
P73 : INT3 input (noise rejection filter attached input/timer 0 event input
Interrupt receiver format vector address
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising/Falling</th><th>H level</th><th>L level</th><th>Vector</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>03H</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>0BH</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>13H</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>1BH</td></tr>
</table></td><td>Pull-up resistor provided/ not provided (in bit units)</td><td>P70 : VPP (*3)
P71 : DASEC (*4)
P72 : OE (*5)
P73 : CE (*6)</td></tr>
<tr><td>Port 9
P90 to P93</td><td>
13 to 16</td><td>
I</td><td>4-bit input port
Other function
A/D converter input port (4 lines)</td><td></td><td>A0 to A3 (*3)</td></tr>
</table>

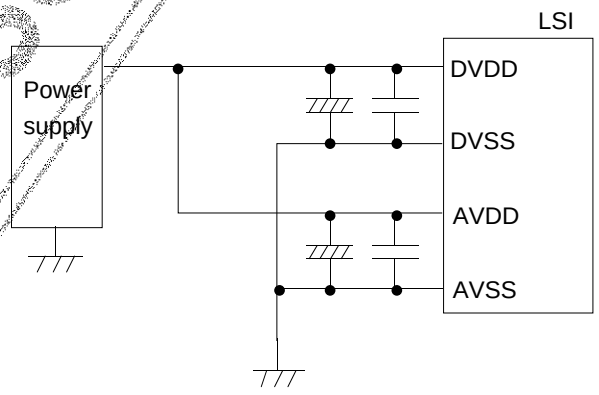
*1 An → Address input
*2 Data I/O
*3 Power for programming
*4 Memory select input/output for data security
*5 Output Enable input
*6 Chip Enable input

- All of port options except the 4-bit unit pull-up resistor option of Port 0 can be specified in a bit unit.

• Port status during reset

Terminal	I/O	Pull-up resistor status at selecting pull-up option
Port 0	Input	Pull-up resistor OFF, ON after reset release
Port 1	Input	Programmable pull-up resistor OFF
Port 7	Input	Fixed pull-up resistor provided

* AVDD and AVSS are the power supply terminals for built-in analog circuit while DVDD and DVSS are the power supply terminals for built-in digital circuit. Connect them like the following figure to reduce the mutual noise influence.



Specifications

1. Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter		Symbol	Pins	Conditions		Ratings			Unit
					V_{DD} [V]	min	typ	max	
Supply voltage		V_{DD}max	DVDD, AVDD	DVDD = AVDD		–0.3		+7.0	V
Input voltage		V_I(1)	• P71, 72, 73 • Port 9 • $\overline{RES}$,$\overline{HS}$,$\overline{VS}$,CVIN			–0.3		V_{DD}+0.3	
Output voltage		V_O(1)	R, G, B, BL, I, FILT			–0.3		V_{DD}+0.3	
		V_O(2)	PWM0 to PWM9			–0.3		+15	
Input/output voltage		V_{IO}(1)	Ports 0, 1, P70			–0.3		V_{DD}+0.3	
High-level output current	Peak output current	I_{OPH}(1)	Ports 0, 1	• Pull-up MOS transistor output • At each pin		–2			mA
		I_{OPH}(2)	Ports 0, 1	• CMOS output • At each pin		–4			
		I_{OPH}(3)	R, G, B, BL, I	• CMOS output • At each pin		–5			
	Total output current	$\sum I_{OAH}$(1)	Port 1	The total of all pins		–10			
		$\sum I_{OAH}$(2)	Port 0	The total of all pins		–10			
		$\sum I_{OAH}$(3)	R, G, B, BL, I	The total of all pins		–15			
Low-level output current	Peak output current	I_{OPL}(1)	Ports 0, 1	At each pin				20	
		I_{OPL}(2)	P70	At each pin				30	
		I_{OPL}(3)	• R, G, B, BL, I • PWM0 to PWM9	At each pin				5	
	Total output current	$\sum I_{OAL}$(1)	Port 0	The total of all pins				40	
		$\sum I_{OAL}$(2)	Port 1, P70	The total of all pins				40	
		$\sum I_{OAL}$(3)	R, G, B, BL, I	The total of all pins				15	
		$\sum I_{OAL}$(4)	PWM0 to PWM9	The total of all pins				30	
Maximum power dissipation		Pd max	DIP52S	Ta = –30 to +70°C				430	mW
Operating temperature range		Topr				–30		+70	°C
Storage temperature range		Tstg				–55		+125	

* DVSS and AVSS must be supplied the same voltage, V_{SS}. V_{SS} = DVSS = AVSS
DVDD and AVDD must be supplied the same voltage, V_{DD}. V_{DD} = DVDD = AVDD

2. Recommended Operating Range at Ta = –30°C to +70°C, V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions		Ratings			Unit
				V_{DD} [V]	min	typ	max	
Operating supply voltage range	V_{DD}	DVDD, AVDD	0.98 µs ≤ tCYC tCYC ≤ 1.02 µs		4.5		5.5	V
Hold voltage	V_{HD}	DVDD, AVDD	RAMs and the registers hold data at HOLD mode.		2.0		5.5	
Input high-level voltage	V_{IH}(1)	Port 0 (Schmitt)	Output disable	4.5 to 5.5	0.6V_{DD}		V_{DD}	
	V_{IH}(2)	• Port 1 (Schmitt) • P72,73 • $\overline{HS}$,$\overline{VS}$	Output disable	4.5 to 5.5	0.75V_{DD}		V_{DD}	
	V_{IH}(3)	• P70 port input / interrupt • P71 • $\overline{RES}$ (Schmitt)	Output N-channel transistor OFF	4.5 to 5.5	0.75V_{DD}		V_{DD}	
	V_{IH}(4)	P70 Watchdog timer input	Output N-channel transistor OFF	4.5 to 5.5	V_{DD}-0.5		V_{DD}	
	V_{IH}(5)	Port 9 port input		4.5 to 5.5	0.7V_{DD}		V_{DD}	
Input low-level voltage	V_{IL}(1)	Port 0 (Schmitt)	Output disable	4.5 to 5.5	V_{SS}		0.2V_{DD}	
	V_{IL}(2)	• Port 1 (Schmitt) • P72,73 • $\overline{HS}$,$\overline{VS}$ • Port 9	Output disable	4.5 to 5.5	V_{SS}		0.25V_{DD}	
	V_{IL}(3)	• P70 port input / interrupt • P71 • $\overline{RES}$ (Schmitt)	N-channel transistor OFF	4.5 to 5.5	V_{SS}		0.25V_{DD}	
	V_{IL}(4)	P70 Watchdog timer input	N-channel transistor OFF	4.5 to 5.5	V_{SS}		0.6V_{DD}	
	V_{IL}(5)	Port 9 port input		4.5 to 5.5	V_{SS}		0.3V_{DD}	
CVIN input amplitude	V_{CVIN}	CVIN		5.0	0.7		2.3	Vp-p *
Operation cycle time	tCYC(1)		OSD function	4.5 to 5.5	0.98	1	1.02	µs
	tCYC(2)		Except OSD function	4.5 to 5.5	0.98		30	

* Vp-p : Peak-to-peak voltage

Parameter	Symbol	Pins	Conditions		Ratings			Unit
				V_{DD} [V]	min	typ	max	
Oscillation frequency range (Note 1)	FmCF	CF1, CF2	12MHz (ceramic resonator oscillation) Refer to Figure 1.	4.5 to 5.5	11.76	12	12.24	MHz
	FmLC	LC1, LC2	14.11MHz (LC oscillation) Refer to Figure 2.	4.5 to 5.5		14.11		
	FmRC		RC oscillation	4.5 to 5.5	0.4	0.8	2.0	
Oscillation stable time period (Note 2)	tmsCF	CF1, CF2	12 MHz (ceramic resonator oscillation) Refer to Figure 3.	4.5 to 5.5		0.02	0.2	ms

(Note 1) The oscillation constant is shown on Table 1 and Table 2.

(Note 2) The oscillation stable time period means the time to oscillate stably after the following conditions.

1. Supplying voltage.
2. Release the HOLD mode.
3. Release stopping the main-clock oscillation.

Refer to Figure 3 for details.

3. Electrical Characteristics at Ta = –30°C to +70°C, V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions	Ratings				Unit
				V_{DD}[V]	min	typ	max	
Input high-level current	I_{IH}(1)	• Port 1 • Port 0 without pull-up MOS transistor	• Output disable • Pull-up MOS transistor OFF • V_{IN} = V_{DD} (including the off-leak current of the output transistor)	4.5 to 5.5			1	µA
	I_{IH}(2)	• Port 7 without pull-up MOS transistor • Port 9 • $\overline{RES}$ • HS,VS	V_{IN} = V_{DD}	4.5 to 5.5			1	
Input low-level current	I_{IL}(1)	• Port 1 • Port 0 without pull-up MOS transistor	• Output disable • Pull-up MOS transistor OFF • V_{IN} = V_{SS} (including the off-leak current of the output transistor)	4.5 to 5.5	–1			
	I_{IL}(2)	• Port 7 without pull-up MOS transistor • Port 9	V_{IN} = V_{SS}	4.5 to 5.5	–1			
	I_{IL}(3)	• $\overline{RES}$ • HS,VS	V_{IN} = V_{SS}	4.5 to 5.5	–1			
Output high-level voltage	V_{OH}(1)	CMOS output of Ports 0,1	I_{OH} = –1.0 mA	4.5 to 5.5	V_{DD}–1			V
	V_{OH}(2)	R, G, B, BL, I	I_{OH} = –0.1 mA	4.5 to 5.5	V_{DD}–0.5			
Output low-level voltage	V_{OL}(1)	Ports 0, 1	I_{OL} = 10 mA	4.5 to 5.5			1.5	
	V_{OL}(2)	Ports 0, 1	• I_{OL} = 1.6 mA • The total current of the ports 0,1 is not over 40 mA	4.5 to 5.5			0.4	
	V_{OL}(3)	• R, G, B, BL, I • PWM0 to PWM9	• I_{OL} = 30 mA • The current of any unmesurement pin is not over 3 mA.	4.5 to 5.5			0.4	
	V_{OL}(4)	P70	I_{OL} = 1 mA	4.5 to 5.5			0.4	
Pull-up MOS transistor resistance	Rpu	• Ports 0,1 • Port 7	V_{OH} = 0.9 V_{DD}	4.5 to 5.5	13	38	80	kΩ
Output off-leakage current	I_{OFF}	PWM0 to PWM9	V_{OUT} = 13.5 V	4.5 to 5.5			5	µA
Hysteresis voltage	V_{HIS}	• Ports 0,1 • Port 7 • $\overline{RES}$ • HS,VS	Output disable	4.5 to 5.5		0.1 V_{DD}		V

Parameter	Symbol	Pins	Conditions	Ratings				Unit
				V_{DD}[V]	min	typ	max	
Input clamp voltage	V_{CLMP}	CVIN		5.0	2.3	2.5	2.7	V
Pin capacitance	CP	All pins	• f = 1 MHz • Unmeasured input pins are set to V_{SS} level. • Ta = 25°C	4.5 to 5.5		10		pF

4. Serial Input/Output Characteristics at Ta = –30°C to +70°C, V_{SS} = 0 V

Parameter			Symbol	Pins	Conditions	Ratings				Unit
						V_{DD}[V]	min	typ	max	
Serial clock	Input clock	Cycle	tCKCY (1)	• SCK0 • SCLK0	Refer to Figure 5.	4.5 to 5.5	2			tCYC
		Low-level pulse width	tCKCY (1)			4.5 to 5.5	1			
		High-level pulse width	tCKCY (1)			4.5 to 5.5	1			
	Output clock	Cycle	tCKCY (2)	• SCK0 • SCLK0	• Use a pull-up resistor (1 kΩ) during open drain output • Refer to Figure 5.	4.5 to 5.5	2			
		Low-level pulse width	tCKCY (2)			4.5 to 5.5		1/2tCKCY		
		High-level pulse width	tCKCY (2)			4.5 to 5.5		1/2tCKCY		
Serial input	Data set-up time		tICK	SI0	• Data set-up to SCK0 rising • Data hold from SCK0 rising • Refer to Figure 5.	4.5 to 5.5	0.1			µs
	Data hold time		tCKI			4.5 to 5.5	0.1			
Serial output	Output delay time (External serial clock)		tCKO(1)	SO0	• Use a pull-up resistor (1 kΩ) during open drain output. • Data set-up to SCK0 falling • Data hold from SCK0 falling • Refer to Figure 5.	4.5 to 5.5			7/12tCYC +0.2	µs
	Output delay time (Internal serial clock)		tCKO(2)			4.5 to 5.5			1/3tCYC +0.2	

5. Pulse Input Conditions at Ta = –30°C to +70°C, V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions	Ratings				Unit
				V_{DD} [V]	min	typ	max	
High/low level pulse width	tPIH(1) tPIL(1)	• INT0,INT1 • INT2/T0IN	• Interrupt acceptable • Timer0-countable	4.5 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3/T0IN (The noise rejection clock is selected to 1/1)	• Interrupt acceptable • Timer0-countable	4.5 to 5.5	2			
	tPIH(3) tPIL(3)	INT3/T0IN (The noise rejection clock is selected to 1/16)	• Interrupt acceptable • Timer0-countable	4.5 to 5.5	32			
	tPIL(4)	$\overline{RES}$	Reset acceptable	4.5 to 5.5	200			µs
	tPIH(5) tPIL(5)	$\overline{HS}$, $\overline{VS}$	Display position controllable Each active edge of $\overline{HS}$, $\overline{VS}$ must be more than 1tCYC. Refer to Figure 7.	4.5 to 5.5	10			tCYC
Rising/falling time	tTHL tTLH	$\overline{HS}$	Refer to Figure 7.	4.5 to 5.5			500	ns
Horizontal pull-in range	FH	$\overline{HS}$	The monitor point in Figure 10 is 1/2 V_{DD}.	4.5 to 5.5	15.23	15.73	16.23	kHz

6. A/D Converter Characteristics at Ta = –30°C to +70°C, V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions	Ratings				Unit
				V_{DD} [V]	min	typ	max	
Resolution	N			4.5 to 5.5	4			bit
Absolute precision	ET		(Note 3)	4.5 to 5.5		± 1/4	± 1/2	LSB
Conversion time	tCAD	From selecting Vref to resulting	1 bit conversion time = 2tCYC	4.5 to 5.5			1.96	µs
Reference current	I_{REF}		(Regulate the ladder resistor)	4.5 to 5.5		1.0	2.0	mA
Analog input voltage range	V_{AIN}	AN0 to AN3		4.5 to 5.5	V_{SS}		V_{DD}	V
Analog port input current	I_{AINH}		V_{AIN} = V_{DD}	4.5 to 5.5			1	µA
	I_{AINL}		V_{AIN} = V_{SS}	4.5 to 5.5	–1			

(Note 3) Absolute precision excepts quantizing error (±1/2 LSB).

7. Current Dissipation Characteristics at Ta = –30°C to +70°C , V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions	Ratings				Unit
				V_{DD} [V]	min	typ	max	
Current dissipation during basic operation (Note 4)	I_{DDOP}(1)	DVDD, AVDD	• FmCF = 12 MHz Ceramic resonator oscillation • FmLC = 14.11 MHz LC oscillation • System clock : CF oscillation • Internal RC oscillation stops	4.5 to 5.5		21	32	mA
Current dissipation in HALT mode (Note 4)	I_{DDHALT}(1)	DVDD, AVDD	• HALT mode • FmCF = 12 MHz Ceramic resonator oscillation • FmLC = 0 Hz (oscillation stops) • System clock : CF oscillation • Internal RC oscillation stops.	4.5 to 5.5		5	10	mA
	I_{DDHALT}(2)	DVDD, AVDD	• HALT mode • FmCF = 0 MHz (oscillation stops) • FmLC = 0 Hz (oscillation stops) • System clock : Internal RC	4.5 to 5.5		400	800	µA
Current dissipation in HOLD mode (Note 4)	I_{DDHOLD}	DVDD, AVDD	• HOLD mode • All oscillation stops.	4.5 to 5.5		0.05	20	µA

(Note 4) The currents of the output transistors and the pull-up MOS transistors are ignored.

Oscillation type	Manufacturer	Oscillator	C1	C2
12 MHz ceramic resonator oscillation	Murata	CSA12.0MTZ	33 pF	33 pF
		CST12.0MTW	on chip	
	Kyocera	KBR-12.0M	47 pF	47 pF

* Both C1 and C2 must use an K rank (±10%) and an SL characteristics.

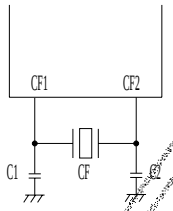
Table 1. Ceramic Resonator Oscillation Guaranteed Constant (main-clock)

Oscillation type	L	C3	C4
14.11 MHz LC oscillation	5.6 μH	27 pF	30 pF (Trimmer)
	4.7 μH ± 10% (Variable)	27 pH	27 pH

* See Figure 11,12.

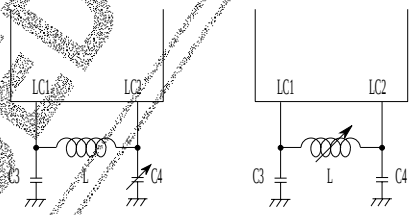
Table 2. LC Oscillation Guaranteed Constant (OSD clock)

(Notes)
- Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length.
- If you use other oscillators than those shown above, we provide no guarantee for the characteristics.
- Adjust the voltage of monitor point in Figure 10 to $1/2V_{DD} \pm 10\%$ by the LC oscillation constant 'L' or 'C' to lock the PLL circuit.



Main clock

Figure 1 Ceramic Resonator Oscillation



OSD clock

Figure 2 LC Resonator Oscillation

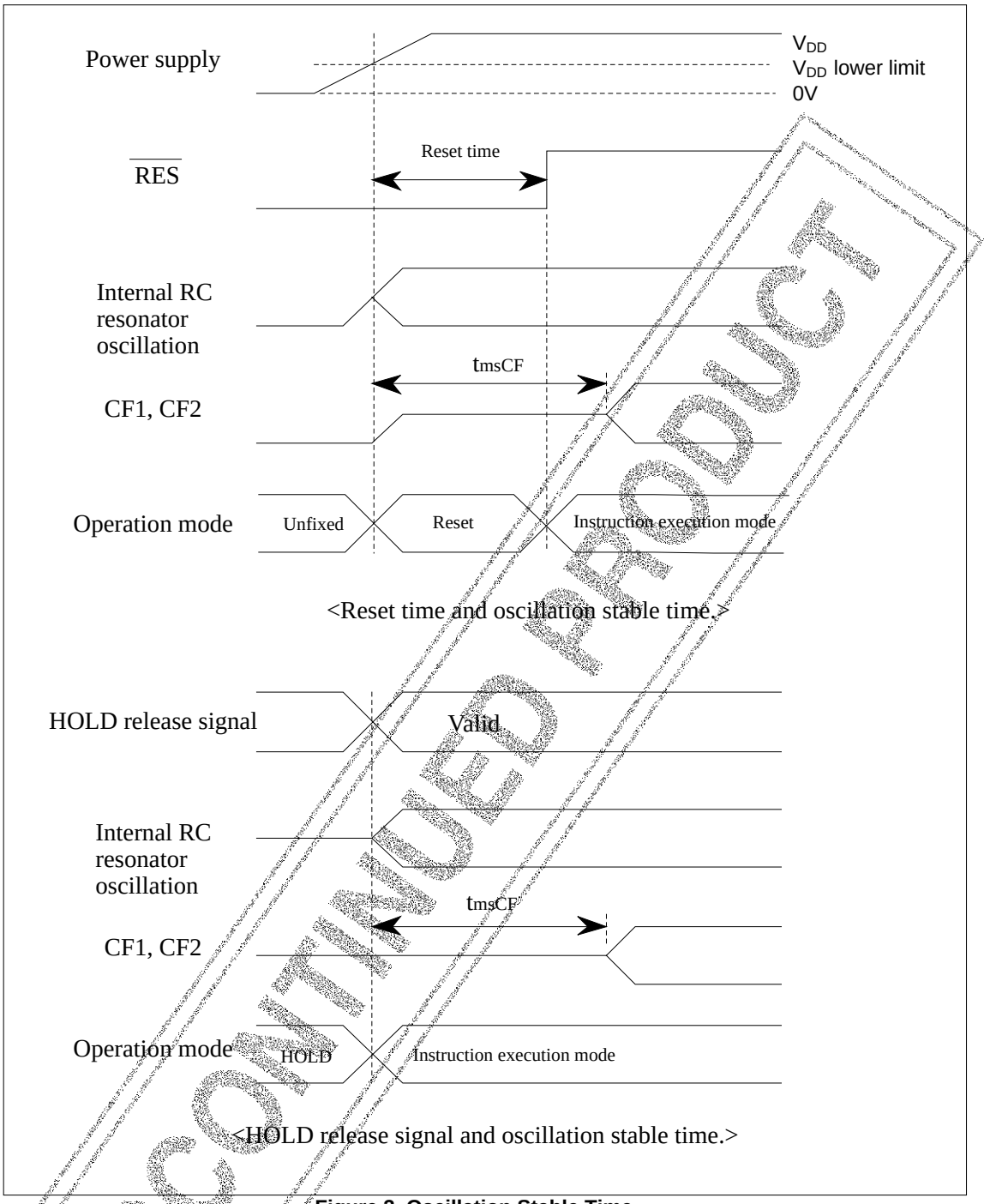
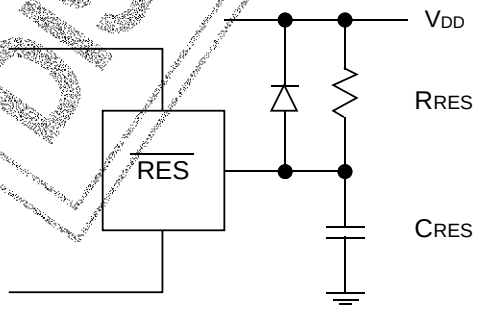


Figure 3 Oscillation Stable Time



(Note) Set the values of C_{RES}, R_{RES} so that the reset time is 200 μs or longer.

Figure 4 Reset Circuit

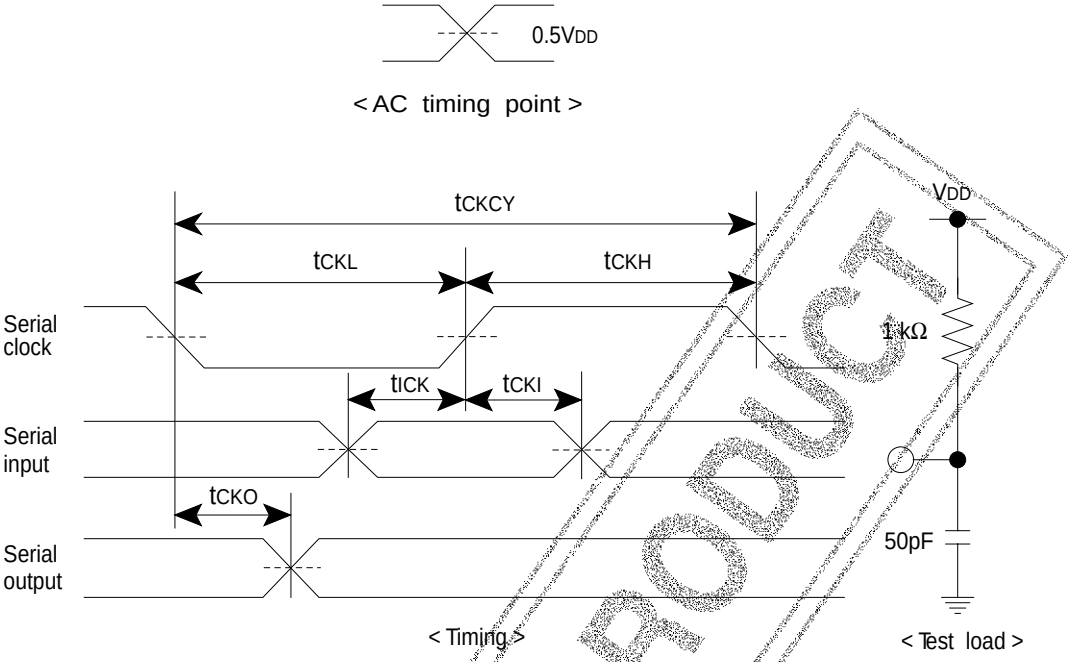


Figure 5 Serial Input/output Test Condition

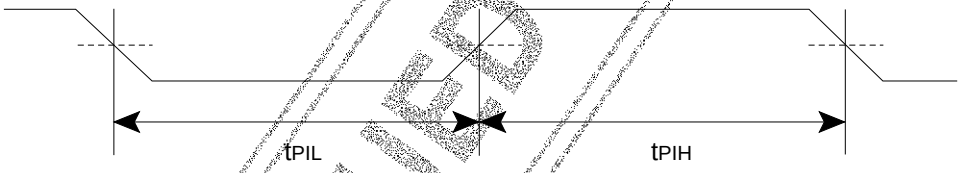
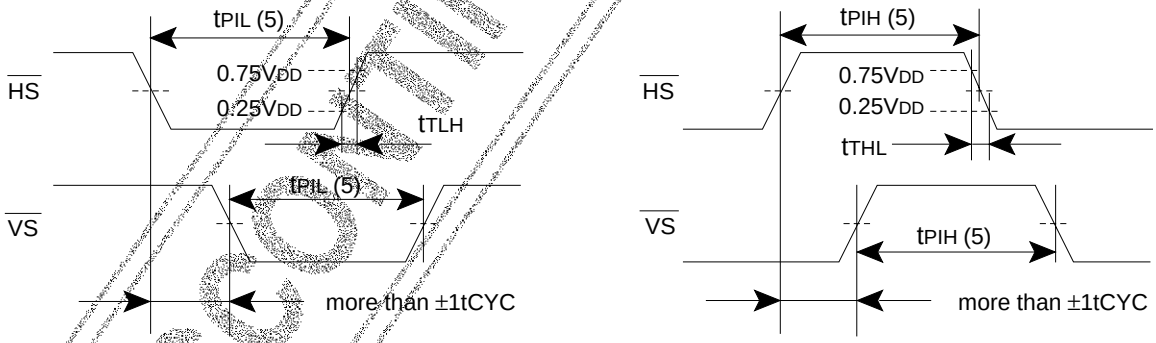


Figure 6 Pulse Input Timing Condition - 1



(a) In case of active low (b) In case of active high

Figure 7 Pulse Input Timing Condition - 2

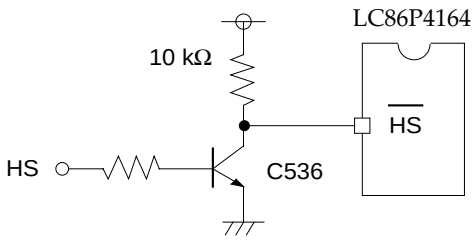


Figure 8 Recommended Interface Circuit

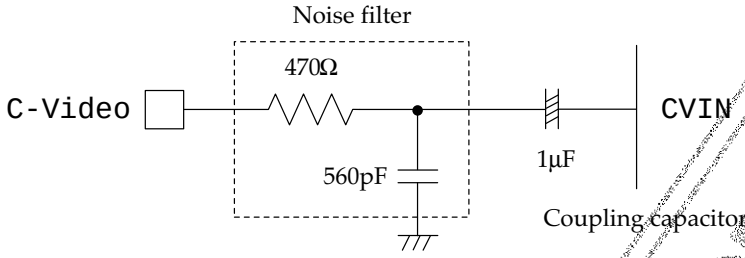


Figure 9 CVIN Recommended Circuit

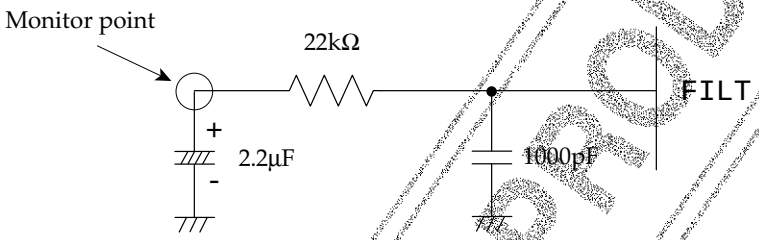


Figure 10 FILT Recommended Circuit

(Note) • Place the parts connected to the FILT terminal at the shortest pattern length possible on the board.

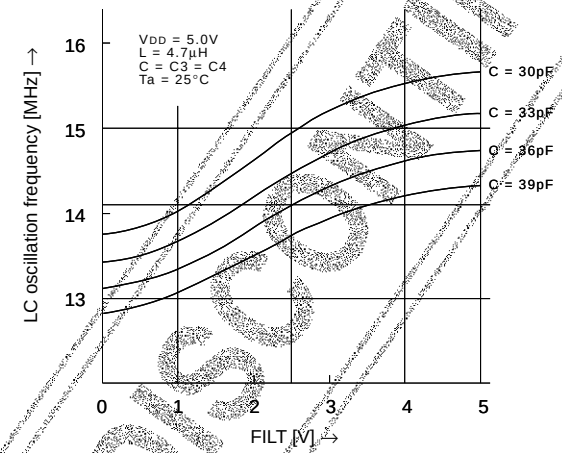


Figure 11 FILT-LC Oscillation Frequency (1)

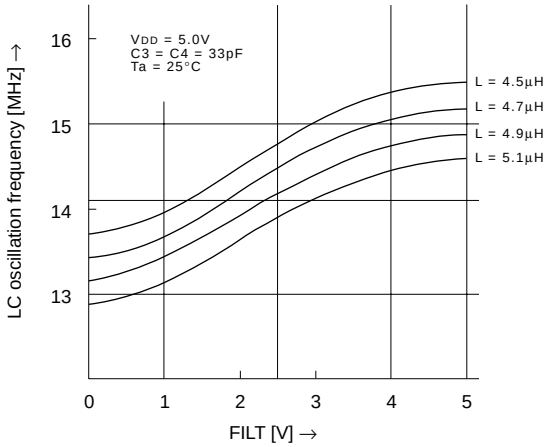


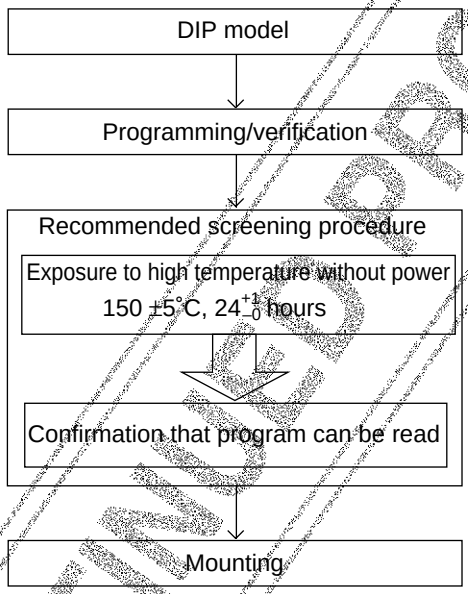
Figure 12 FILT-LC Oscillation Frequency (2)

Requirements Prior to Mounting

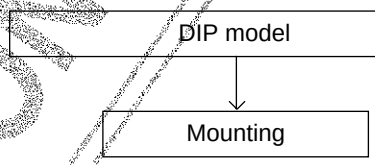
Notes on Handling

- The construction of one-time microcontrollers in which the PROM is not programmed precludes Sanyo from fully testing them before they are shipped. The screening procedure described below is recommended in order to attain higher reliability after programming the PROM.
- The nature of one-time microcontrollers in which the PROM is not programmed precludes us from fully testing them by writing all of the bits. Therefore, it is not possible for us to guarantee a write yield of 100%.
- Storage in moisture-proof packaging (unopened)
  While they are still in the moisture-proof packaging, these devices should be stored at a temperature of 30˚C and a humidity of no more than 70%.
- After opening the moisture-proof packaging
  These devices should be mounted and soldered as soon as possible after the moisture-proof packaging is opened. Once the moisture-proof packaging is opened, the devices should be stored at a temperature of 30˚C and a humidity of no more than 70% for no more than 96 hours.

a. In the case of models that are programmed by the user (models that are shipped with the PROM not programmed)



b. Requirements prior to mounting for models that are programmed by Sanyo (models that are shipped with the PROM already programmed)



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