Integrated Device Technology, Inc.

NICStAR Evaluation Board for IDT77211 PCI Segmentation and Reassembly Controller

ADVANCE INFORMATION
IDT77911

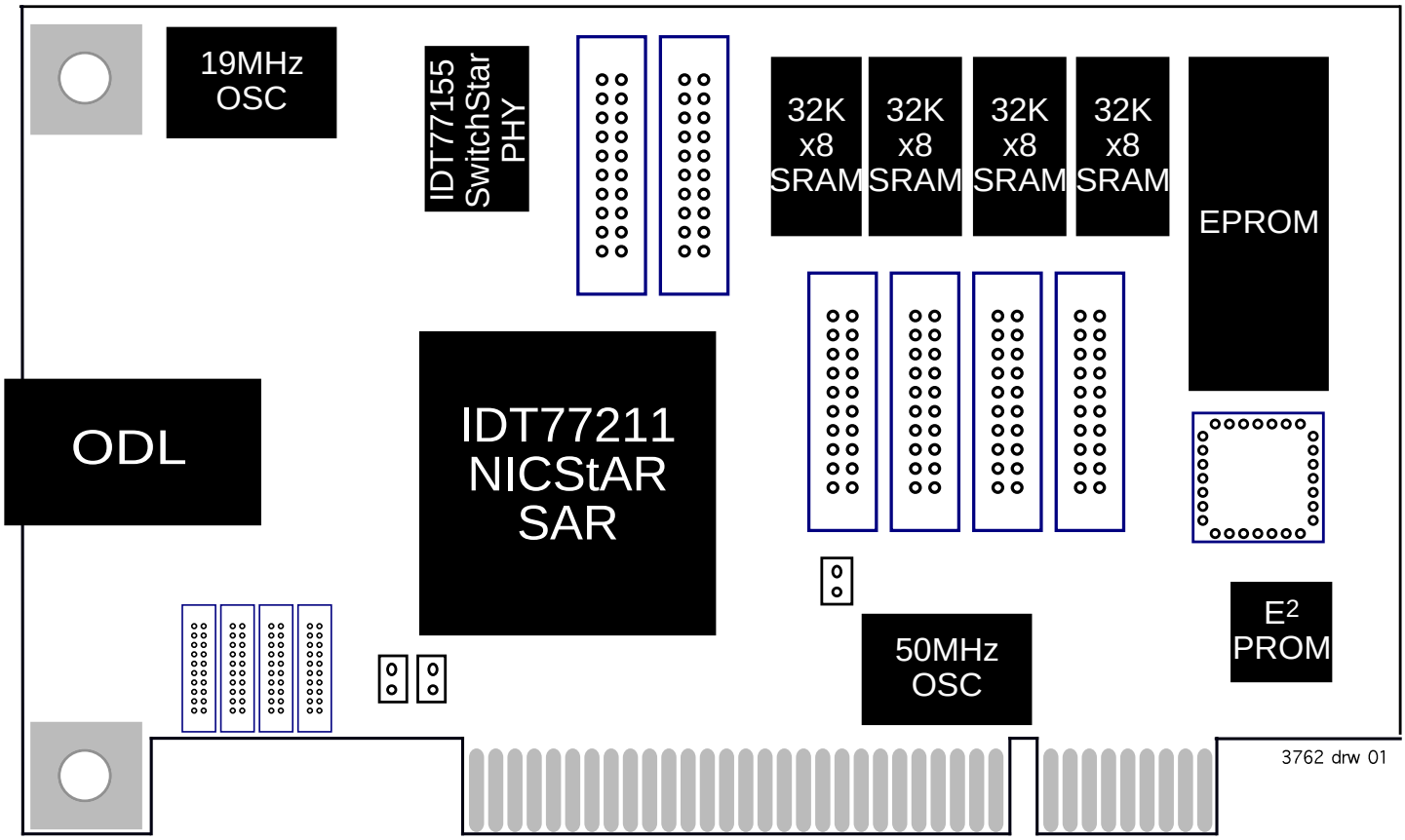
FEATURES:

- Complete 155Mbps PCI-bus ATM Network Interface Card
- Complete reference design including schematics, bill of materials, and theory of operation
- Connectors for logic analyzers and oscilloscopes
- Supports 33MHz, 32-bit PCI 2.0 bus
- 155Mbps Multimode fiber optical interface
- Complete reference design including schematics, bill of materials, and data bases needed for production.
- Capable of supporting up to 16K receive connections
- Supports tens of thousands of transmit connections
- E^2 PROM layout for Sub-vendor ID
- "SARWIN" software evaluation program available for Windows 3.1™
- Third Party Software available:
  - Telogy Networks
    Windows NT™ Drivers and other Windows Drivers
    21 Firstfield Road, Gaithersburg, Maryland 20878
    (301) 527-2788 (phone) (301) 417-0324 (FAX)
    hluterman@telogy.com
  - Harris & Jefferies
    Novel Netware™ Drivers
    888 Washington Street, Dedham,
    Massachusetts, 02026
    (617) 329-3200 (phone) (617) 329-4148 (FAX)
    chrisb@hjinc,com
  - Advancenet Systems Inc.
    Windows NT™ and Windows 95™ Drivers
    406 Timbermill Rd., Durham, North Carolina 27713
    (919) 544-5601 (phone) (919) 544-4601 (FAX)
    j.harford@ieee.org or
    75141,2635@compuserve.com

DESCRIPTION:

The IDT77911 is designed to provide a stable reference platform for evaluation, design, and test of IDT's 77211 Segmentation and Reassembly controller. The IDT77911 provides a fiber media physical (PHY) interface. The IDT77911 features complete PCI-bus ATM NIC functionality, plugging directly into PCI bus expansion slots.Test points, including sockets for logic analyzer and oscilloscope probes are provided on all buses. These connectors may be used for simple

FUNCTIONAL BLOCK DIAGRAM



probing into all buses and active signals lines for hardware and/or software design, verification, and debugging operations.

FUNCTIONAL OVERVIEW

COMPATIBILITY AND CONFIGURATION

The board is designed for use in PCI systems, which may include PC compatibles, MIPS, Alpha, Windows NT systems, future PowerPC Macintosh systems, and so on. It supports the 32 bit, 33 MHz, 5V part of the PCI spec, although this also permits operation in a 64-bit, 33 MHz, 5V PCI slot.

OVERVIEW

The heart of the board is the IDT 77211 NICStAR, which is an ATM Segmentation And Reassembly (SAR) controller. The NICStAR connects directly to the PCI bus, a private SRAM/EPROM bus, and the Utopia PHY interface. The PHY device is an IDT77155. The PHY device connects in turn to a Hewlett-Packard HFBR-5103 Optical Data Link (ODL) device for the fiber optic connection. The ODL incorporates its own fiber optic connectors.

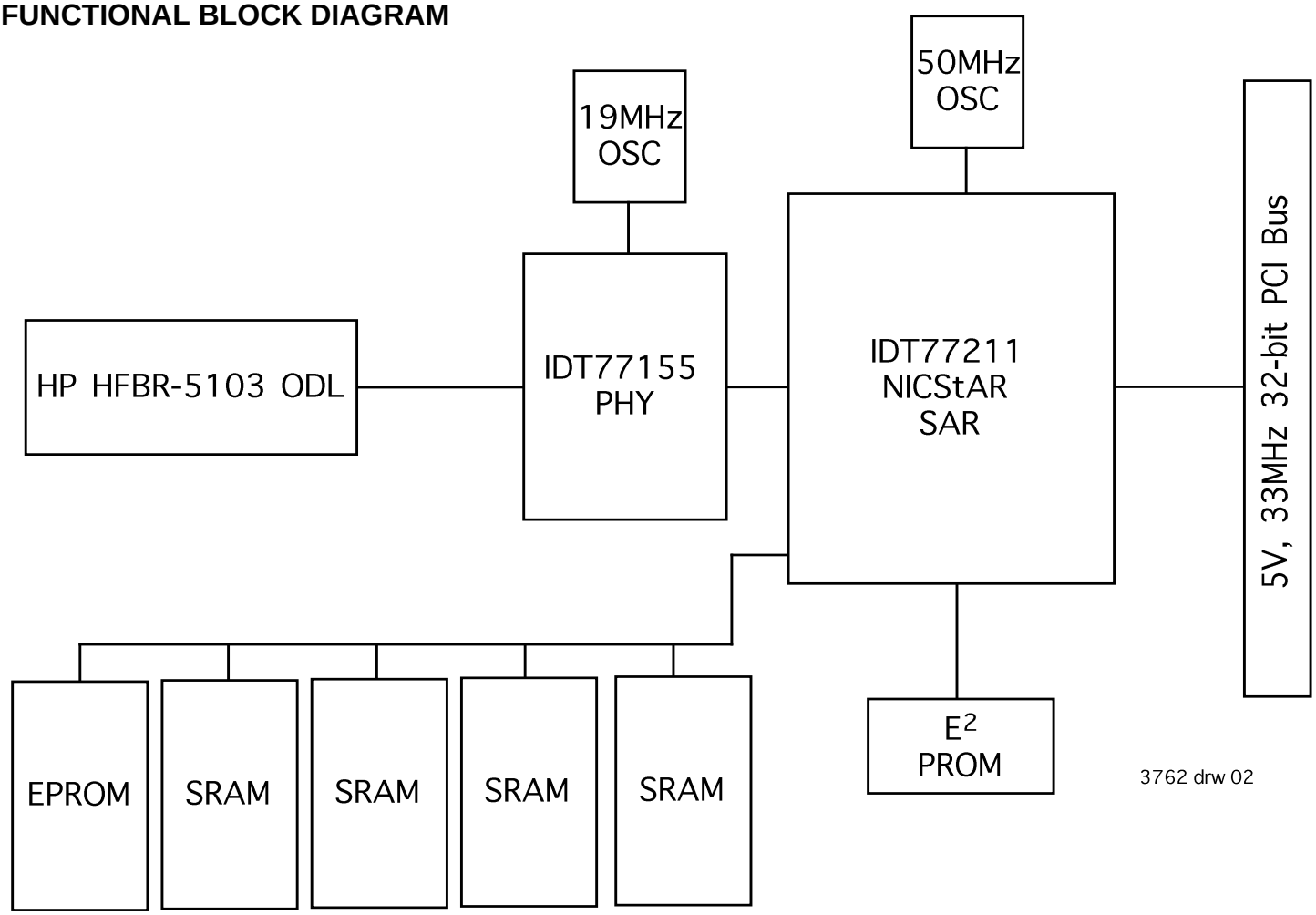
THEORY OF OPERATION

The NICStAR has 50 signal pins which connect directly to the PCI bus edge connector. 32 of these are multiplexed address/data signals, and the remainder are control signals. The NICStAR is compatible with the 5V, 33 MHz portion of the PCI spec, so the eval board will work in motherboards with 32 or 64 bit, 5V, 33 MHz slots. The board will not work in 3.3V slots.

The 77911 connects the PCI bus PRSNT1# and PRSNT2# pins to ground; R59 (see schematic) is provided between the PCI bus RST# signal and the NICStAR's RST# input to facilitate testing. This resistor is normally 0 Ohms but it could be removed, and the pads used to insert some sort of AND gate to allow the NICStAR to be reset without resetting the host computer.

The NICStAR receives two clock input signals. One is from the PCI bus, and this one can vary from DC to 33.333MHz. The other is from a local oscillator on the 77911. U14 is the NICStAR's main clock: SAR_CLK. It runs typically at 50 MHz. The rate of the Utopia interface, PHY_CLK is connected to a

FUNCTIONAL BLOCK DIAGRAM



devide by 2 output clock from the SAR. Optionally, this clock can be supplied via a separate osallator, U15, PHY clock and runs typically at 25 MHz. All clock oscillators on the board have ferrite-bead power supply filters, and both SAR oscillator sockets have 33 Ohm source series and 330/220 Ohm end parallel termination resistors provided for optimum signal integrity.

The NICStAR has a private local SRAM/EPROM data bus, SR_I/O[31:0] and address bus, SR_A[16:0]. It also supports a four-wire private EEPROM bus, three of which are outputs (EE_SCLK, EE_CS#, EE_DO) and one of which is an input (EE_DI).

NICStAR supports 4 32Kx8 or 128Kx8 asynchronous SRAMS. SRAM timing is fixed at one cycle. The NICStAR spec requires 20 ns access time SRAMs when the NICStAR is running at 50 MHz. When 32Kx8 devices are installed, R64-R67 should be 0 Ohms. When 128Kx8 devices are installed, R64-R67 should be 1K Ohms.

NICStAR supports 1 32Kx8 or 128Kx8 EPROM. EPROM timing is fixed at three cycles. NICStAR requires a 70 ns access time EPROM.

NICStAR supports 1 EEPROM device. The four EEPROM signals are completely under software control, so access times and protocols can be specified by the user. The eval board uses a Xicor X25020 EEPROM. This device requires EE_CS# to be asserted low during all operations. Control or data bits are taken from EE_DO at the rising edge of EE_SCLK, and EE_DI changes on the falling edge of EE_SCLK. Refer to the X25020 documentation for more information. The 77911 provides LEDs on EE_DO (D6) and EE_SCLK (D5). These LEDs illuminate when the corresponding signal is asserted low, and may be used to signal status to the user when the EEPROM is not being accessed.

The NICStAR has a multiplexed utility bus, UTL_AD[7:0] plus five UTL control signals. This bus may be used to communicate with external 8-bit devices. The 77911 uses the utility bus in this way to communicate with the registers on the PHY. This interface is also under software control, so protocol can be specified by the user.

The last two buses on the NICStAR are the UTOPIA transmit and receive buses. These follow the ATM Forum's specification of the UTOPIA interface. They run at the PHY_CLK speed, with the NICStAR generating the TXCLK and RXCLK signals to the PHY device.

The PHY device used is the IDT77155 SWITCHStAR™. It has the standard transmit and receive UTOPIA or SDH interfaces, and a non-multiplexed utility bus for register access. The PHY utility data bus and address bus are connected together on the eval board; the NICStAR™ ALE signal defines the mode of this combined bus in a way compatible with the IDT77211 NICStAR™ and the IDT77155 SWITCHStAR™.

The IDT77155 reset input is driven by the NICStAR's PHY_RST# input, and R61 is provided to allow this reset signal to be driven by external logic. Normally a 0 Ohm resistor is used in this location, but it could be removed or simply replaced by a 33 Ohm resistor to allow the PHY's reset input to be driven without a direct conflict with the NICStAR's PHY_RST# output. IDT's 77155 also provides an INT# output which is connected to the NICStAR's PHY_INT# input.

The 77155 transmit and receive clock reference frequency is provided by U1, a 19.44 MHz oscillator. This device is specified at 10 ppm accuracy to meet the ATM Forum requirements for 155.52 Mbps operation. As with the other oscillators on the eval board, this oscillator has a ferrite-bead power supply filter, and a 33 Ohm source series termination resistor. End termination is provided as part of a voltage divider network designed to limit the input swing at the AC-coupled RRCLK and TXCLK inputs on the 77155.

The 77155 has several control signals which are connected to pullup and/or pulldown resistors on the eval board. Refer to the 77155 documentation and the 77911 schematics for more details. There are also several status outputs which are not connected. One status output, RALM, goes high when any of several different error conditions are detected by the PHY. It is low only when a signal is present on the receive data inputs, the 77155 is able to recover a valid clock from the signal, and the data on the signal contains proper SONET or SDH frames. RALM is connected to an LED (D4) to act as a "link detect" indicator.

The clock recovery circuitry for the IDT77155 is aided by a filter circuit. On the 77911, this circuitry consists of C61, C62, R50, R45, R47, and U11. Special isolated analog ground and power planes are provided on the 77911 layout to help this circuitry work better.

The eval board contains a linear regulator, U10, to use the +12V supply on the PCI bus to drive the isolated +5V analog power plane. If R35 is installed and U10 is removed, the regular VCC plane is connected to the analog power plane instead.

IDT's 77155 has a six-wire connection to the physical media devices (PMD) which consists of three pairs of PECL-level differential signals. One pair is transmit data, one pair is receive data, and the last pair is signal detect, which can also be connected as a single-ended PECL or CMOS signal. The 77911 provides the PMD connection for the fiber interface. It also includes extensive termination circuitry with several possible configurations to provide the best possible signal integrity between the PHY and the PMD.

77911

The 77911 interface is provided via U9, a 9-pin fiber optical data link (ODL) footprint which can be loaded with any standard 9-pin ODL device. The 77911 is loaded with the

Hewlett-Packard HFBR-5103, which is a short-haul device for multimode fiber, originally designed for FDDI. Other devices in the HFBR-510x and -520x families should also work here, depending on the application. An extra row of 7 ground pins is provided next to the U9 pins to provide ground points for oscilloscope probes.

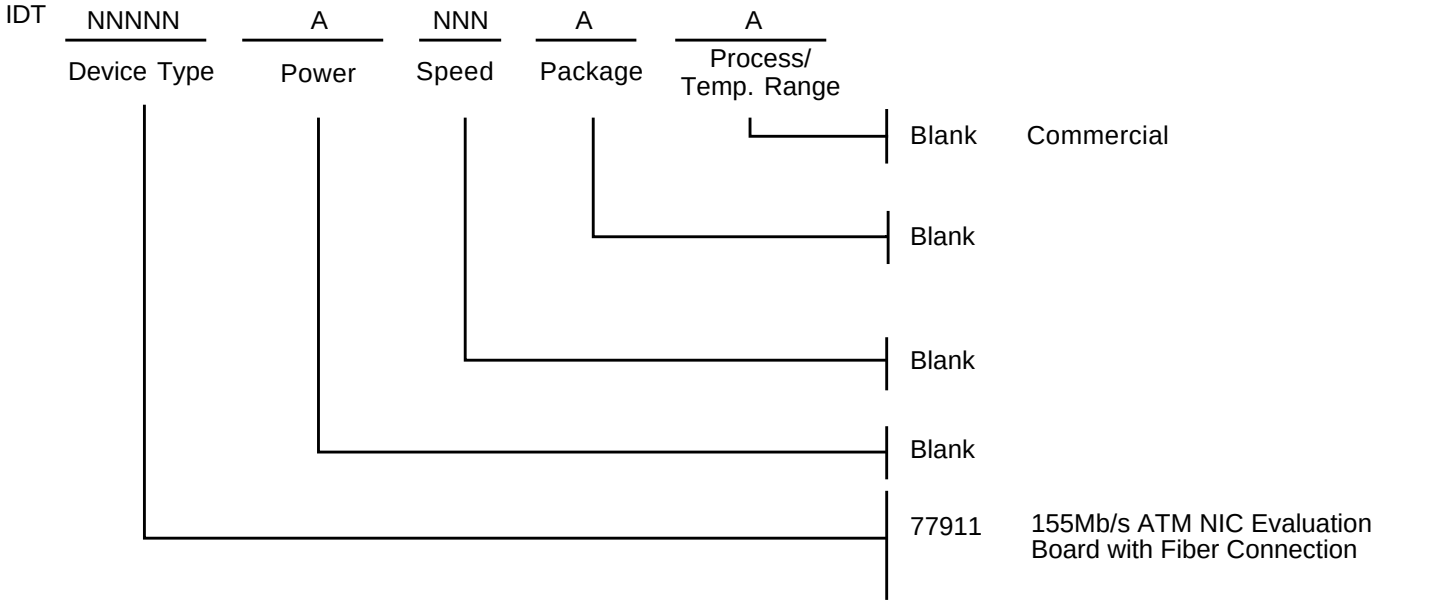
Note that compatibility with the physical layer of the 51.84 Mbps ATM spec is not provided by design in this board. This spec requires Category 3 UTP cable and a different physical media interface than the fiber interface on this board. However, the 77911 does allow the 77155 to support the 51.84 Mbps rate by using different components for the transmit/receive clock oscillator and loop filter, and this allows the 77911 to be used to test the SAR's own support for the 51.84 Mbps rate. Interoperability with other 51.84 Mbps ATM devices using the correct physical media interface is possible but not guaranteed.

The 77911/2 provides many test points for Hewlett-Packard logic analyzer termination adapters and two-pin analog oscilloscope probes such as those used on the Tektronix TLS-216 oscilloscope. J3-J8 are 20-pin headers in the configuration required by the HP termination adapters, and TP1-TP14 are two-pin headers where pin 1 is the signal and pin 2 is ground. The pins of U9 can also be used as oscilloscope test points as described above.

Two SOIC footprints, U18 and U19, for either 0.15" or 0.3" body width devices are provided as spare IC positions; the PHY_CLK synchronization circuit normally occupies U19. U16 is a spare footprint for a PLCC-28 package, such as a 22V10 GAL. A large through-hole prototyping area is provided at the right end of the fab. All of the through-holes on the top, right, and bottom edges of this area are bussed together on the bottom of the board and connected to the internal ground plane, which is also connected to the ground plane on the rest of the board. The through-holes just inside the grounded through-holes are also bussed together, on the top side of the board, and connected to the internal power plane. However, the power plane under the prototyping area is NOT internally connected to the power plane on the rest of the board, and must be connected externally if required. This allows the PC board to be cut in half along the dotted line on the bottom side of the board without risk of the exposed edges of the power and ground planes shorting together.

Other special features-- the EPROM, EEPROM, oscillator, and ODL through-hole devices may all be socketed. The oscillators may have the "8-pin" half-size or the "14-pin" full-size footprint, and a special ground plane is provided on the top side of the board to minimize radiated EMI. The ODL socket must have flush-mount socket pins for mechanical reasons. Through-hole size was specified for the Mill-Max 0552-2-15-01-11-14-10-0 socket pin, though other socket pins will work here. The pads for the NICStAR, U13, were designed to work with the AMP 824160-1 QFP-208 socket, which allows a CQFP-208 or PQFP-208 device to be socketed into a QFP-208 footprint (this eliminates the need for a redundant PGA footprint, as other QFP-208 sockets require).

ORDERING INFORMATION



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ADVANCE INFORMATION DATASHEET: DEFINITION

"Advance Information" datasheets contain initial descriptions, subject to change, for products which are in development, including features and block diagrams.

Datasheet Document History

1/15/97: Initial Draft

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