Integrated Circuit Systems, Inc.

ICS9148-49

# Pentium/Pro™ System Clock Chip

General Description

The **ICS9148-49** is part of a reduced pin count two-chip clock solution for designs using an Intel BX style chipset. Companion SDRAM buffers are ICS9179-03, -04 and -12.

There are two PLLs, with the first PLL capable of spread spectrum operation. Spread spectrum typically reduces system EMI by 8-10dB. The second PLL provides support for USB 48MHz requirements. CPU frequencies up to 100MHz are supported.
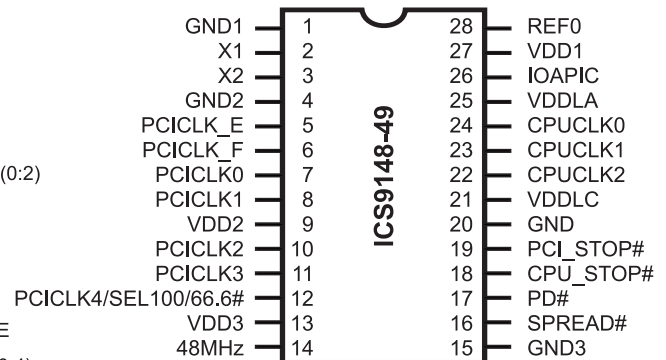
Features

- 3 CPUs @2.5V, up to 100MHz.
- 7 PCIs @3.3V (including 1 free running, 1 Early).
- 1-48MHz(@3.3V) fixed.
- 1 REF(3.3V, 14.318MHz), 1 IOAPIC(2.5V, 14.318MHz)
- Strong REF clock (1V/ns @ 50pf load)
- Excellent power management features including Power down, PCI and CPU stops
- Spread Spectrum for EMI control(0.5% down spread)
- Early PCI (3.0ns ±250ps)

Block Diagram
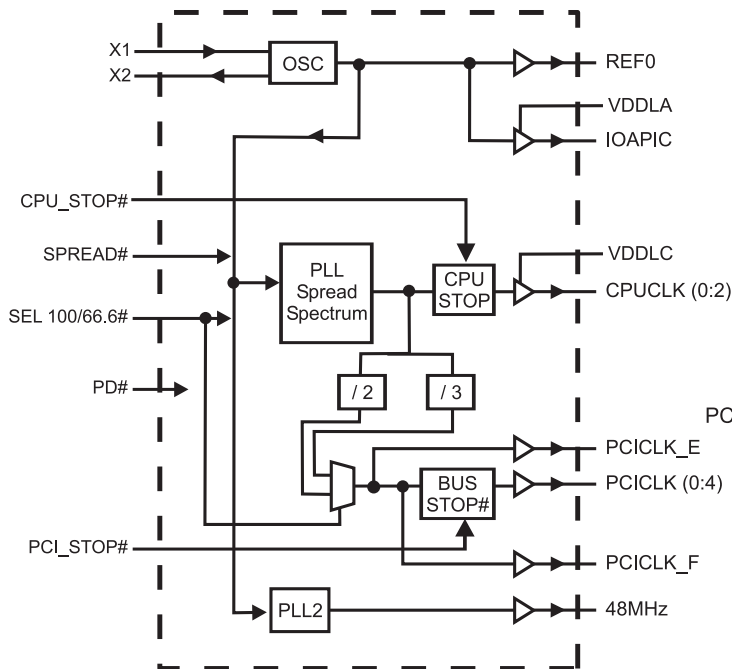
Pin Configuration

28-pin SSOP (209mil body)

Power Groups

VDD1=REF0, X1, X2
VDD2=PCICLK_E, PCICLK_F, PCICLK(0:4)
VDD3=48MHz
VDDLC=CPUCLK(0:2)
VDDLA=IOAPIC

Ground Groups

GND1=REF0, X1, PLL CORE, X2, IOAPIC
GND2=PCICLK_E, PCICLK_F, PCICLK(04)
GND=CPUCLK
GND3=48MHz

Frequency Table:

SEL 100/66.6#	CPU MHz	PCI MHz
1	100	33.3
0	66.6	33.3

Pin Descriptions

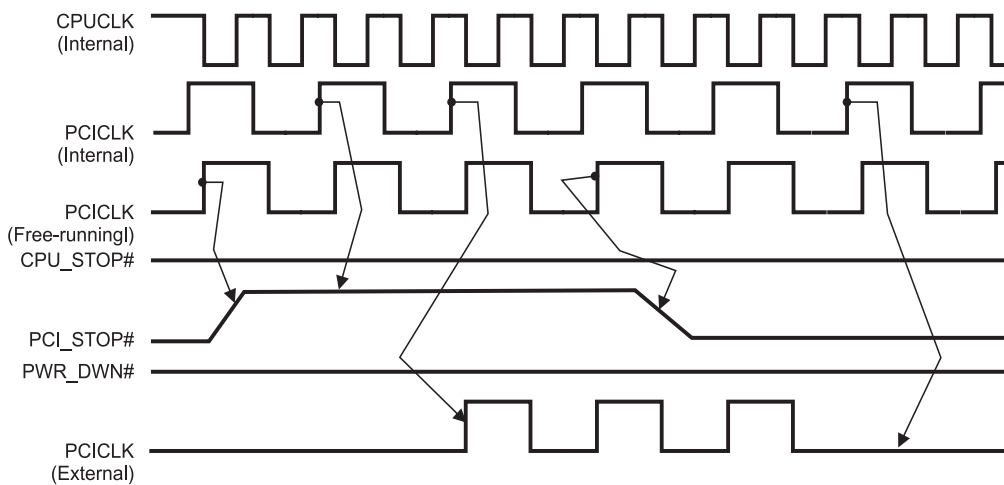| PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	GND1	PWR	Ground for REF outputs, X1, X2.
2	X1	IN	XTAL_IN 14.318MHz Crystal input, has internal 33pF load cap and feed back resistor from X2
3	X2	OUT	XTAL_OUT Crystal output, has internal load cap 33pF
4	GND2	PWR	Ground for PCI outputs
5	PCICLK_E	OUT	Early PCICLK. Leads PCICLK (0:4,_F) by 2ns ±250ps. Not affected by PCI_STOP#
6	PCICLK_F	OUT	Free Running PCI output. oNot affected by PCI_STOP#
7,8,10,11	PCICLK (0:3)	OUT	PCI clock outputs. TTL compatible 3.3V
9	VDD2	PWR	Power for PCICLK outputs, nominally 3.3V
12	PCICLK_4	OUT	PCI clock output. TTL compatible 3.3V
	SEL100/66.6#	IN	Select pin for enabling 100MHz or 66.6MHz H=100MHz, L=66.6MHz (PCI always synchronous 33.3MHz)
13	VDD3	PWR	Power for 48MHz
14	48MHz	OUT	Fixed CLK output @ 48MHz
15	GND3	PWR	Ground for 48MHz
16	SPREAD#	IN	Turns on Spread Spctrum when active. 0.5% down spread.1
17	PD#	IN	Powers down chip. Internal PLLs, all output are turned off.
18	CPU_STOP#	IN	Halt CPUCLK (2:0) at logic "0" level when input is low.
19	PCI_STOP#	IN	Halts PCICLK (0:4) at logic "0" level when input low. Does not affect PCICLK_E 7 PCICLK_F
20	GND	PWR	Ground for PLL core
21	VDDLC	PWR	Power for CPU outputs, nominally 2.5V
22,23,24	CPUCLK (2:0)	OUT	CPU and Host clock outputs nominally 2.5V
26	IOAPIC	OUT	IOAPIC clock output 14.318MHz.
25	VDDLA	PWR	Power for IOAPIC
27	VDD1	PWR	Power for REF outputs.
28	REF0	OUT	14.318MHz clock output/Latched input at power up.

CPU_STOP# Timing Diagram

CPUS_TOP# is an asychronous input to the clock synthesizer. It is used to turn off the CPUCLKs for low power operation. CPU_STOP# is synchronized by the **ICS9148-49**. All other clocks will continue to run while the CPUCLKs clocks are disabled. The CPUCLKs will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPUCLK on latency is less than 4 CPUCLKs and CPUCLK off latency is less than 4 CPUCLKs.

INTERNAL CPUCLK

PCICLK (0:4)

CPU_STOP#
PCI_STOP# (High)
PD# (High)
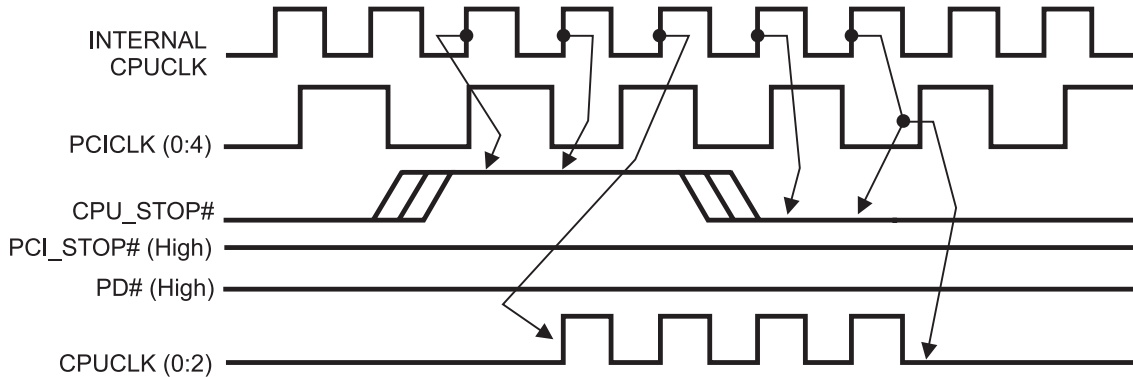
CPUCLK (0:2)

Notes:
1. All timing is referenced to the internal CPUCLK.
2. CPU_STOP# is an asynchronous input and metastable conditions may exist.
   This signal is synchronized to the CPUCLKs inside the **ICS9148-49**.
3. All other clocks continue to run undisturbed including SDRAMR.
4. PD# and PCI_STOP# are shown in a high (true) state.

PCI_STOP# Timing Diagram

PCI_STOP# is an asynchronous input to the **ICS9148-49**. It is used to turn off the PCICLK (0:5) clocks for low power operation. PCI_STOP# is synchronized by the **ICS9148-49** internally. PCICLK (0:5) clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK (0:5) clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.

CPUCLK (Internal)

PCICLK (Internal)

PCICLK (Free-runningl)
CPU_STOP#

PCI_STOP#
PWR_DWN#

PCICLK (External)

Notes:
1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9148 device.)
2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS9148.
3. All other clocks continue to run undisturbed.
4. PD# and CPU_STOP# are shown in a high (true) state.

PD# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal is synchronized internal by the **ICS9148-49** prior to its control action of powering down the clock synthesizer. Internal clocks will not be running after the device is put in power down state. When PD# is active (low) all clocks are driven to a low state and held prior to turning off the VCOs and the Crystal oscillator. The power on latency is guaranteed to be less than 3 mS. The power down latency is less than three CPUCLK cycles. PCI_STOP# and CPU_STOP# are don't care signals during the power down operations.
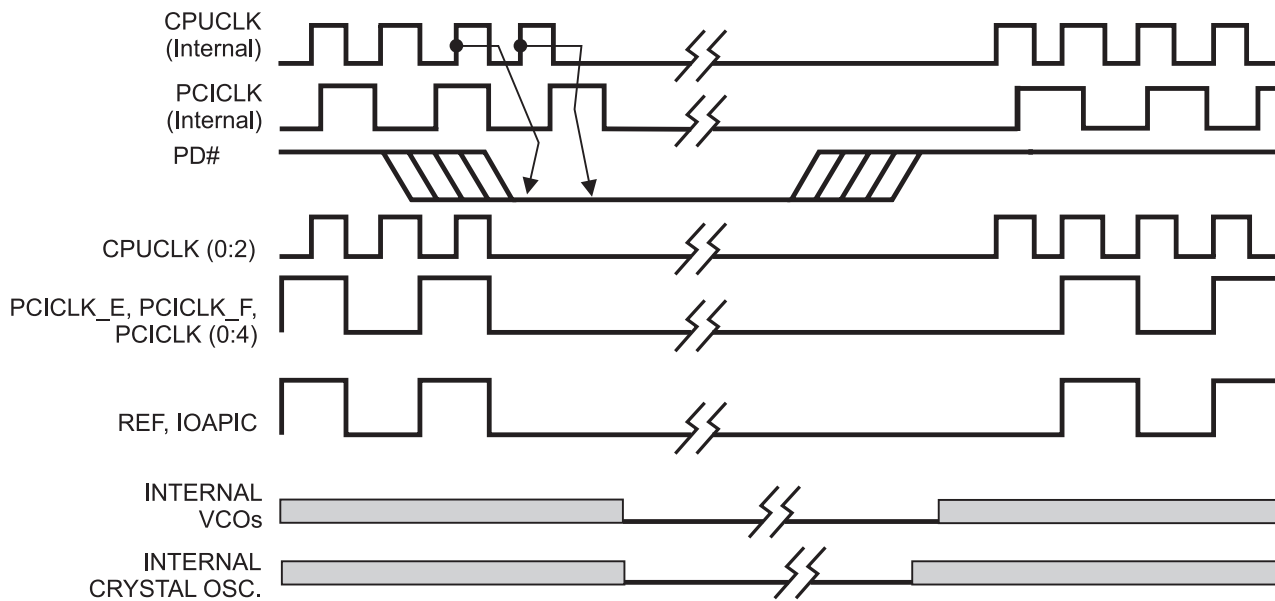

Notes:
1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9148 device).
2. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside the ICS9148.
3. The shaded sections on the VCO and the Crystal signals indicate an active clock is being generated.

Absolute Maximum Ratings

Supply Voltage . . . . 7.0 V

Logic Inputs . . . . GND –0.5 V to V_{DD} +0.5 V

Ambient Operating Temperature . . . . 0°C to +70°C

Storage Temperature . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = V_{DDL} = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}		0.1	5	μA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5	2.0		μA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200	-100		μA
Operating Supply Current	$I_{DD3.3OP}$	C_L = 0 pF; 66.6 MHz		70	100	mA
		C_L = 0 pF; 100 MHz		75	100	
Input frequency	F_i	V_{DD} = 3.3 V;	12	14.318	16	MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27	36	45	pF
Transition Time[1]	T_{trans}	To 1st crossing of target Freq.			3	ms
Settling Time[1]	T_s	From 1st crossing to 1% target Freq.			2	ms
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	ms

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current	$I_{DD2.5OP}$	C_L = 0 pF; 66.8 MHz		17	50	mA
		C_L = 0 pF;133 MHz		27	50	
Power Down Current	$I_{DD2.5OPD}$			5	100	μA
Skew[1]	$T_{CPU-PCI(F,0:4)}$	V_T = 1.5 V / 1.25V; CPU leads	1.5	3	4	ns
	$T_{CPU-PCI(E)}$	VT = 1.5 V / 1.25V; PCI leads	180	200	250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPU

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	VOH2B	I_{OH} = -12 mA	2	2.2		V
Output Low Voltage	VOL2B	I_{OL} = 12 mA		0.3	0.4	V
Output High Current	IOH2B	V_{OH} = 1.7 V		-20	-16	mA
Output Low Current	IOL2B	V_{OL} = 0.7 V	19	26		mA
Rise Time	tr2B[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V		1.2	1.6	ns
Fall Time	tf2B[1]	V_{OH} = 2.0 V, V_{OL} = 0.4 V		1.2	1.6	ns
Duty Cycle	dt2B[1]	V_T = 1.25 V	45	50	55	%
Skew	tsk2B[1]	V_T = 1.25 V		60	175	ps
Jitter, Single Edge Displacement[2]	tjsed2B[1]	V_T = 1.25 V		200	250	ps
Jitter, One Sigma	tj1s2B[1]	V_T = 1.25 V		65	150	ps
Jitter, Absolute	tjabs2B[1]	V_T = 1.25 V	-300	160	300	ps

[1] Guaranteed by design, not 100% tested in production.

[2] Edge displacement of a period relative to a 10-clock-cycle rolling average period.

Electrical Characteristics - PCI

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-10%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -11 mA	2.6	3		V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA		0.2	0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V		-30	-22	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	16	25		mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.7	2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.6	2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	51	55	%
Skew	t_{sk1}[1]	V_T = 1.5 V		200	500	ps
Jitter, Single Edge Displacement[2]	tjsed2B[1]	V_T = 1.25 V		200	500	ps
Jitter, Absolute[1]	tab_{s1a}	V_T = 1.5 V			200	ps
	t_{jabs1b}	V_T = 1.5 V	-250		250	ps

[1] Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF0

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-10%; C_L = 50 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -12 mA	2.6	2.7		V
Output Low Voltage	V_{OL5}	I_{OL} = 9 mA		0.3	0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V		-32	-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16	25		mA
Rise Time	t_{r5}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.2	2	ns
Fall Time	t_{f5}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.1	2	ns
Duty Cycle	d_{t5}[1]	V_T = 1.5 V	53	54	55	%
Jitter, One Sigma	t_{j1s5}[1]	V_T = 1.5 V		1	3	%
Jitter, Absolute	t_{jabs5}[1]	V_T = 1.5 V	-5	-	5	%

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - IOAPIC

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-10%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	VOH2B	I_{OH} = -12 mA	2	2.2		V
Output Low Voltage	VOL2B	I_{OL} = 12 mA		0.3	0.4	V
Output High Current	IOH2B	V_{OH} = 1.7 V		-20	-16	mA
Output Low Current	IOL2B	V_{OL} = 0.7 V	19	26		mA
Rise Time	tr2B[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V		1.2	1.6	ns
Fall Time	tf2B[1]	V_{OH} = 2.0 V, V_{OL} = 0.4 V		1.2	1.6	ns
Duty Cycle	dt2B[1]	V_T = 1.25 V	45	50	55	%
Jitter, One Sigma[1]	t_{j1s1}	V_T = 1.5 V		2	3	%
Jitter, Absolute1	t_{jabs1b}	V_T = 1.5 V	-6	4.5	6	%

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 48M

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 20 pF

| PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -11 mA	2.4	3		V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA		0.2	0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V		-22	-18	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	12	20		mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V		2.2	2.5	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.9	2.5	ns
Duty Cycle[1]	D_{t1}	V_T = 1.5 V	45	50	55	%
Jitter, One Sigma[1]	T_{j1s1}	V_T = 1.5 V		2	3	%
Jitter, Absolute[1]	T_{jabs1}	V_T = 1.5 V	-6	4.5	6	%

[1]Guaranteed by design, not 100% tested in production.

General Layout Precautions:
1) Use a ground plane on the top layer of the PCB in all areas not used by traces.
2) Make all power traces and vias as wide as possible to lower inductance.

Notes:
1 All clock outputs should have series terminating resistor. Not shown in all places to improve readibility of diagram
2 Optional EMI capacitor should be used on all CPU, SDRAM, and PCI outputs.
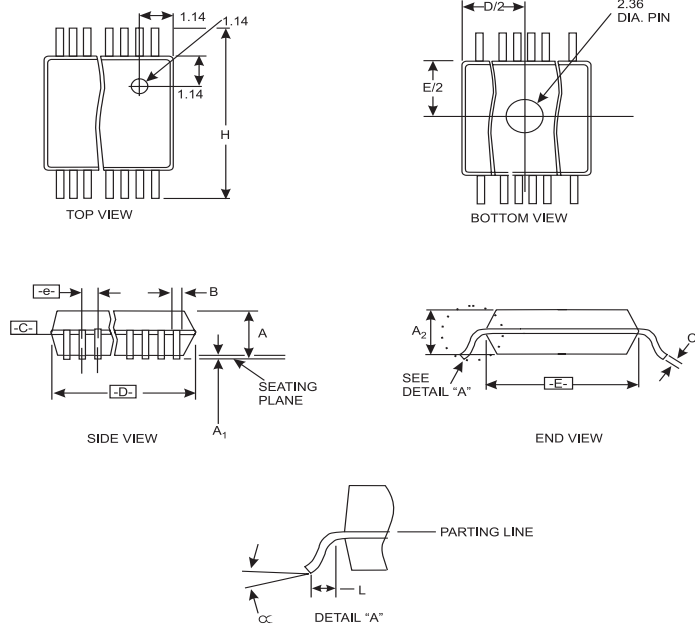3 Optional crystal load capacitors are recommended.
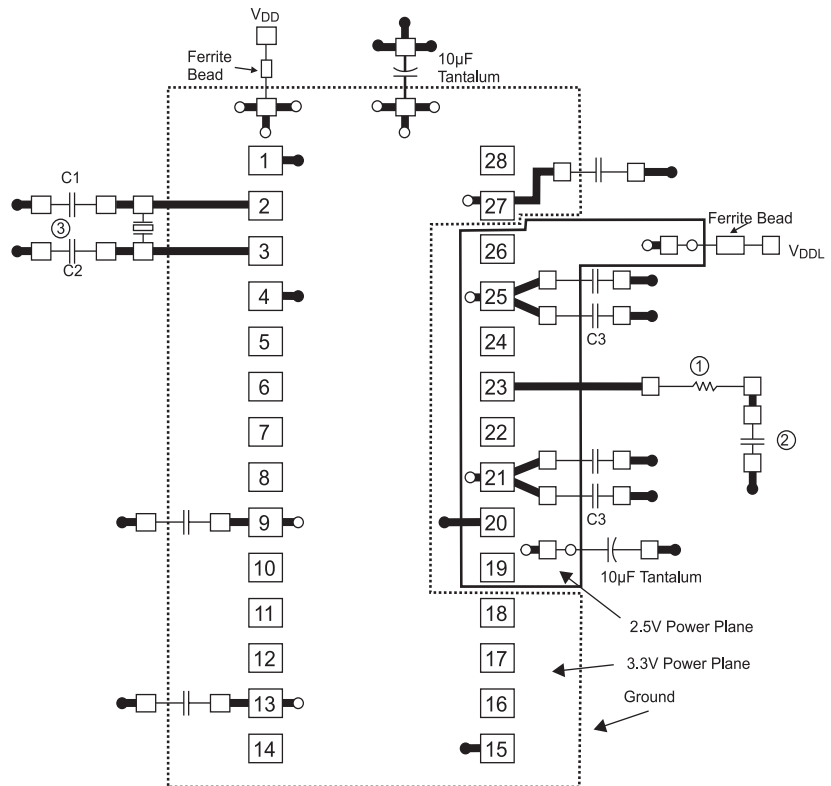
● = Ground Plane Connection

○ = Power Plane Conncetion

□ = Solder Pads

Capacitor Values:

C1, C2 : Crystal load values determined by user

C3 : 100pF ceramic

All unmarked capacitors are 0.01 μF ceramic

TOP VIEW

BOTTOM VIEW

SIDE VIEW

END VIEW

DETAIL "A"

SYMBOL	COMMON DIMENSIONS			VARIATIONS	D		
	MIN.	NOM.	MAX.	N	MIN.	NOM.	MAX.
A	0.068	0.073	0.078	14	0.239	0.244	0.249
A1	0.002	0.005	0.008	16	0.239	0.244	0.249
A2	0.066	0.068	0.070	20	0.278	0.284	0.289
b	0.010	0.012	0.015	24	0.318	0.323	0.328
c	0.004	0.006	0.008	28	0.397	0.402	0.407
D		See Variations		30	0.397	0.402	0.407
E	0.205	0.209	0.212				
e		0.0256 BSC					
H	0.301	0.307	0.311		Dimensions in inches		
L	0.025	0.030	0.037				
N		See Variations					
∝	0°	4°	8°				

Ordering Information

28 Pin SSOP Package

ICS9148F-49

Example:

ICS XXXX F - PPP

- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  F=SSOP
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device