HN62W4018M Series

1048576-word × 16-bit CMOS MASK Programmable ROM

HITACHI

ADE-203-447(Z)
Preliminary
Rev. 0.0
Nov. 1, 1995

Description

The HN62W4018M is a 16-Mbit CMOS mask-programmable ROM organized as 1,048,576-word by 16-bit. Realizing low power consumption, this memory is allowed for battery operation. And a high speed access of 120/150 ns (max) is the most suitable to the system using a high speed micro-computer by 16-bit.

Features

- Low voltage operation: 3.3 V ± 0.3 V
- High speed
  Normal access time: 120 ns/150 ns (max)
  Page access time: 40 ns/50 ns (max)
- Low power consumption
  Active : 360 mW (max)
  Standby : 0.72 mW (max)
  Power down mode : 36 µW (max)
- 8-word page access mode
- Three-state data output for or-tying
- LVTTL compatible

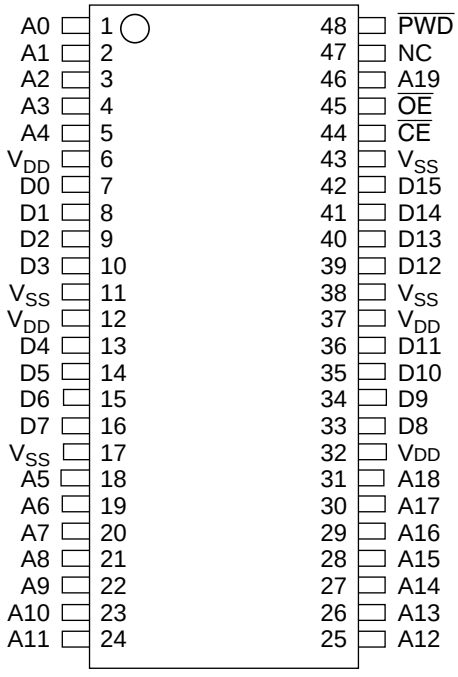
Ordering Information

Type No.	Access time	Package
HN62W4018MTA-12	120 ns	48-pin plastic TSOP - II (TTP-48D)
HN62W4018MTA-15	150 ns	

Note: The specifications of device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

Pin Arrangement

HN62W4018MTA

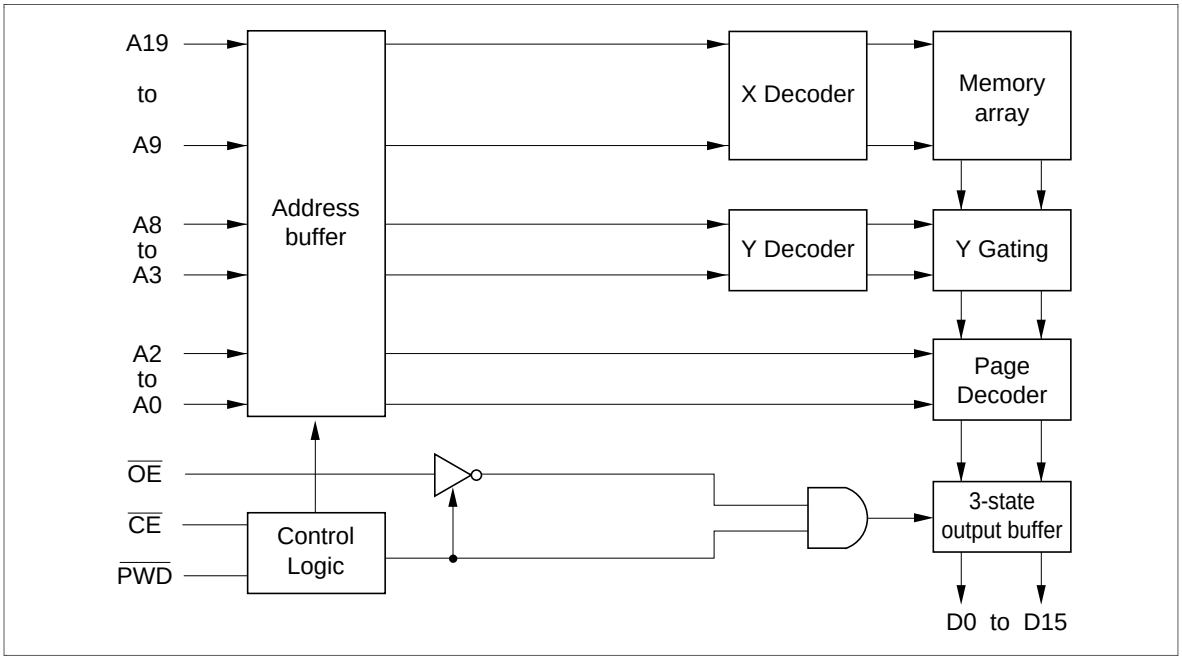


(Top view)

Pin Description

Pin name	Function
A3 to A19	Address inputs
A0 to A2	Page address inputs
D0 to D15	Data output
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{PWD}$	Power down input
NC	No connection
V_{DD}	Power supply
V_{SS}	Ground

Block Diagram



Mode Selection

	Pin					
				Data output	Address input	
Mode	**$\overline{PWD}$**	**$\overline{CE}$**	**$\overline{OE}$**	**D0-D15**	**LSB**	**MSB**
Power down	L	×[*1]	×	High-Z[*2]	—	—
Standby	H	H	×	High-Z	—	—
Output disable	H	L	H	High-Z	—	—
Read (16-bit)	H	L	L	D0 to D15	A0	A19

Notes: 1. ×: Don't care.
2. High-Z: High impedance.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Supply voltage	V_{DD}	–0.3 to +5.5	V	1
All input and output voltage	Vin, Vout	–0.3 to V_{DD} + 0.3	V	1
Operating temperatue range	Topr	0 to +70	°C	
Storage temperature range	Tstg	–55 to +125	°C	
Temperature under bias	Tbias	–20 to +85	°C	

Note: 1. With respect to V_{SS}

Recommended DC Operating Conditions (V_{SS} = 0 V, Ta = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V
Input voltage	V_{IH}	2.2	—	V_{DD} + 0.3	V
	V_{IL}	–0.3	—	0.8	V

DC Characteristics (V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V, Ta = 0 to 70°C)

Parameter	Symbol	Min	Max	Unit	Test conditions
Active supply current	I_{DD}	—	100	mA	V_{DD} = 3.6 V, I_{DOUT} = 0 mA, t_{RC} = min
Standby power supply current	I_{SB1}	—	200	µA	V_{DD} = 3.6 V, $\overline{CE} \geq V_{DD} - 0.2$ V
	I_{SB2}	—	3	mA	V_{DD} = 3.6 V, $\overline{CE} \geq 2.2$ V
Power down supply current	I_{PWD}	—	10	µA	V_{DD} = 3.6 V, $\overline{PWD} \leq 0.2$ V
Input leakage current	$\|I_{IL}\|$	—	10	µA	Vin = 0 V to V_{DD}
Output leakage current	$\|I_{OL}\|$	—	10	µA	$\overline{CE}$ = 2.2 V, Vout = 0 V to V_{DD}
Output voltage	V_{OH}	2.4	—	V	I_{OH} = –2 mA
	V_{OL}	—	0.4	V	I_{OL} = 2 mA

Capacitance (V_{DD} = 3.3 V ±0.3 V, V_{SS} = 0 V, Ta = 25°C, Vin = 0 V, f = 1 MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance*1	Cin	—	10	pF
Output capacitance*1	Cout	—	15	pF

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V, Ta = 0 to 70°C)

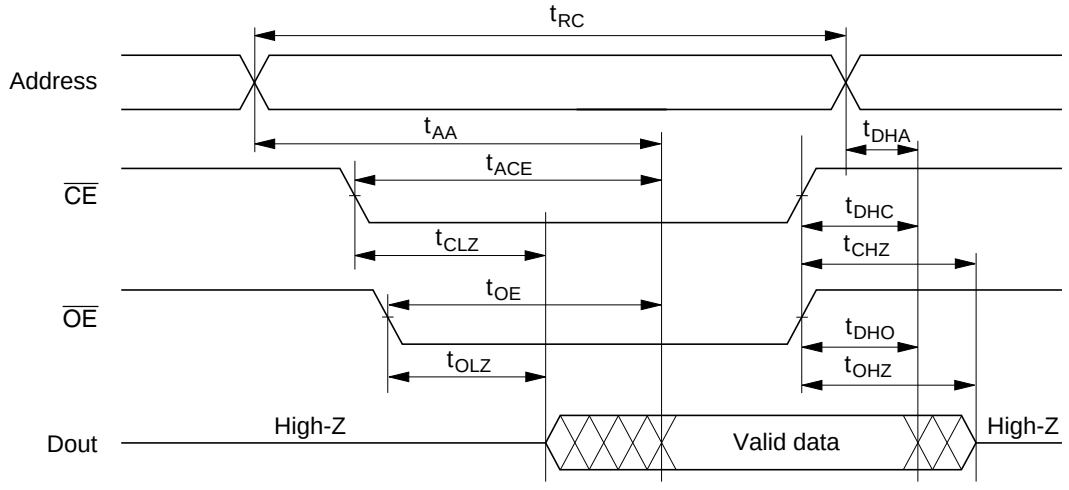
- Output load: 1TTL + C_L = 100 pF (including jig capacitance)
- Input pulse level: 0.4 V to 2.4 V
- Input and output timing reference levels: 1.4 V
- Input rise and fall time: 5 ns

		HN62W4018M-12		HN62W4018M-15			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Note**
Read cycle time	t_{RC}	120	—	150	—	ns	
Page read cycle time	t_{PC}	40	—	50	—	ns	
Address access time	t_{AA}	—	120	—	150	ns	
Page address access time	t_{PA}	—	40	—	50	ns	
$\overline{CE}$ access time	t_{ACE}	—	120	—	150	ns	
$\overline{OE}$ access time	t_{OE}	—	40	—	50	ns	
Output hold time from address change	t_{DHA}	0	—	0	—	ns	
Output hold time from $\overline{CE}$	t_{DHC}	0	—	0	—	ns	
Output hold time from $\overline{OE}$	t_{DHO}	0	—	0	—	ns	
Output hold time from $\overline{PWD}$	t_{DHP}	0	—	0	—	ns	
$\overline{CE}$ to output in high-Z	t_{CHZ}	—	40	—	50	ns	1
$\overline{OE}$ to output in high-Z	t_{OHZ}	—	40	—	50	ns	1
$\overline{CE}$ to output in low-Z	t_{CLZ}	5	—	5	—	ns	
$\overline{OE}$ to output in low-Z	t_{OLZ}	5	—	5	—	ns	
Recovery time from $\overline{PWD}$	t_R	10	—	10	—	µs	

Note: 1. t_{CHZ} and t_{OHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

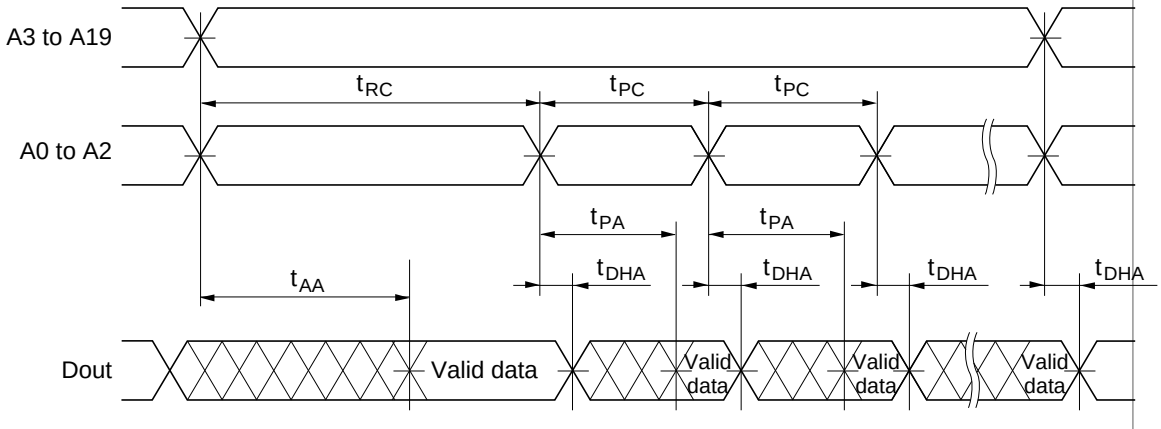
Timing Waveforms

Normal Mode



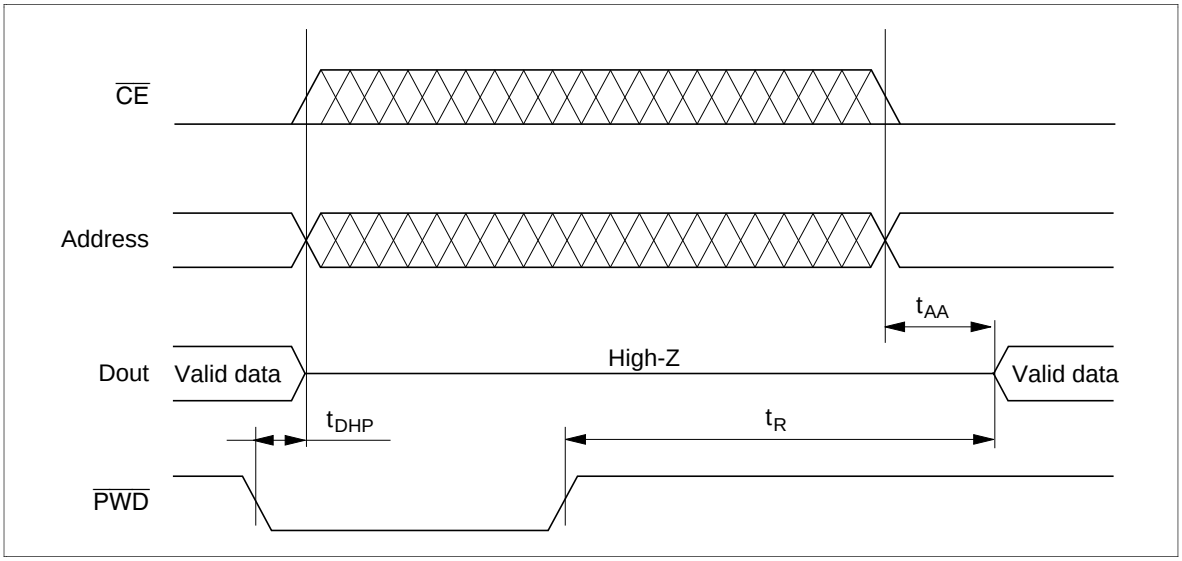
Notes: 1. t_{DHA}, t_{DHC}, t_{DHO}: Determined by faster.
2. t_{AA}, t_{ACE}, t_{OE}: Determined by slower.
3. t_{CLZ}, t_{OLZ}: Determined by slower.

Page Mode

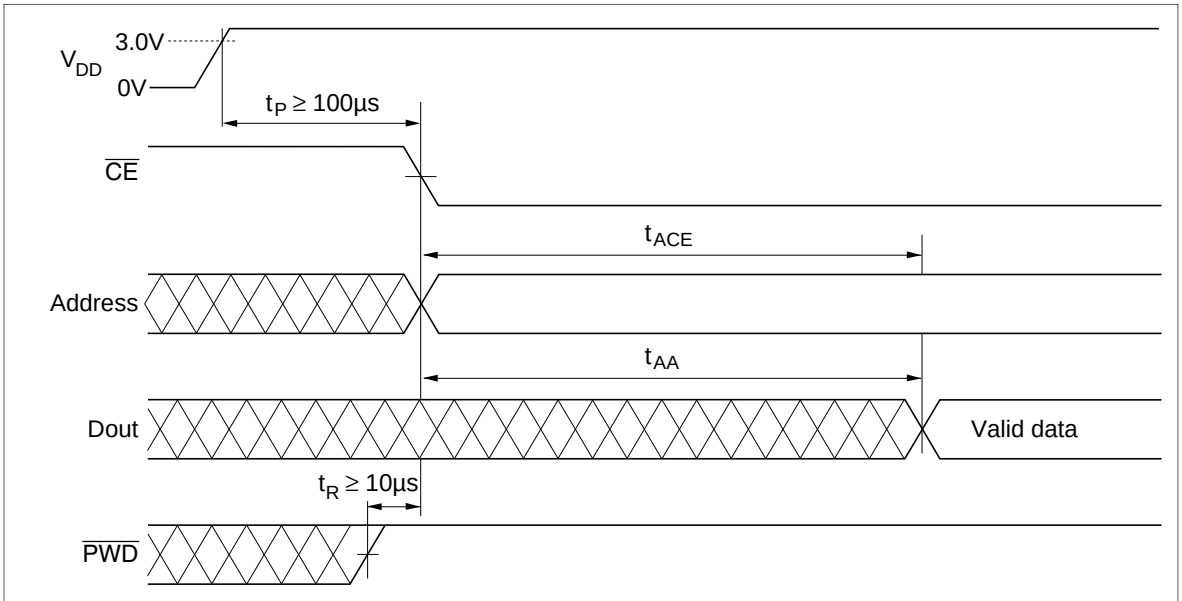


Notes: 1. $\overline{CE}$ and $\overline{OE}$ are enable.

Power Down Mode



Power Up Sequence



Notes: 1. This device is used ATD(Address Transition Detector). Therefore, transfer either $\overline{CE}$ or address(A19 to A3) after power up to 3.0 V.
2. t_P, t_R: Determined by slower.

Package Dimensions

HN62W4018MTA Series (TTP-48D) Unit: mm