



# Very Low Power/Voltage CMOS SRAM

## 256K X 16 bit

# BS616LV4018

### ■ FEATURES

- Vcc operation voltage : 4.5V ~ 5.5V
- Very low power consumption :
  - Vcc = 5.0V C-grade: 63mA (@55ns) operating current
  - I-grade: 65mA (@55ns) operating current
  - C-grade: 53mA (@70ns) operating current
  - I-grade: 55mA (@70ns) operating current
  - 2.0uA (Typ.) CMOS standby current
- High speed access time :
  - 55 55ns
  - 70 70ns
- Automatic power down when chip is deselected
- Three state outputs and TTL compatible
- Fully static operation
- Data retention supply voltage as low as 1.5V

- Easy expansion with  $\overline{CE}$  and  $\overline{OE}$  options
- I/O Configuration x8/x16 selectable by LB and  $\overline{UB}$  pin

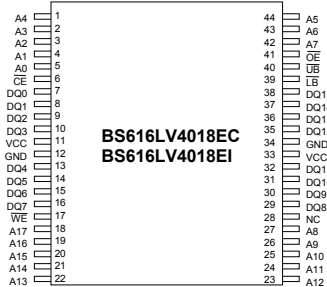
### ■ DESCRIPTION

The BS616LV4018 is a high performance, very low power CMOS Static Random Access Memory organized as 262,144 words by 16 bits and operates from a range of 4.5V to 5.5V supply voltage. Advanced CMOS technology and circuit techniques provide both high speed and low power features with a typical CMOS standby current of 2.0uA at 5.0V/25°C and maximum access time of 55ns at 5.0V/85°C. Easy memory expansion is provided by an active LOW chip enable ( $\overline{CE}$ ), active LOW output enable ( $\overline{OE}$ ) and three-state output drivers. The BS616LV4018 has an automatic power down feature, reducing the power consumption significantly when chip is deselected. The BS616LV4018 is available in DICE form, JEDEC standard 44-pin TSOP Type II package and 48-ball BGA package.

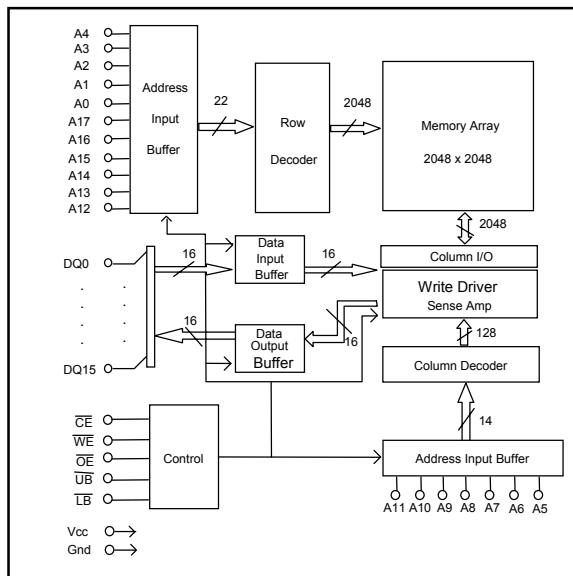
### ■ PRODUCT FAMILY

PRODUCT FAMILY	OPERATING TEMPERATURE	Vcc RANGE	SPEED (ns)	POWER DISSIPATION			PKG TYPE
				STANDBY (IccSBT, Max)	Operating (Icc, Max)		
				55ns:4.5~5.5V 70ns:4.5~5.5V	Vcc = 5.0V	Vcc = 5.0V 55ns	
BS616LV4018DC	+0°C to +70°C	4.5V ~ 5.5V	55 / 70	30uA	63mA	53mA	DICE
BS616LV4018EC							TSOP2-44
BS616LV4018AC							BGA-48-0608
BS616LV4018DI	-40°C to +85°C	4.5V ~ 5.5V	55 / 70	60uA	65mA	55mA	DICE
BS616LV4018EI							TSOP2-44
BS616LV4018AI							BGA-48-0608

### ■ PIN CONFIGURATIONS



### ■ BLOCK DIAGRAM



48-ball CSP - Top View

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**■ PIN DESCRIPTIONS**

Name	Function
<b>A0-A17 Address Input</b>	These 18 address inputs select one of the 262,144 x 16-bit words in the RAM.
<b><math>\overline{CE}</math> Chip Enable Input</b>	$\overline{CE}$ is active LOW. Chip enables must be active when data read from or write to the device. If chip enable is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high impedance state when the device is deselected.
<b><math>\overline{WE}</math> Write Enable Input</b>	The write enable input is active LOW and controls read and write operations. With the chip selected, when $\overline{WE}$ is HIGH and $\overline{OE}$ is LOW, output data will be present on the DQ pins; when $\overline{WE}$ is LOW, the data present on the DQ pins will be written into the selected memory location.
<b><math>\overline{OE}</math> Output Enable Input</b>	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{OE}$ is inactive.
<b><math>\overline{LB}</math> and <math>\overline{UB}</math> Data Byte Control Input</b>	Lower byte and upper byte data input/output control pins.
<b>DQ0 - DQ15 Data Input/Output Ports</b>	These 16 bi-directional ports are used to read data from or write data into the RAM.
<b>Vcc</b>	Power Supply
<b>Gnd</b>	Ground

**■ TRUTH TABLE**

MODE	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	D0~D7	D8~D15	Vcc CURRENT
Not selected (Power Down)	H	X	X	X	X	High Z	High Z	$I_{CCSB}$ , $I_{CCSB1}$
	X	X	X	H	H	High Z	High Z	$I_{CCSB}$ , $I_{CCSB1}$
Output Disabled	L	X	X	H	H	High Z	High Z	$I_{CC}$
	L	H	H	X	X	High Z	High Z	$I_{CC}$
Read	L	H	L	L	L	Dout	Dout	$I_{CC}$
				H	L	High Z	Dout	$I_{CC}$
				L	H	Dout	High Z	$I_{CC}$
Write	L	L	X	L	L	Din	Din	$I_{CC}$
				H	L	X	Din	$I_{CC}$
				L	H	Din	X	$I_{CC}$

**■ ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

SYMBOL	PARAMETER	RATING	UNITS
VTERM	Terminal Voltage with Respect to GND	-0.5 to V <sub>CC</sub> +0.5	V
TBIAS	Temperature Under Bias	-40 to +85	°C
TSTG	Storage Temperature	-60 to +150	°C
PT	Power Dissipation	1.0	W
IOUT	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**■ DC ELECTRICAL CHARACTERISTICS (TA = -40 to +85°C)**

PARAMETER NAME	PARAMETER	TEST CONDITIONS		MIN. TYP. <sup>(1)</sup> MAX.			UNITS
V <sub>IL</sub>	Guaranteed Input Low Voltage <sup>(2)</sup>		V <sub>CC</sub> =5.0V	-0.5	--	0.8	V
V <sub>IH</sub>	Guaranteed Input High Voltage <sup>(2)</sup>		V <sub>CC</sub> =5.0V	2.2	--	V <sub>CC</sub> +0.3	V
I <sub>IL</sub>	Input Leakage Current	V <sub>CC</sub> = Max, V <sub>IN</sub> = 0V to V <sub>CC</sub>		--	--	1	µA
I <sub>LO</sub>	Output Leakage Current	V <sub>CC</sub> = Max, $\overline{CE} = V_{IH}$ , or $\overline{OE}_i = V_{IH}$ V <sub>IO</sub> = 0V to V <sub>CC</sub>		--	--	1	µA
V <sub>OL</sub>	Output Low Voltage	V <sub>CC</sub> = Max, I <sub>OL</sub> = 2.0mA	V <sub>CC</sub> =5.0V	--	--	0.4	V
V <sub>OH</sub>	Output High Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = -1.0mA	V <sub>CC</sub> =5.0V	2.4	--	--	V
I <sub>CC</sub> <sup>(5)</sup>	Operating Power Supply Current	$\overline{CE} = V_{IL}$ , I <sub>DD</sub> = 0mA, F = F <sub>max</sub> <sup>(3)</sup>	V <sub>CC</sub> =5.0V	70ns 55ns	--	55 65	mA
I <sub>CCSB</sub>	Standby Current-TTL	$\overline{CE} = V_{IH}$ , I <sub>DD</sub> = 0mA	V <sub>CC</sub> =5.0V	--	--	1.0	mA
I <sub>CCSB1</sub> <sup>(4)</sup>	Standby Current-CMOS	$\overline{CE} \geq V_{CC} - 0.2V$ , V <sub>IN</sub> $\geq V_{CC} - 0.2V$ or V <sub>IN</sub> $\leq 0.2V$	V <sub>CC</sub> =5.0V	--	2.0	60	µA

1. Typical characteristics are at TA = 25°C.

2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.

3. F<sub>max</sub> = 1/t<sub>RC</sub>.

4. I<sub>CCSB1\_max</sub> is 30µA at V<sub>CC</sub>=5.0V and TA=70°C.

5. I<sub>CC\_max</sub> is 63mA(@55ns) / 53mA(@70ns) at V<sub>CC</sub>=5.0V/TA=0~70°C.

**■ OPERATING RANGE**

RANGE	AMBIENT TEMPERATURE	V <sub>CC</sub>
Commercial	0 °C to +70 °C	4.5V ~ 5.5V
Industrial	-40 °C to +85 °C	4.5V ~ 5.5V

**■ CAPACITANCE<sup>(1)</sup> (TA = 25°C, f = 1.0 MHz)**

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> =0V	6	pF
CDQ	Input/Output Capacitance	V <sub>I/O</sub> =0V	8	pF

1. This parameter is guaranteed and not 100% tested.

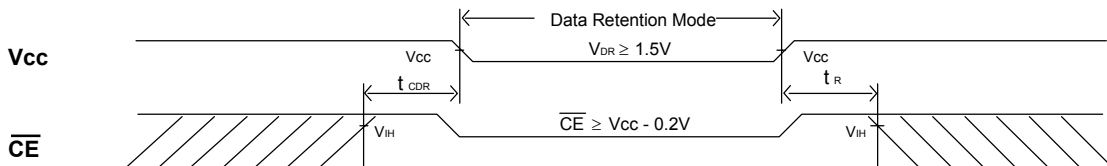
**■ DATA RETENTION CHARACTERISTICS (  $T_A = -40$  to  $+85^\circ\text{C}$  )**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN. TYP. <sup>(1)</sup> MAX.			UNITS
$V_{DR}$	Vcc for Data Retention	$\overline{CE} \cong V_{CC} - 0.2V$ $V_{IN} \cong V_{CC} - 0.2V$ or $V_{IN} \cong 0.2V$	1.5	--	--	V
$I_{CCDR}^{(3)}$	Data Retention Current	$\overline{CE} \cong V_{CC} - 0.2V$ $V_{IN} \cong V_{CC} - 0.2V$ or $V_{IN} \cong 0.2V$	--	0.3	1.3	$\mu\text{A}$
$t_{CDR}$	Chip Deselect to Data Retention Time	See Retention Waveform	0	--	--	ns
$t_R$	Operation Recovery Time		$T_{RC}^{(2)}$	--	--	ns

1.  $V_{CC} = 1.5V$ ,  $T_A = +25^\circ\text{C}$

2.  $t_{RC}$  = Read Cycle Time

3.  $I_{CCDR}(\text{Max.})$  is  $0.8\mu\text{A}$  at  $T_A=70^\circ\text{C}$ .






**■ LOW  $V_{CC}$  DATA RETENTION WAVEFORM (  $\overline{CE}$  Controlled )**


**■ AC TEST CONDITIONS**

(Test Load and Input/Output Reference)

Input Pulse Levels	V <sub>cc</sub> / 0V
Input Rise and Fall Times	1V/ns
Input and Output Timing Reference Level	0.5V <sub>cc</sub>
Output Load	C <sub>L</sub> = 30pF+1TTL C <sub>L</sub> = 100pF+1TTL

**■ KEY TO SWITCHING WAVEFORMS**

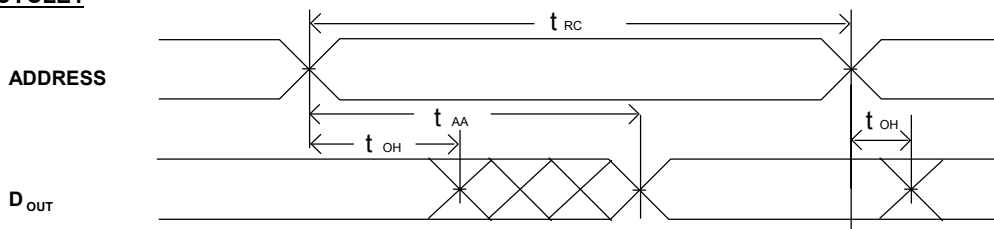
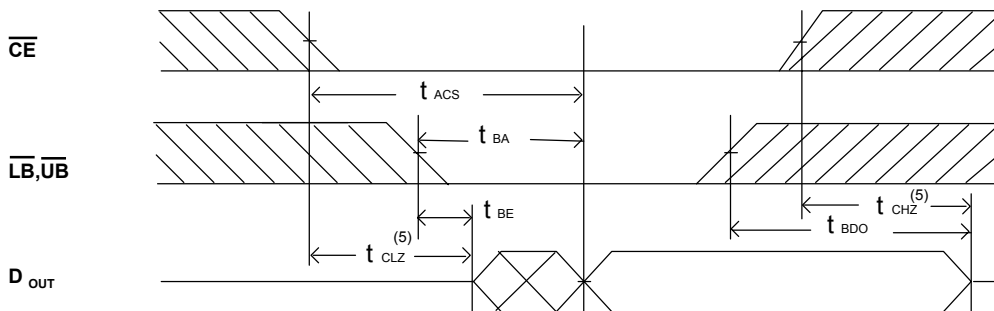
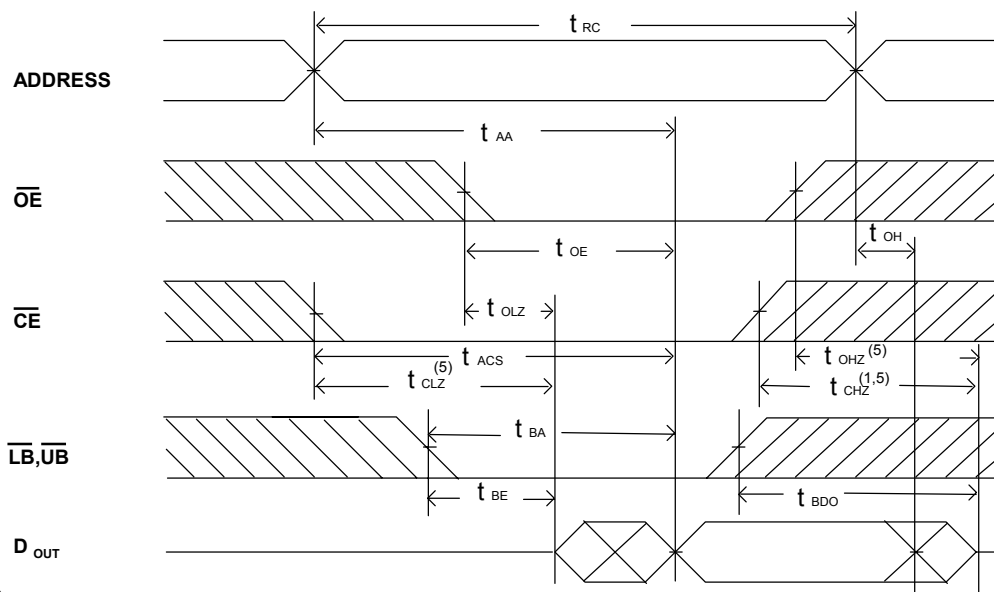
WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	MUST BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGE FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGE: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

**■ AC ELECTRICAL CHARACTERISTICS ( TA = -40 to + 85°C )**
**READ CYCLE**

JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	CYCLE TIME : 55ns (V <sub>cc</sub> = 4.5~5.5V)			CYCLE TIME : 70ns (V <sub>cc</sub> = 4.5~5.5V)			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
t <sub>AVAX</sub>	t <sub>RC</sub>	Read Cycle Time	55	--	--	70	--	--	ns
t <sub>AVQV</sub>	t <sub>AA</sub>	Address Access Time	--	--	55	--	--	70	ns
t <sub>ELQV</sub>	t <sub>ACS</sub>	Chip Select Access Time	--	--	55	--	--	70	ns
t <sub>BA</sub>	t <sub>BA</sub> <sup>(1)</sup>	Data Byte Control Access Time (LB,UB)	--	--	30	--	--	35	ns
t <sub>GLQV</sub>	t <sub>OE</sub>	Output Enable to Output Valid	--	--	30	--	--	35	ns
t <sub>E1LQX</sub>	t <sub>CLZ</sub>	Chip Select to Output Low Z	10	--	--	10	--	--	ns
t <sub>BE</sub>	t <sub>BE</sub>	Data Byte Control to Output Low Z (LB,UB)	5	--	--	5	--	--	ns
t <sub>GLQX</sub>	t <sub>OLZ</sub>	Output Enable to Output in Low Z	5	--	--	5	--	--	ns
t <sub>EHQZ</sub>	t <sub>CHZ</sub>	Chip Deselect to Output in High Z	--	--	30	--	--	35	ns
t <sub>BDO</sub>	t <sub>BDO</sub>	Data Byte Control to Output High Z (LB,UB)	--	--	30	--	--	35	ns
t <sub>GHQZ</sub>	t <sub>OHZ</sub>	Output Disable to Output in High Z	--	--	25	--	--	30	ns
t <sub>AXOX</sub>	t <sub>OH</sub>	Data Hold from Address Change	10	--	--	10	--	--	ns

NOTE :

 1. t<sub>BA</sub> is 30ns/35ns (@speed=55ns/70ns) with address toggle. ; t<sub>BA</sub> is 55ns/70ns (@speed=55ns/70ns) without address toggle.

**SWITCHING WAVEFORMS (READ CYCLE)**
**READ CYCLE1 (1,2,4)**

**READ CYCLE2 (1,3,4)**

**READ CYCLE3 (1,4)**

**NOTES:**

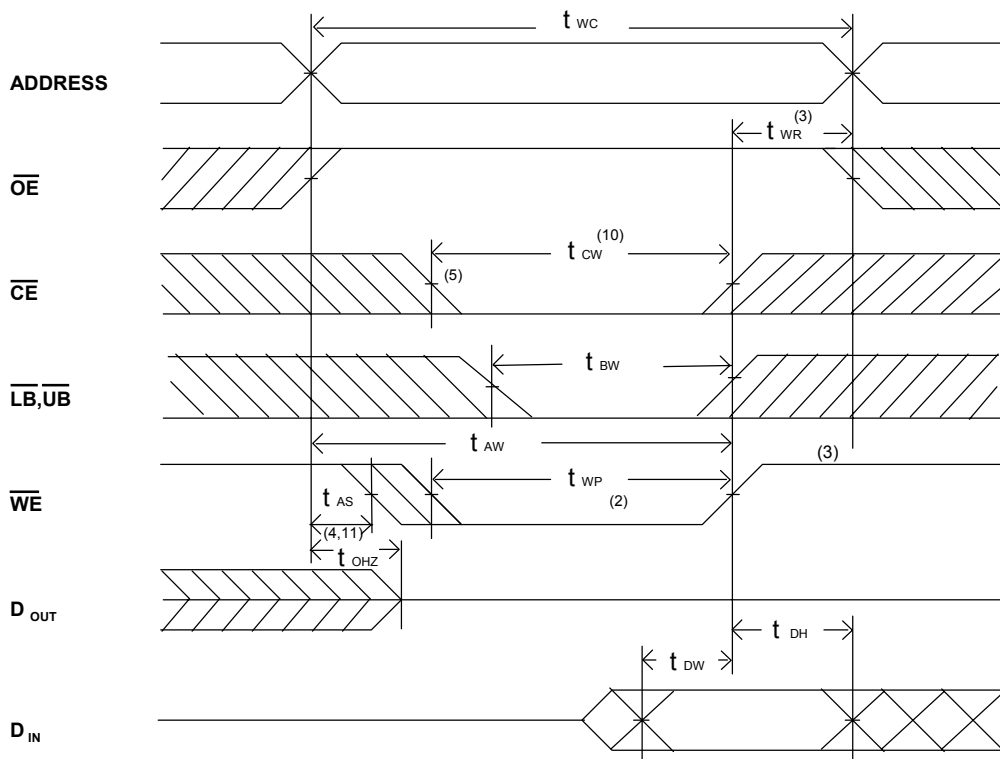
1.  $\overline{WE}$  is high in read Cycle.
2. Device is continuously selected when  $\overline{CE} = V_{IL}$ .
3. Address valid prior to or coincident with  $\overline{CE}$  transition low.
4.  $\overline{OE} = V_{IL}$ .
5. The parameter is guaranteed but not 100% tested.

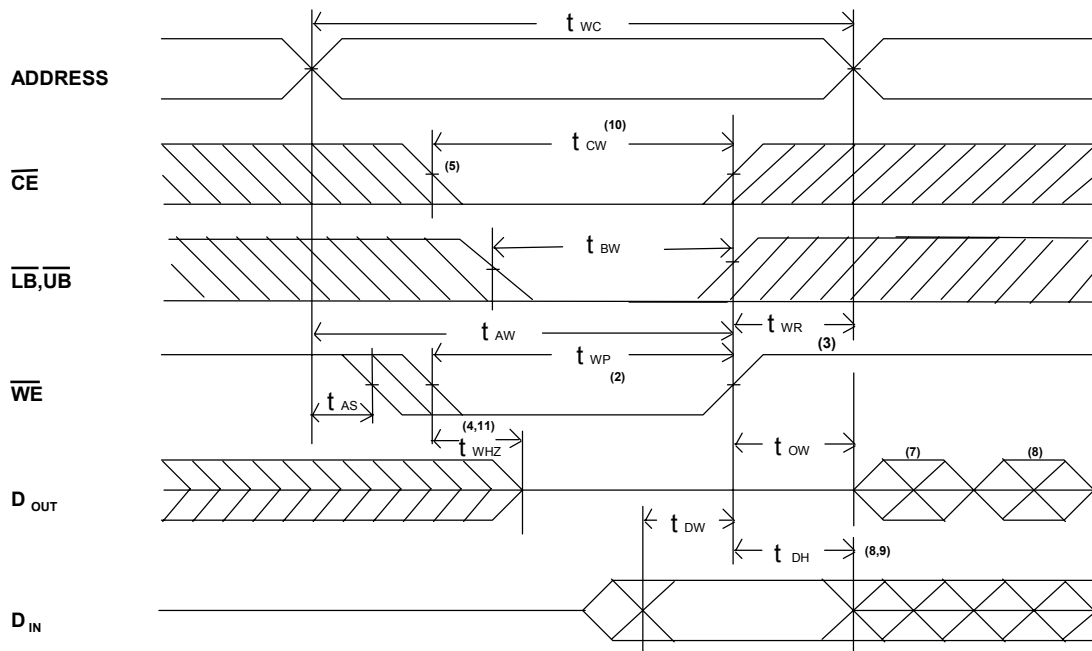
**■ AC ELECTRICAL CHARACTERISTICS ( TA = -40 to + 85°C )**  
**WRITE CYCLE**

JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	CYCLE TIME : 55ns (V <sub>CC</sub> = 4.5~5.5V)			CYCLE TIME : 70ns (V <sub>CC</sub> = 4.5~5.5V)			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
t <sub>AVAX</sub>	t <sub>WC</sub>	Write Cycle Time	55	--	--	70	--	--	ns
t <sub>E1LWH</sub>	t <sub>CW</sub>	Chip Select to End of Write	55	--	--	70	--	--	ns
t <sub>AVWL</sub>	t <sub>AS</sub>	Address Setup Time	0	--	--	0	--	--	ns
t <sub>AVWH</sub>	t <sub>AW</sub>	Address Valid to End of Write	55	--	--	70	--	--	ns
t <sub>WLWH</sub>	t <sub>WP</sub>	Write Pulse Width	30	--	--	35	--	--	ns
t <sub>WHAX</sub>	t <sub>WR</sub>	Write recovery Time (CE,WE)	0	--	--	0	--	--	ns
t <sub>BW</sub>	t <sub>BW</sub> <sup>(1)</sup>	Date Byte Control to End of Write (LB,UB)	25	--	--	30	--	--	ns
t <sub>WLQZ</sub>	t <sub>WHZ</sub>	Write to Output in High Z	--	--	25	--	--	30	ns
t <sub>DVWH</sub>	t <sub>DW</sub>	Data to Write Time Overlap	25	--	--	30	--	--	ns
t <sub>WHDX</sub>	t <sub>DH</sub>	Data Hold from Write Time	0	--	--	0	--	--	ns
t <sub>GHQZ</sub>	t <sub>OHZ</sub>	Output Disable to Output in High Z	--	--	25	--	--	30	ns
t <sub>WHOX</sub>	t <sub>OW</sub>	End of Write to Output Active	5	--	--	5	--	--	ns

NOTE :

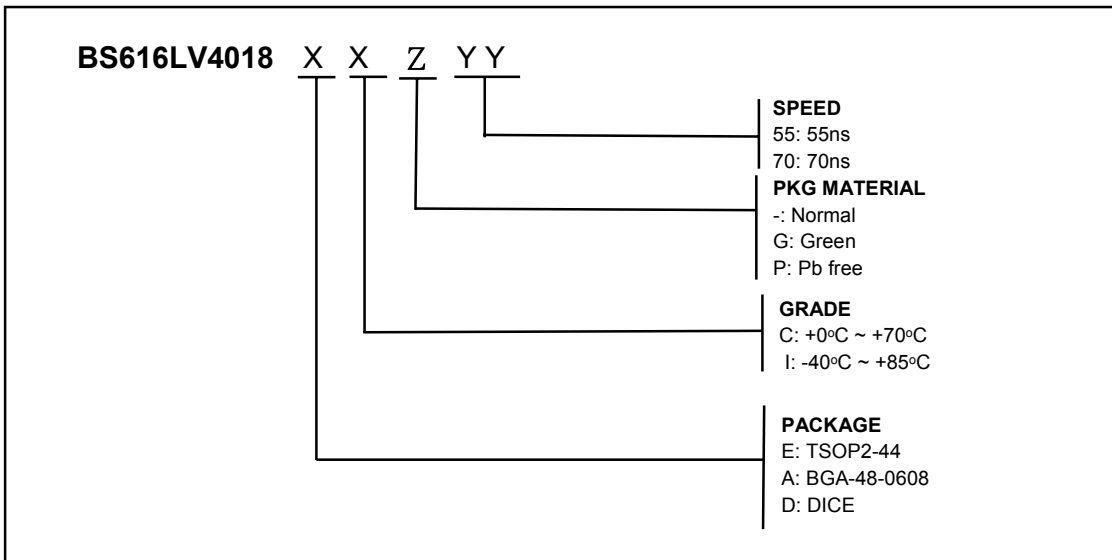
 1. t<sub>BW</sub> is 25ns/30ns (@speed=55ns/70ns) with address toggle. ; t<sub>BW</sub> is 55ns/70ns (@speed=55ns/70ns) without address toggle.

**■ SWITCHING WAVEFORMS (WRITE CYCLE)**
**WRITE CYCLE1<sup>(1)</sup>**


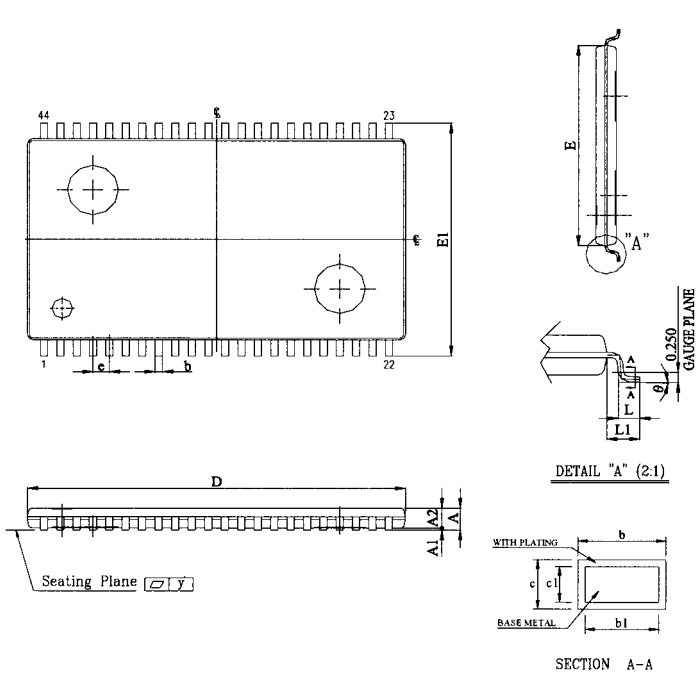
**WRITE CYCLE2 (1,6)**

**NOTES:**

1.  $\overline{WE}$  must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of  $\overline{CE}$  and  $\overline{WE}$  low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3.  $t_{WR}$  is measured from the earlier of  $\overline{CE}$  or  $\overline{WE}$  going high at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the  $\overline{CE}$  low transition occurs simultaneously with the  $\overline{WE}$  low transitions or after the  $\overline{WE}$  transition, output remain in a high impedance state.
6.  $\overline{OE}$  is continuously low ( $\overline{OE} = V_{IL}$ ).
7.  $D_{OUT}$  is the same phase of write data of this write cycle.
8.  $D_{OUT}$  is the read data of next address.
9. If  $\overline{CE}$  is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10.  $t_{CW}$  is measured from the later of  $\overline{CE}$  going low to the end of write.
11. The parameter is guaranteed but not 100% tested.



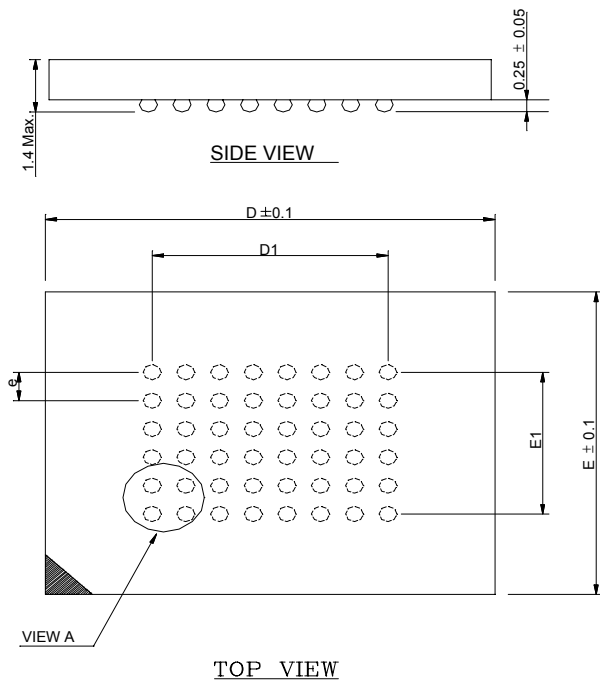
**ORDERING INFORMATION**


Note:  
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**PACKAGE DIMENSIONS**


SYMBOL	UNIT	INCH	MM
A		0.0433± 0.004	1.10± 0.10
A1		0.004± 0.002	0.10± 0.05
A2		0.039± 0.002	1.00± 0.05
b		0.012 ~ 0.018	0.30 ~ 0.45
b1		0.012 ~ 0.016	0.30 ~ 0.40
c		0.005 ~ 0.008	0.12 ~ 0.21
c1		0.005 ~ 0.006	0.12 ~ 0.16
D		0.725± 0.004	18.41± 0.10
E		0.400± 0.004	10.16± 0.10
E1		0.463± 0.008	11.76± 0.20
e		0.0315± 0.004	0.80± 0.10
L		0.0197± 0.004	0.50± 0.10
L1		0.0315± 0.004	0.80± 0.10
y		0.004 Max.	0.1 Max.
θ		0° ~ 8°	0° ~ 8°

**TSOP2-44**

**■ PACKAGE DIMENSIONS (continued)**


**48 mini-BGA (6 x 8mm)**

**NOTES:**

- 1: CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
- 2: PIN#1 DOT MARKING BY LASER OR PAD PRINT.
- 3: SYMBOL "N" IS THE NUMBER OF SOLDER BALLS.

N	D	E	D1	E1
48	8.0	6.0	5.25	3.75

