AN2125FHS

Analog signal processing super single-chip IC for CCD camera

■ Overview

The AN2125FHS is a super single-chip IC, working as an image signal processing circuit for CCD camera including Y/C mix, 75-Ω driver, and sub-carrier generation functions as well as luminance signal processing, color difference signal processing functions and an encoder.

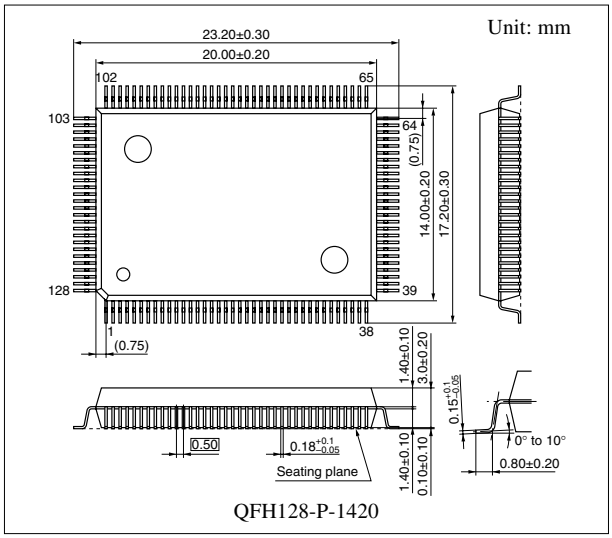
Moreover, the AN2125FHS includes auto-white-balance control circuits, operational amplifiers for AGC, and automatic read-out function from EEPROM at power-on sequence, and DACs for adjustment, therefore a CCD camera system without a microcomputer can be constructed by only additional EEPROM.

■ Features

- For 510H (250000 pixels) CCD
- NTSC/PAL compatible
- On-chip FH lock system (sub-carrier generation)
- On-chip automatic read-out function from EEPROM data at power-on
- On-chip DAC for adjustment (8 bits, 32 channels)
- On-chip circuit for external synchronization
- On-chip comparator for electronic iris

■ Applications

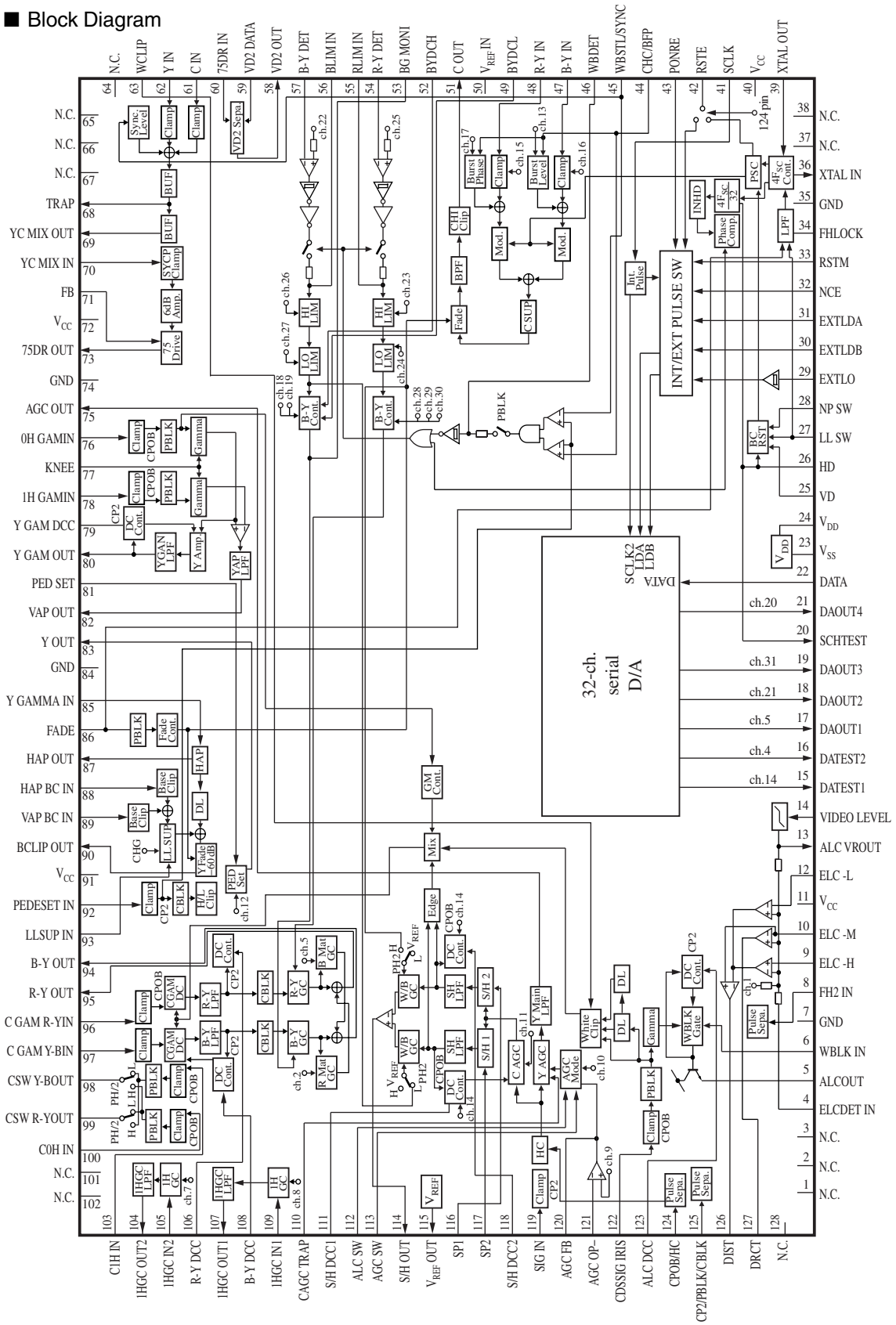
- General CCD cameras including monitor cameras, board cameras, video cameras, videophones, video conference systems, and PC input camera



QFH128-P-1420

Note) The package of this product will be changed to lead-free type (QFH128-P-1420E). See the new package dimensions section later of this datasheet.

■ Block Diagram



■ Pin Descriptions

Pin No.	Description	Pin No.	Description
1	N.C.	38	N.C.
2	N.C.	39	XTAL OUT
3	N.C.	40	V_{CC}
4	ELCDET IN	41	SCLK
5	ALCOUT	42	RSTE
6	WBLK IN	43	PONRE
7	GND	44	CHC / BFP
8	FH2 IN	45	WBSTL / SYNC
9	ELC –H	46	WBDET
10	ELC –M	47	B-Y IN
11	V_{CC}	48	R-Y IN
12	ELC –L	49	BYDCL
13	ALC VROUT	50	V_{REF} IN
14	VIDEO LEVEL	51	C OUT
15	DATEST 1	52	BYDCH
16	DATEST 2	53	BG MONI
17	DAOUT 1	54	R-Y DET
18	DAOUT 2	55	RLIM IN
19	DAOUT 3	56	BLIM IN
20	SCHTEST	57	B-Y DET
21	DAOUT 4	58	VD2 OUT
22	DATA	59	VD2 DATA
23	V_{SS}	60	75DR IN
24	V_{DD}	61	C IN
25	VD	62	Y IN
26	HD	63	WCLIP
27	LL SW	64	N.C.
28	NP SW	65	N.C.
29	EXTLO	66	N.C.
30	EXTLDB	67	N.C.
31	EXTLDA	68	TRAP
32	NCE	69	YC MIX OUT
33	RSTM	70	YC MIX IN
34	FHLOCK	71	FB
35	GND	72	V_{CC}
36	XTAL IN	73	75DR OUT
37	N.C.	74	GND

■ Pin Descriptions (continued)

Pin No.	Description	Pin No.	Description
75	AGC OUT	102	N.C.
76	0H GAMIN	103	C1H IN
77	KNEE	104	1HGC OUT2
78	IH GAMIN	105	1HGC IN2
79	Y GAM DCC	106	R-Y DCC
80	Y GAM OUT	107	1HGC OUT1
81	PED SET	108	B-Y DCC
82	VAP OUT	109	1HGC IN1
83	Y OUT	110	CAGC TRAP
84	GND	111	S/H DCC1
85	Y GAMMA IN	112	ALC SW
86	FADE	113	AGC SW
87	HAP OUT	114	S/H OUT
88	HAP BC IN	115	V_{REF} OUT
89	VAP BC IN	116	SP1
90	BCLIP OUT	117	SP2
91	V_{CC}	118	S/H DCC 2
92	PEDESET IN	119	SIG IN
93	LLSUP IN	120	AGC FB
94	B-Y OUT	121	AGC OP–
95	R-Y OUT	122	CDSSIG IRIS
96	C GAM R-YIN	123	ALC DCC
97	C GAM Y-BIN	124	CPOB / HC
98	CSW Y-BOUT	125	CP2 / PBLK / CBLK
99	CSW R-YOUT	126	DIST
100	C0H IN	127	DRCT
101	N.C.	128	N.C.

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	5.5	V
Supply current	I_{CC}	170	mA
Power dissipation *2	P_D	876	mW
Operating ambient temperature *1	T_{opr}	–20 to +75	°C
Storage temperature *1	T_{stg}	–55 to +150	°C

Note) ∗1: Except for the operating ambient temperature and storage temperature, all ratings are for T_a = 25°C.

∗2: The above power dissipation shows the package power dissipation at T_a = 75°C in free air.

■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Supply voltage	V_{CC}	4.5 to 5.1	V

■ Electrical Characteristics at T_a = 25°C ± 2°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Circuit current	I_{TOT}	V_{CC} = 4.8 V	90	120	150	mA
Reference voltage 1	V_{REF}	V_{CC} = 4.8 V Output voltage of pin 115	1.66	1.76	1.86	V
Reference voltage 2	V_{DD}	V_{CC} = 4.8 V	3.21	3.38	3.55	V
Pulse separation CPOB	V_{CPOB}	V_{CC} = 4.8 V Voltage of pin 124 is increased from 0 V. Voltage of pin 124 when the voltage of pin 100 changes from the low-level to V_{REF} .	3.3	3.6	3.9	V
Pulse separation PBLK	V_{PBLK}	V_{CC} = 4.8 V Voltage of pin 100 and voltage of pin 125 are increased from V_{REF} + 1 V and from 0 V, respectively. Voltage of pin 125 when the voltage of pin 99 is reduced by 1 V from the high-level.	1.55	1.8	2.05	V
Pulse separation CP2	V_{CP2}	V_{CC} = 4.8 V Voltage of pin 125 is increased from 0 V. Voltage of pin 125 when the voltage of pin 92 changes from the low-level to V_{REF} .	3.6	3.9	4.2	V
Pulse separation CBLK	V_{CBLK}	V_{CC} = 4.8 V Voltage of pin 92 and voltage of pin 125 are increased from V_{REF} + 1 V and from 0 V, respectively. Voltage of pin 125 when the voltage of pin 83 is reduced by 0.5 V or more from the high-level. (V_{REF} + 1 V)	0.6	0.8	1.0	V
Pulse separation FH/2	V_{FH2}	V_{CC} = 4.8 V Voltage of pin 103, voltage of pin 100 and voltage of pin 8 are increased from V_{REF} , V_{REF} + 1 V, and 0 V, respectively. Voltage of pin 8 when the voltage of pin 99 is reduced by 1 V from the high-level.	1.15	1.4	1.65	V

■ Electrical Characteristics at T_a = 25°C ± 2°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Pulse separation SYNC	V_{SYNC}	V_{CC} = 4.8 V Voltage of pin 62 and voltage of pin 45 are reduced from V_{REF} and V_{CC}, respectively. Voltage of pin 45 when the voltage of pin 68 is reduced by 0.3 V or more.	0.8	1.0	1.2	V
Pulse separation BFP	V_{BFP}	V_{CC} = 4.8 V Inputs sine wave of 14 MHz at 1 V[p-p] to pin 36. Voltage of pin 44 is increased from 0 V. Voltage of pin 44 when chroma output of 200 V[p-p] or more at pin 51 is generated.	3.35	3.65	3.95	V
Pulse separation SP 1	V_{SP1}	V_{CC} = 4.8 V Pulse level of SP1 is 1.1 V.	0.8	1.0	1.2	V
Pulse separation SP 2	V_{SP2}	V_{CC} = 4.8 V Pulse level of SP2 is 1.1 V.	0.8	1.0	1.2	V
Pulse separation VD2	V_{VD2}	V_{CC} = 4.8 V Open pin 60. Voltage of pin 59 is increased from 0 V. Voltage difference between pin 59 and V_{REF} when the voltage of pin 58 changes from the high-level to the low-level.	0.8	1.0	1.2	V
Comparator threshold 1	V_{CP1}	V_{CC} = 4.8 V, Pin 9 = 2.8 V, Pin 10 = 2.3 V, Pin 12 = 1.8 V, Pin 14 = V_{REF}, CH1 = 80 V Voltage of pin 4 is increased from 0 V. Voltage of pin 4 when the output voltage of pin 126 changes from the high-level to the low-level. Voltage of pin 4 is increased from 0 V.	1.55	1.8	2.05	V
Comparator threshold 2	V_{CP2}	V_{CC} = 4.8 V, Pin 9 = 2.8 V, Pin 10 = 2.3 V, Pin 12 = 1.8 V, Pin 14 = V_{REF}, CH1 = 80 V Voltage of pin 4 is increased from 0 V. Voltage of pin 4 when the output voltage of pin 127 changes from the low-level to the high-level.	2.05	2.3	2.65	V
FH lock detection DC	V_{FHDC}	V_{CC} = 4.8 V Output voltage of pin 34 at Pin 27 = V_{CC}	1.9	2.0	2.1	V
YAGC maximum gain	G_{YAX}	V_{119} = 10 steps, 20 mV[p-p]	20	24	28	dB
CAGC maximum gain	G_{CAX}	V_{119} = 10 steps, 20 mV[p-p]	20	24	28	dB

■ Electrical Characteristics at T_a = 25°C ± 2°C (continued)

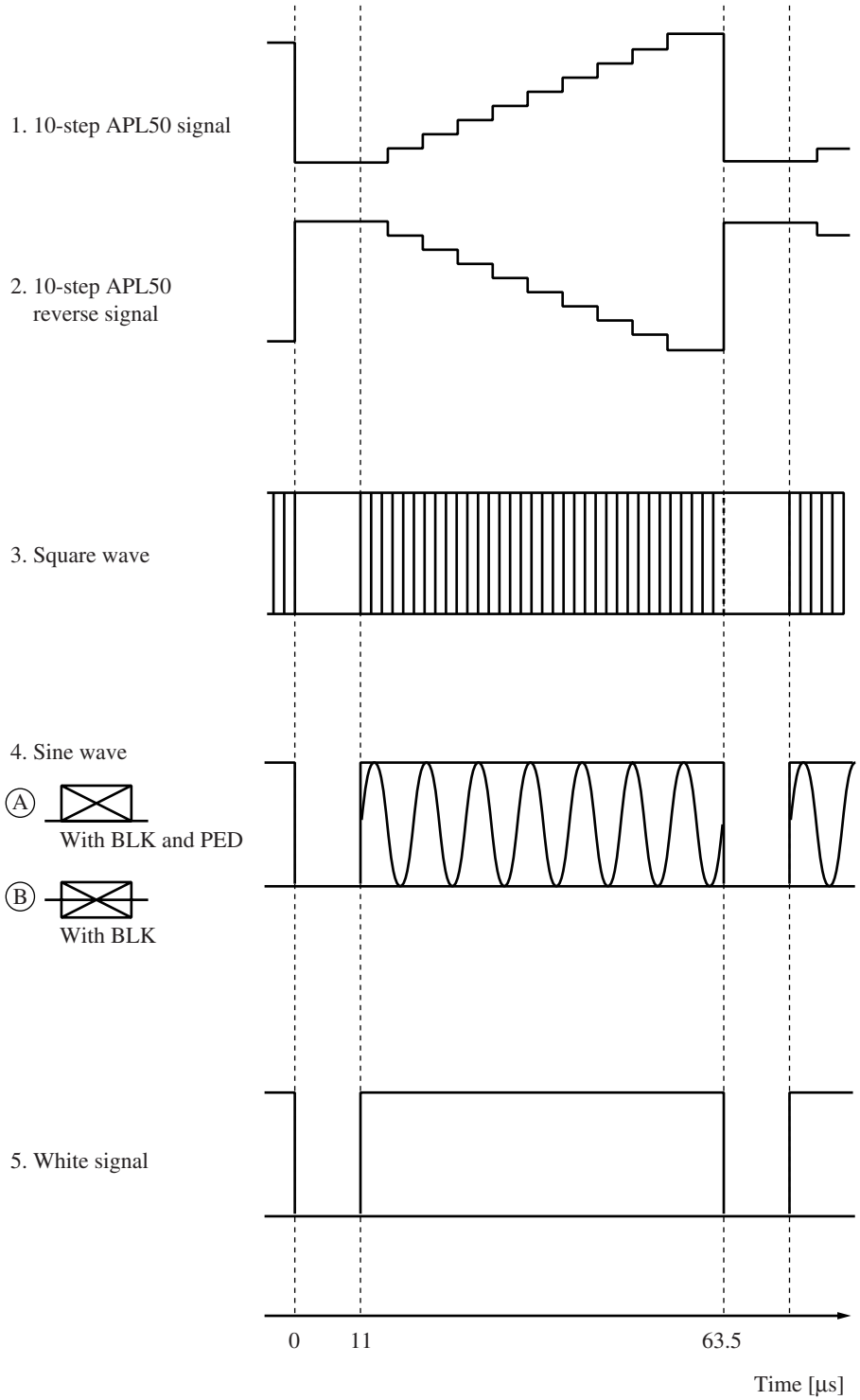
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
AGC minimum gain 1	G_{YAN1}	V_{119} = 10 steps, 1 200 mV[p-p]	−8.5	−6.5	−4.5	dB
AGC minimum gain 2	G_{YAN2}	V_{119} = 10 steps, 1 200 mV[p-p]	−4.5	−2.5	− 0.5	dB
WB characteristic 1	V_{SH2}	V_{119} = sin, 500 kHz, 500 mV[p-p]	−470	−400	−330	mV[p-p]
WB characteristic 2	G_{SH6}	V_{119} = sin, 500 kHz, 500 mV[p-p]	−2	0	2	dB
S/H characteristic	V_{SH9}	V_{119} = Square wave 500 kHz, 1 V[p-p]	700	800	900	mV[p-p]
Iris GC characteristic	V_{TR2}	V_{122} = 10 steps, 1 200 mV[p-p] V_6 = GND	1 100	1 300	1 500	mV[p-p]
Iris gate level difference	V_{WG}	V_{122} = C-GND	−20	0	20	mV[p-p]
Iris gamma 1	V_{IG1}	V_{122} = 10 steps, 1 500 mV[p-p]	800	900	1 000	mV[p-p]
Iris gamma 2	G_{IG2}	V_{122} = 10 steps, 1 500 mV[p-p]	0.5	1.7	2.9	dB
Iris gamma 3	G_{IG3}	V_{122} = 10 steps, 1 500 mV[p-p]	0.5	—	—	dB
Iris BLK level difference	V_{WB}	V_{122} = C-GND	−20	0	20	mV[p-p]
Delay signal amplifier gain 1	G_{IH2}	V_{105} = sin, 500 kHz, 500 mV[p-p]	6.5	8.0	—	dB
Delay signal amplifier gain 2	G_{IH5}	V_{109} = sin, 500 kHz, 500 mV[p-p]	6.5	8.0	—	dB
Luminance gamma characteristic 1	V_{YG1}	V_{76} = 10 steps, 700 mV[p-p]	450	550	650	mV[p-p]
Luminance gamma characteristic 2	G_{YG2}	V_{76} = 10 steps, 700 mV[p-p]	−13	−11	−9	dB
Luminance gamma characteristic 3	G_{YG3}	V_{76} = 10 steps, 1 500 mV[p-p]	1.5	3.5	5.5	dB
Luminance gamma BLK level difference	V_{YGB}	V_{76} = C-GND	−20	0	20	mV[p-p]
V aperture gain	V_{VA1}	V_{78} = sin, 500 kHz, 300 mV[p-p]	−1 250	−1 050	−850	mV[p-p]
V aperture BLK level difference	V_{VAB}	V_{76} = V_{78} = C-GND	−20	0	20	mV[p-p]
H aperture gain	V_{HA1}	V_{92} = sin, 4 MHz, 200 mV[p-p]	900	1 100	1 300	mV[p-p]
H aperture base clip	V_{HB1}	V_{88} = sin, 500 kHz, 100 mV[p-p]	90	130	160	mV[p-p]
V aperture base clip	V_{VB1}	V_{89} = sin, 500 kHz, 100 mV[p-p]	90	130	160	mV[p-p]
Luminance output amplifier gain	G_{Y1}	V_{92} = 10 steps, 600 mV[p-p]	− 0.5	1.0	2.5	dB
Luminance high clip level	V_{YH}	V_{92} = 10 steps, 1 V[p-p]	700	840	980	mV[p-p]
Luminance low clip level	V_{YL}	V_{92} = 10 steps, 200 mV[p-p]	−50	−30	−10	mV[p-p]
Synchronizing signal output level 2	V_{SYN2}	V_{62} = C-GND	260	300	340	mV[p-p]
Pedestal control characteristic 1	V_{YP1}	V_{92} = C-GND	60	90	120	mV[p-p]
Pedestal control characteristic 2	V_{TP2}	V_{92} = C-GND	−30	−15	0	mV[p-p]
Luminance fade characteristic	G_{YFB}	V_{85} = 10 steps, 600 mV[p-p]	—	−40	−26	dB
CSW (R-Y) gain	G_{CS1}	V_{100} = V_{103} = 10 steps, 600 mV[p-p]	−1.5	0	1.5	dB
CSW (B-Y) gain	G_{CS2}	V_{100} = V_{103} = 10 steps, 600 mV[p-p]	−1.5	0	1.5	dB
CSW (R-Y) BLK level difference	V_{CSB1}	V_{100} = V_{103} = C-GND	−20	0	20	mV[p-p]
CSW (B-Y) BLK level difference	V_{CSB2}	V_{100} = V_{103} = C-GND	−20	0	20	mV[p-p]
CSW (R-Y) FH2 level difference	V_{CSF1}	V_{100} = V_{103} = C-GND	−20	0	20	mV[p-p]
CSW (B-Y) FH2 level difference	V_{CSF2}	V_{100} = V_{103} = C-GND	−20	0	20	mV[p-p]

■ Electrical Characteristics at T_a = 25°C ± 2°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Color difference gamma characteristic 1	V_{CG1}	V_{76} = 10 steps, 700 mV[p-p] V_{96} = 10 steps, 350 mV[p-p]	10	80	F0	HEX
Color difference gamma characteristic 2	G_{CG2}	V_{76} = 10 steps, 700 mV[p-p] V_{96} = 10 steps, 350 mV[p-p]	−13	−10.5	−8	dB
Color difference gamma characteristic 3	G_{CG3}	V_{76} = 10 steps, 1 500 mV[p-p] V_{96} = 10 steps, 750 mV[p-p]	2.0	3.5	5.0	dB
Color difference gamma characteristic 4	V_{CG4}	V_{76} = 10 steps, 700 mV[p-p] V_{96} = 10 steps, 350 mV[p-p]	10	80	F0	HEX
Color difference gamma characteristic 5	G_{CG5}	V_{76} = 10 steps, 700 mV[p-p] V_{96} = 10 steps, 350 mV[p-p]	−13	−10.5	−8	dB
Color difference gamma characteristic 6	G_{CG6}	V_{76} = 10 steps, 1 500 mV[p-p] V_{96} = 10 steps, 750 mV[p-p]	2.0	3.5	5.0	dB
R-Y gain characteristic	G_{CL1}	V_{96} = sin, 500 kHz, 200 mV[p-p]	6.5	10.0	13.5	dB
B-Y gain characteristic	G_{CL3}	V_{97} = sin, 500 kHz, 200 mV[p-p]	6.5	10.0	13.5	dB
B-Y matrix characteristic	V_{CM1I}	V_{97} = 10 steps, 300 mV[p-p]	−160	−100	−40	mV[p-p]
R-Y matrix characteristic	V_{CM2I}	V_{96} = 10 steps, 300 mV[p-p]	40	100	160	mV[p-p]
R-Y BLK level difference	V_{CB1}	V_{100} = V_{103} = C-GND	−20	0	20	mV[p-p]
B-Y BLK level difference	V_{CB2}	V_{100} = V_{103} = C-GND	−20	0	20	mV[p-p]
Burst level	V_{BU1}	V_{48} = White, 200 mV[p-p], V_{47} = C-GND	253	300	347	mV[p-p]
Chroma output amplitude R	G_{CR1}	V_{48} = White, 200 mV[p-p], V_{47} = C-GND	6	8	10	dB
Chroma output amplitude B	G_{CR3}	V_{48} = C-GND, V_{47} = White, 200 mV[p-p]	1	3	5	dB
Chroma high cut characteristic	G_{CH}	V_{48} = White, 400 mV[p-p], V_{47} = C-GND	680	760	840	mV[p-p]
Chroma fade characteristic	G_{CF}	V_{48} =White, 200 mV[p-p], V_{47} = C-GND	—	−40	−20	dB
High-luminance chroma suppress	G_{CS}	V_{48} = V_{92} = White, 500 mV[p-p] V_{47} = C-GND	—	−40	−18	dB
FH lock range H	F_{FH3}	HD + 1 Hz	0.75	—	—	Hz
FH lock range L	F_{FH2}	HD − 1 Hz	—	—	− 0.75	Hz
VXO free-running frequency	F_{FR}	V_{27} = V_{CC} V_{124} = GND	3.57 9 465	3.57 9 545	3.57 9 625	MHz
75-Ω driver gain	G_{DR}	V_{62} = 10 steps, 700 mV[p-p]	−1.5	0	1.5	dB
Luminance main LPF characteristic	G_{YM}	V_{119} = V_{76} = sin, 4.77 MHz, 500 mV[p-p]	−30	−20	−10.5	dB

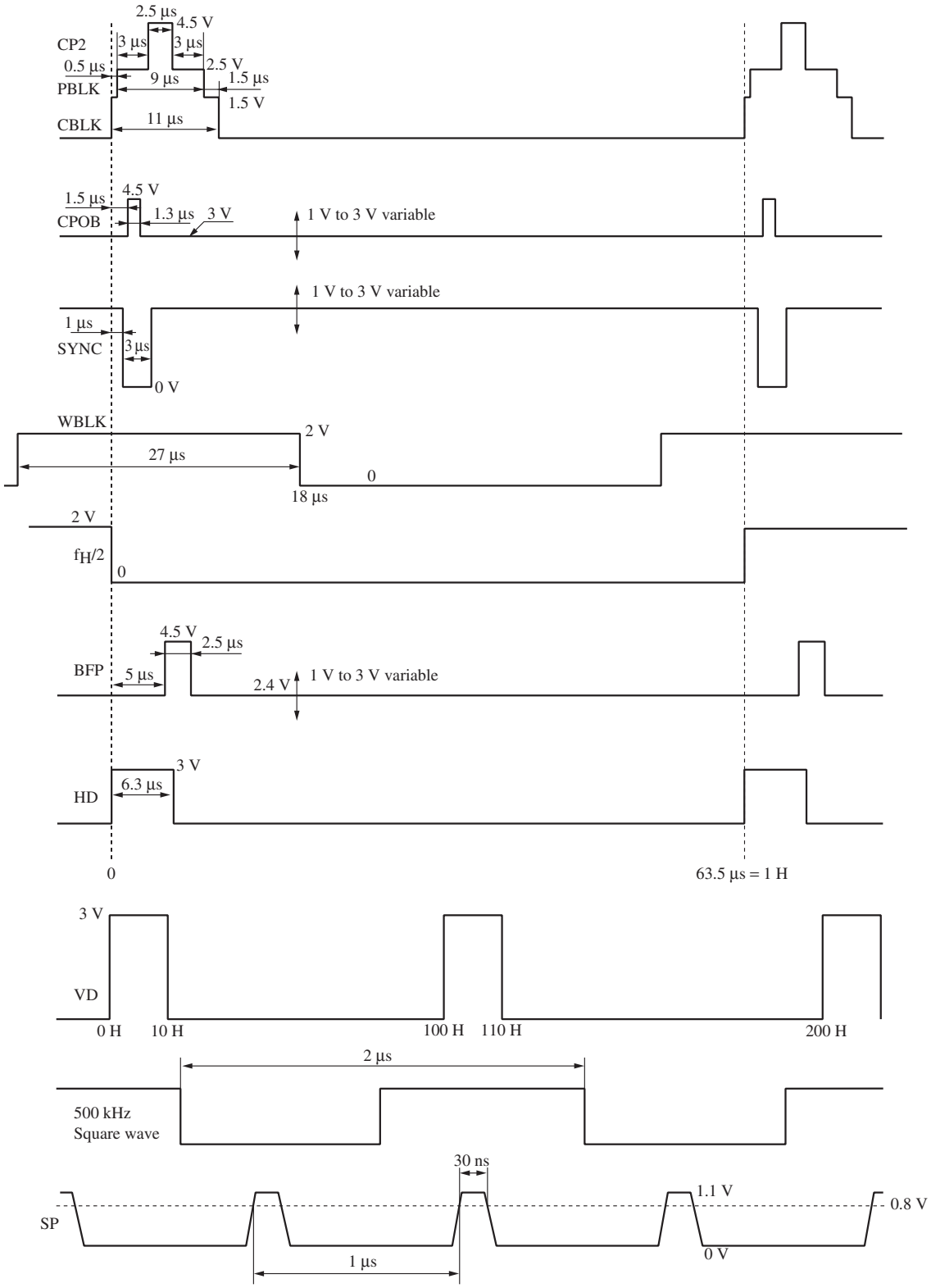
■ Electrical Characteristics at T_a = 25°C ± 2°C (continued)

• Input signal waveform

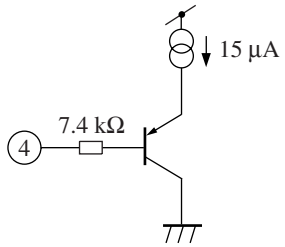
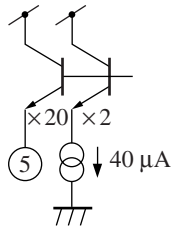
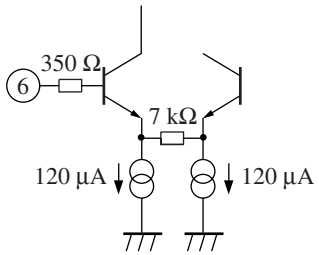
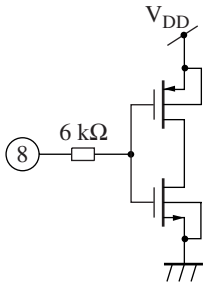
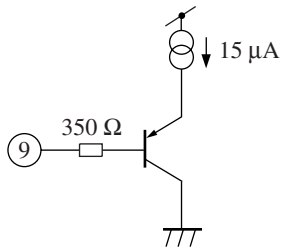


■ Electrical Characteristics at T_a = 25°C ± 2°C (continued)

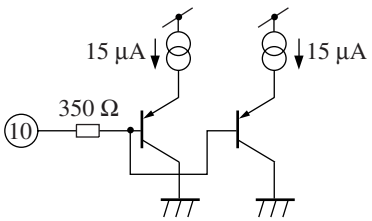
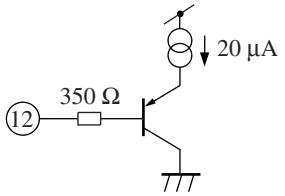
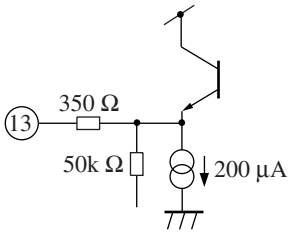
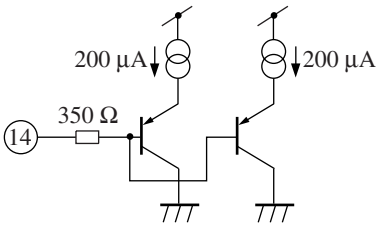
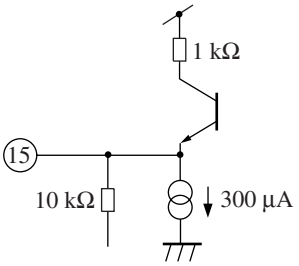
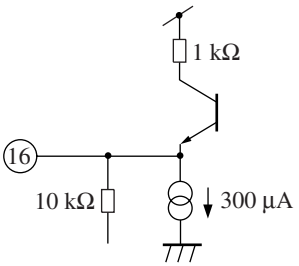
• Input signal waveform (continued)



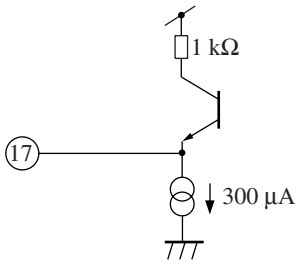
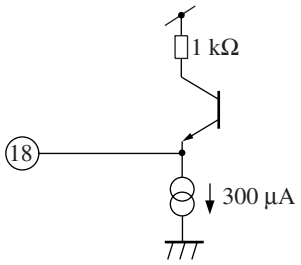
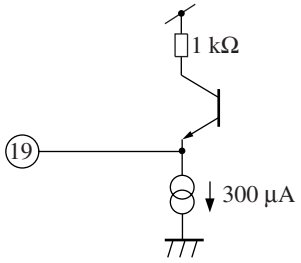
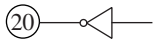
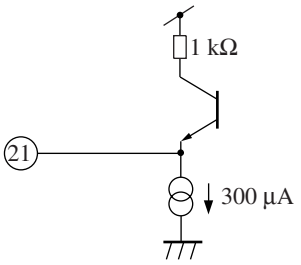
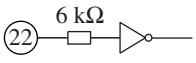
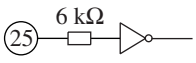
■ Terminal Equivalent Circuits

Pin No.	Pin name	Equivalent circuit	Description
1	N.C.	—	—
2	N.C.	—	—
3	N.C.	—	—
4	ELCDET IN		Comparator detection signal input for ELC
5	ALCOUT		Output for iris detection
6	WBLK IN		Iris signal gate pulse input
7	GND	—	Ground for signal processing system
8	FH2 IN		Color-difference-signal synchronizing-pulse input
9	ELC –H		Comparator "H" threshold for ELC

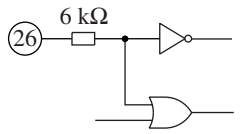
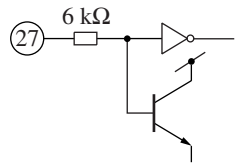
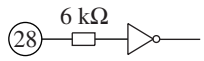
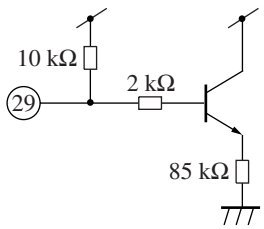
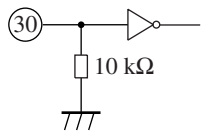
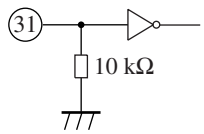
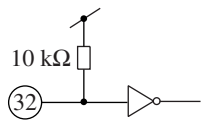
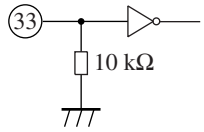
■ Terminal Equivalent Circuits (continued)

Pin No.	Pin name	Equivalent circuit	Description
10	ELC –M		Comparator "M" threshold for ELC
11	V_{CC}	—	V_{CC} for signal processing system
12	ELC –L		Comparator "L" threshold for ELC
13	ALC VROUT		VIDEO LEVEL dead-zone-addition output
14	VIDEO LEVEL		VIDEO LEVEL setting DC input
15	DATEST 1		DC monitor of internal DAC ch.14 output and output for other channel Connect pin 124 to ground for test mode.
16	DATEST 2		Output of internal DAC ch.4 for monitor

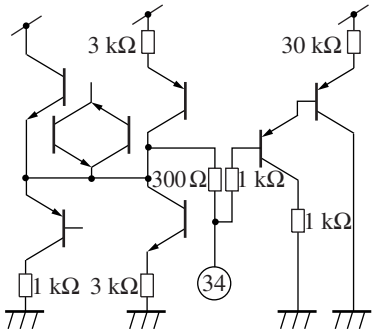
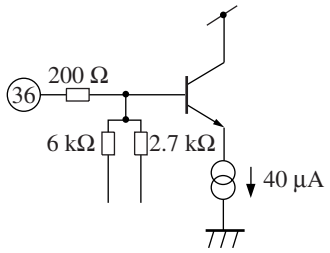
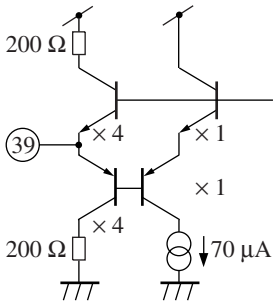
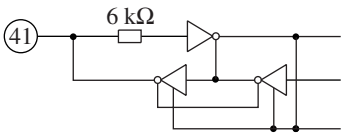
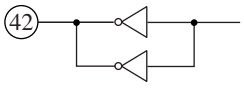
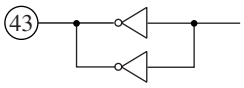
■ Terminal Equivalent Circuits (continued)

Pin No.	Pin name	Equivalent circuit	Description
17	DAOUT 1		External DAC ch.5 output
18	DAOUT 2		External DAC ch.21 output
19	DAOUT 3		External DAC ch.31 output
20	SCHTEST		SCH mode monitor
21	DAOUT 4		External DAC ch.20 output and DC monitor for other channel output Connect pin 124 to ground for test mode.
22	DATA		DAC data input
23	V_{SS}	—	Ground of logic circuits part
24	V_{DD}	—	Power supply monitor of logic circuits part: Approx. 3.5 V
25	VD		Vertical synchronization pulse input

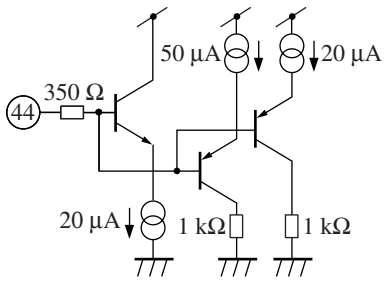
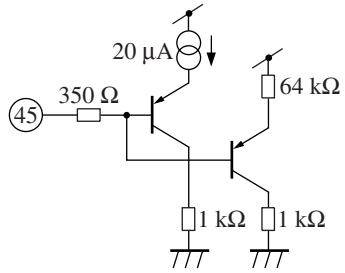
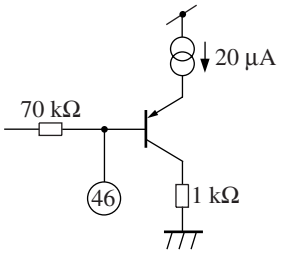
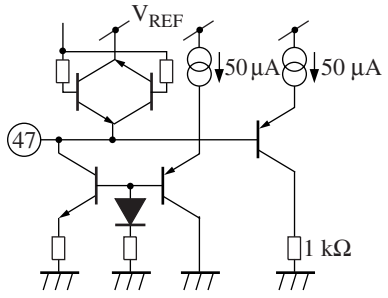
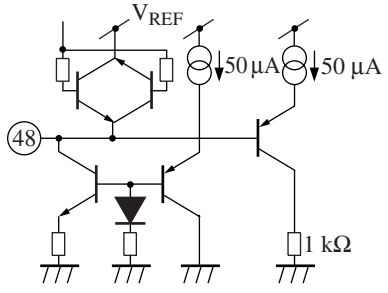
■ Terminal Equivalent Circuits (continued)

Pin No.	Pin name	Equivalent circuit	Description
26	HD		Horizontal synchronization pulse input
27	LL SW		LL/INT setting H: LL mode L: INT mode
28	NP SW		NTSC/PAL setting H: NTSC L: PAL
29	EXTLO		Power-on read setting H: DAC change disabled. L: DAC change enabled.
30	EXTLDB		DAC load pulse input 2 Ch.17 to ch.32 are assigned.
31	EXTLDA		DAC load pulse input 1 Ch.1 to ch.16 are assigned.
32	NCE		CE control input for EEPROM
33	RSTM		RST control input for EEPROM

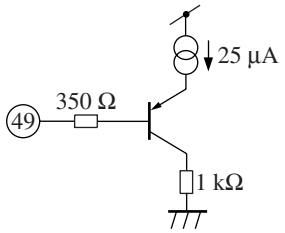
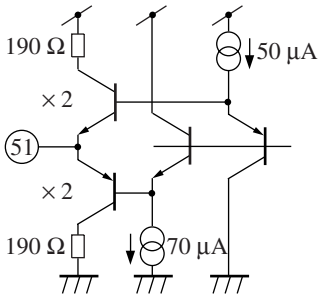
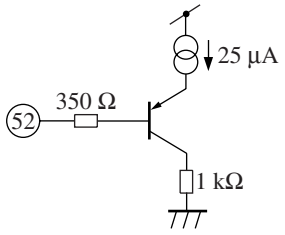
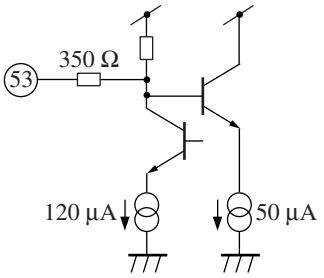
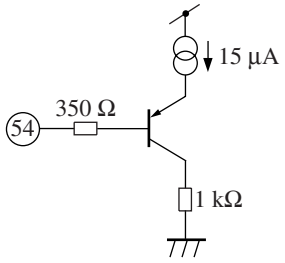
■ Terminal Equivalent Circuits (continued)

Pin No.	Pin name	Equivalent circuit	Description
34	FHLOCK		INT mode error pulse detection output: Approx. 2 VDC
35	GND	—	XTAL: ground of encoder system
36	XTAL IN		4 f_{SC} input
37	N.C.	—	—
38	N.C.	—	—
39	XTAL OUT		4 f_{SC} output
40	V_{CC}	—	XTAL: V_{CC} of encoder system
41	SCLK		DAC CLK I/O SLK input at adjusting CLK output at reading EEPROM data
42	RSTE		RST output for EEPROM
43	PONRE		CE output for EEPROM

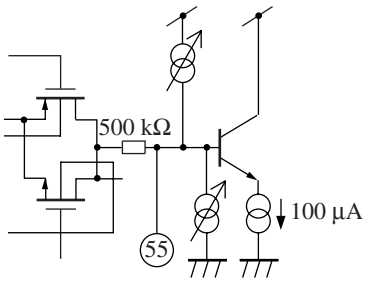
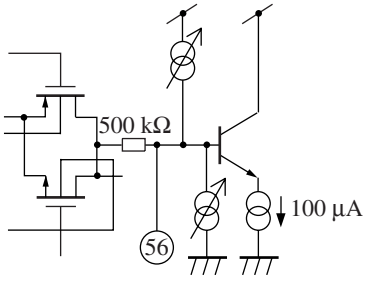
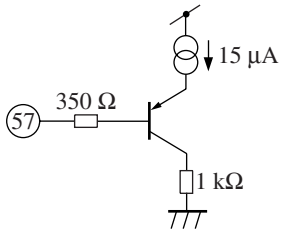
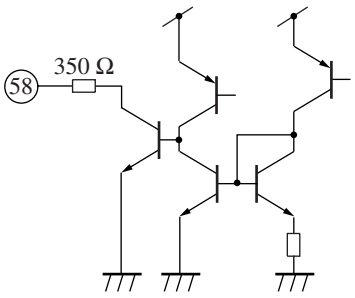
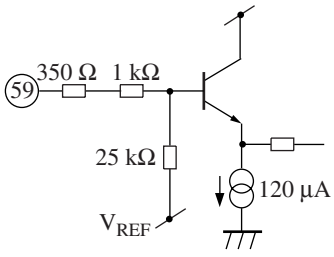
■ Terminal Equivalent Circuits (continued)

Pin No.	Pin name	Equivalent circuit	Description
44	CHC / BFP		Chroma high cut setting/BFP input and luminance High luminance threshold for WB-speed variation-setting
45	WBSTL / SYNC		Low luminance threshold for WB-speed variation-setting SYNC pulse input
46	WBDET		WB variable switch detection output
47	B-Y IN		B-Y signal encoder input
48	R-Y IN		R-Y signal encoder input

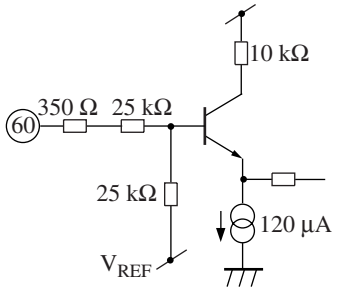
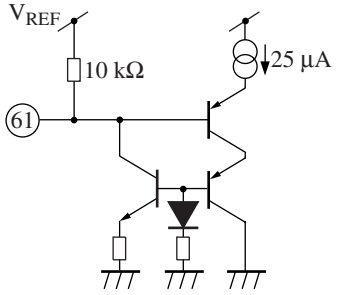
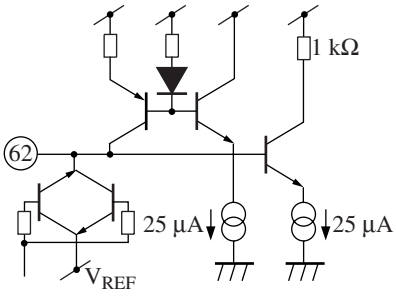
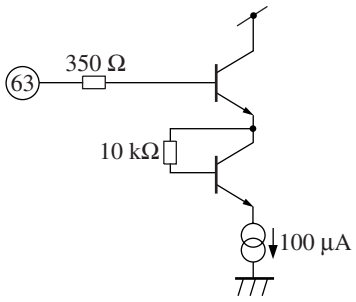
■ Terminal Equivalent Circuits (continued)

Pin No.	Pin name	Equivalent circuit	Description
49	BYDCL		Low color temperature inclination setting for B-Y color reproduction curve
50	V_{REF} IN	—	V_{REF} (pin 115) input
51	C OUT		Encoder chroma output
52	BYDCH		High color temperature inclination setting for B-Y color reproduction curve
53	BG MONI		Y-B color reproduction curve monitor
54	R-Y DET		R-Y comparator input for WB

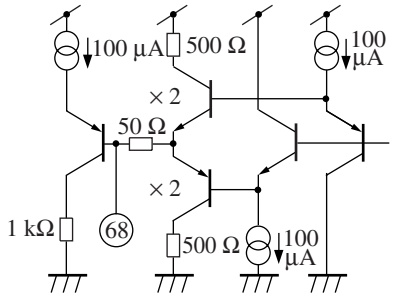
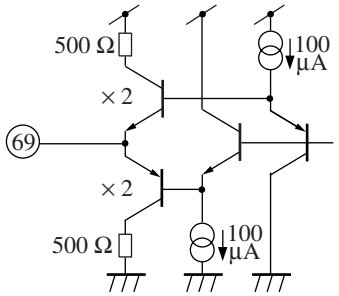
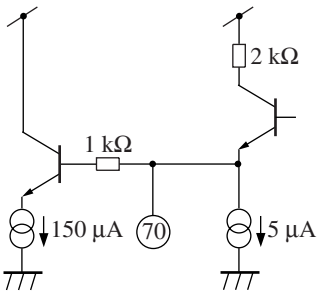
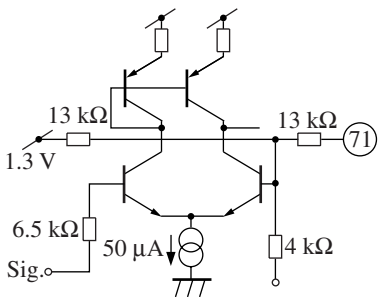
■ Terminal Equivalent Circuits (continued)

Pin No.	Pin name	Equivalent circuit	Description
55	RLIM IN		RWBDC detection
56	BLIM IN		BWBDC detection
57	B-Y DET		B-Y comparator input for WB
58	VD2 OUT		VD2 pulse separation output
59	VD2 DATA		Video signal + VD2 input

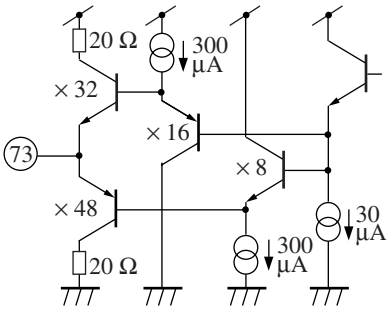
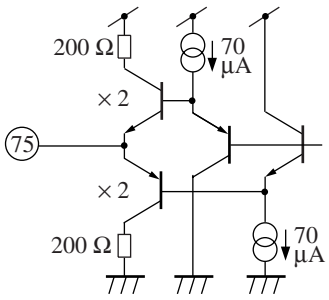
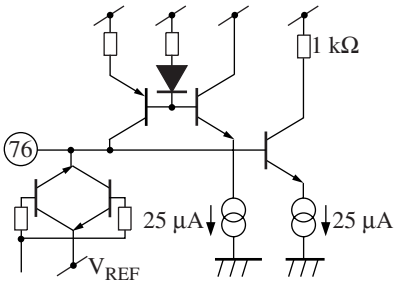
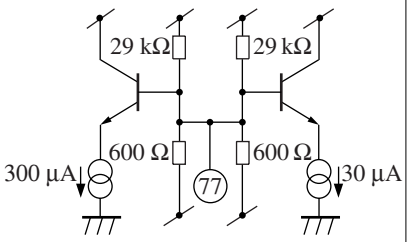
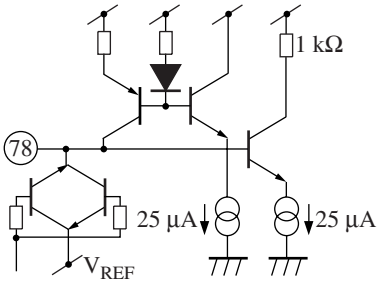
■ Terminal Equivalent Circuits (continued)

Pin No.	Pin name	Equivalent circuit	Description
60	75DR IN		Video signal input before 75-Ω termination
61	C IN		Chroma signal input for Y/C Mix
62	Y IN		Luminance signal input for Y/C Mix
63	WCLIP		Color difference signal high chroma clip setting
64	N.C.	—	—
65	N.C.	—	—
66	N.C.	—	—
67	N.C.	—	—

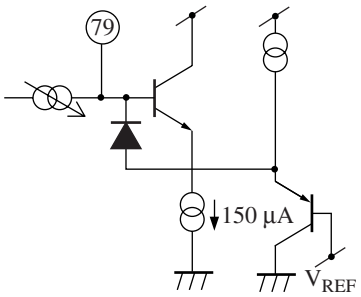
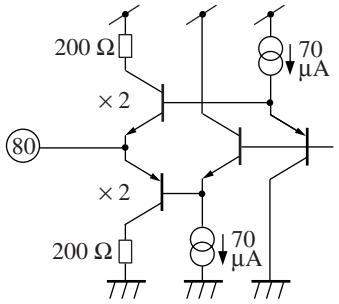
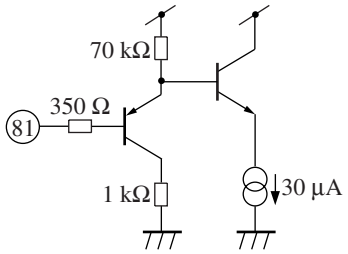
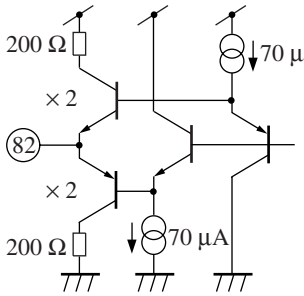
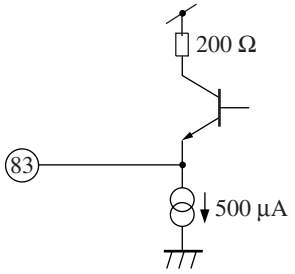
■ Terminal Equivalent Circuits (continued)

Pin No.	Pin name	Equivalent circuit	Description
68	TRAP		Setting to eliminate the frequency characteristic which is not required in Y/C Mix signal.
69	YC MIX OUT		Y/C Mix output
70	YC MIX IN		SYNC-chip clamping for Y/C Mix signal driver input
71	FB		FB input for V sag correction
72	V_{CC}	—	V_{CC} of Y/C Mix, driver and color reproduction circuit

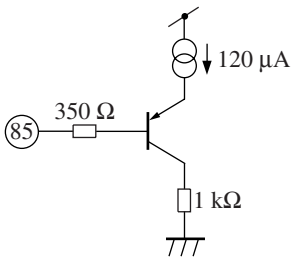
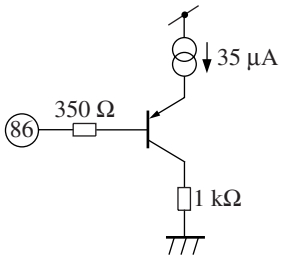
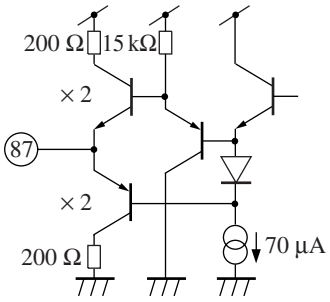
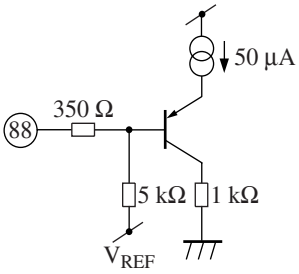
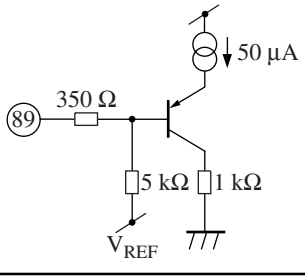
■ Terminal Equivalent Circuits (continued)

Pin No.	Pin name	Equivalent circuit	Description
73	75DR OUT		Driver output of 75 Ω
74	GND	—	GND of Y/C Mix, driver and color reproduction circuit
75	AGC OUT		YAGC output
76	0H GAMIN		Y gamma input non-delay signal
77	KNEE		Y gamma circuit knee-setting Normally open
78	1H GAMIN		Y gamma input delay signal

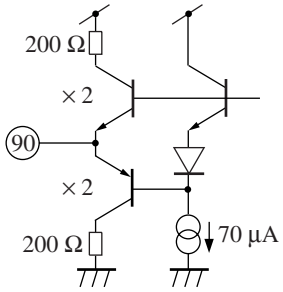
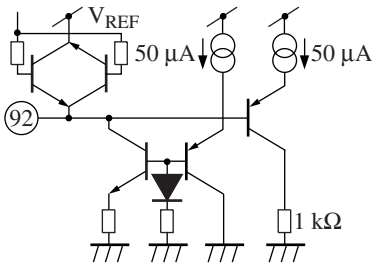
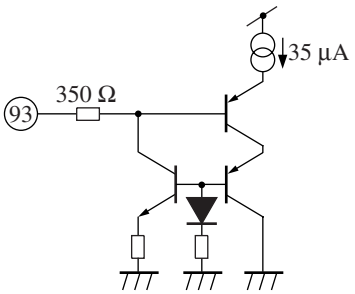
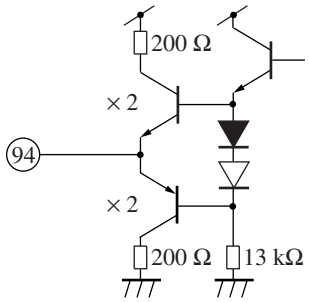
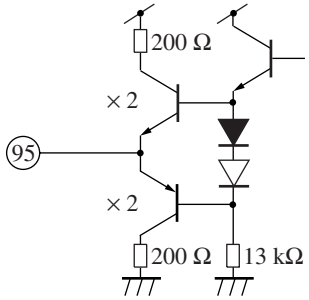
■ Terminal Equivalent Circuits (continued)

Pin No.	Pin name	Equivalent circuit	Description
79	Y GAM DCC		Capacitor pin for Y gamma output DC stabilization circuit
80	Y GAM OUT		Y gamma output
81	PED SET		Pedestal level setting
82	VAP OUT		V aperture output
83	Y OUT		Luminance signal H/L clip Pedestal-added output

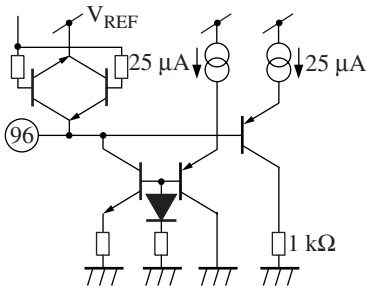
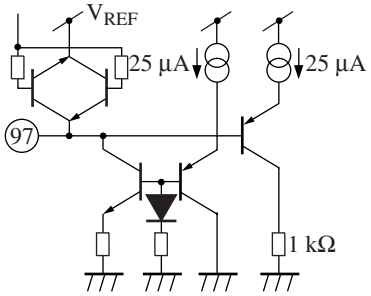
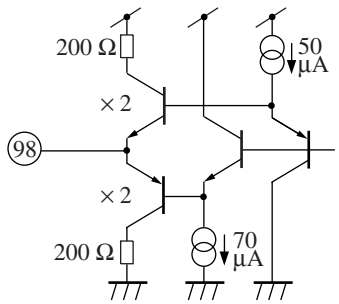
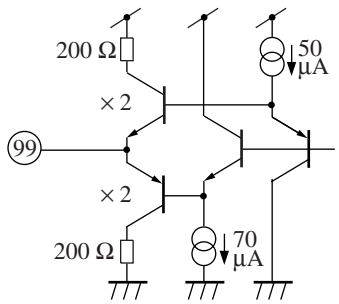
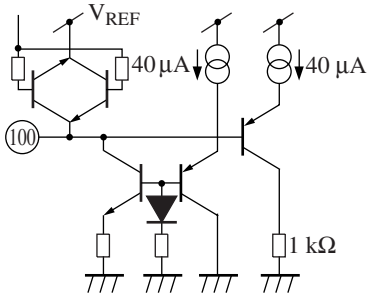
■ Terminal Equivalent Circuits (continued)

Pin No.	Pin name	Equivalent circuit	Description
84	GND	—	Ground for signal processing system
85	Y GAMMA IN		Y gamma signal H aperture generation circuit input
86	FADE		Fade setting 0.5 V or less in the state of fade
87	HAP OUT		H aperture output
88	HAP BC IN		H aperture coring input
89	VAP BC IN		V aperture coring input

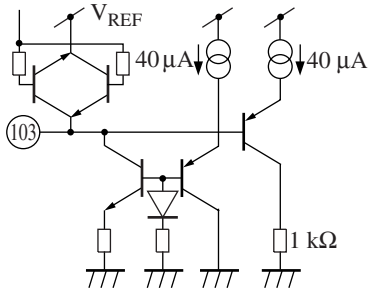
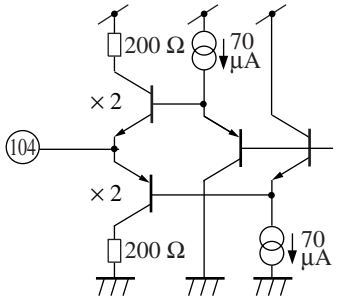
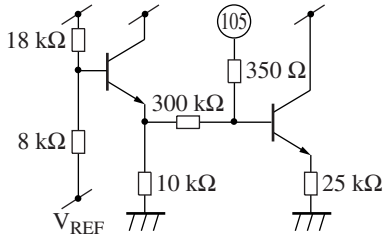
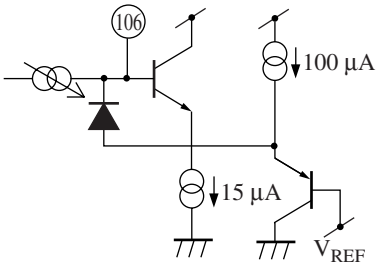
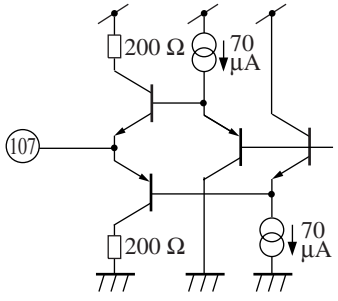
■ Terminal Equivalent Circuits (continued)

Pin No.	Pin name	Equivalent circuit	Description
90	BCLIP OUT		Luminance signal aperture Mix output
91	V_{CC}	—	Ground for signal processing system
92	PEDESET IN		Luminance + aperture signal input
93	LLSUP IN		AGC output detection DC input
94	B-Y OUT		B-Y signal output
95	R-Y OUT		R-Y signal output

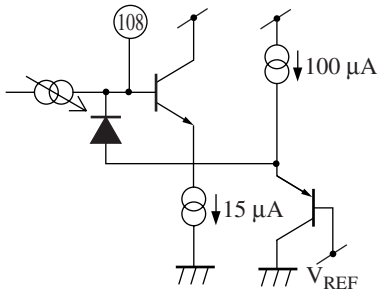
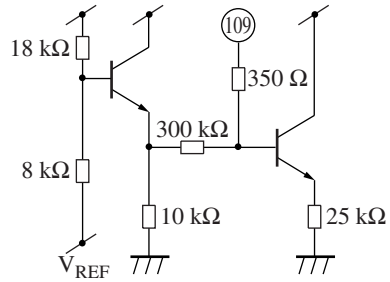
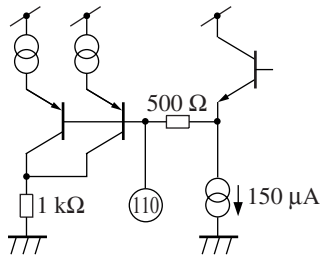
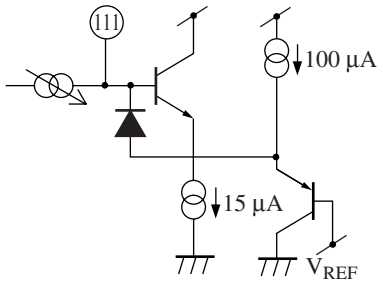
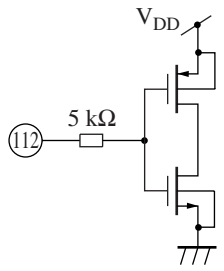
■ Terminal Equivalent Circuits (continued)

Pin No.	Pin name	Equivalent circuit	Description
96	C GAM R-YIN		Color difference signal input after synchronization (R-Y)
97	C GAM Y-BIN		Color difference signal input after synchronization (Y-B)
98	CSW Y-BOUT		Sync. color difference signal input (Y-B)
99	CSW R-YOUT		Color- difference-signal synchronizing-pulse input (R-Y)
100	C0H IN		Input of non-delay signal of S/H output

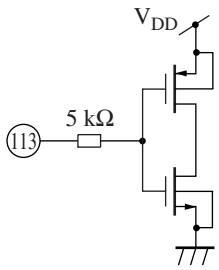
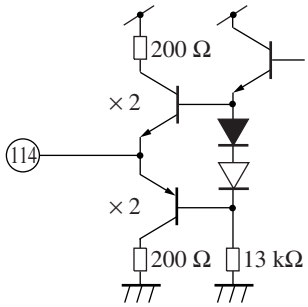
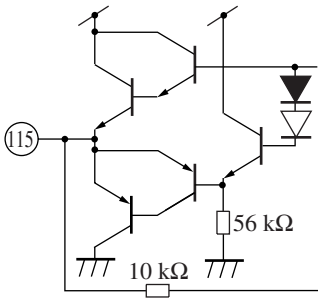
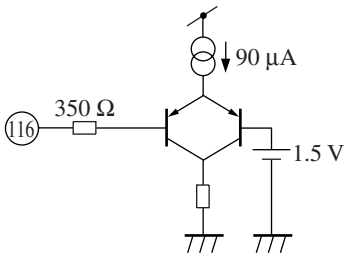
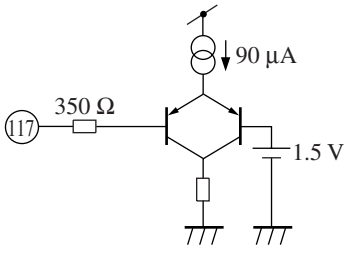
■ Terminal Equivalent Circuits (continued)

Pin No.	Pin name	Equivalent circuit	Description
101	N.C.	—	—
102	N.C.	—	—
103	C1H IN		Input of delay signal of S/H output
104	1HGC OUT2		Output of the amplifier for adjusting amplitude of CCD DL output (color difference)
105	1HGC IN2		Output of the amplifier for adjusting amplitude of CCD DL output (color difference)
106	R-Y DCC		Additional capacitor for DC control
107	1HGC OUT1		Output of the amplifier for adjusting amplitude of CCD DL output (luminance)

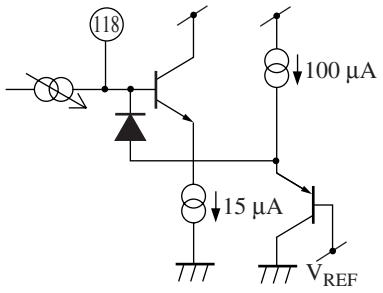
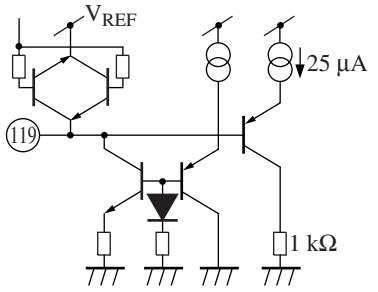
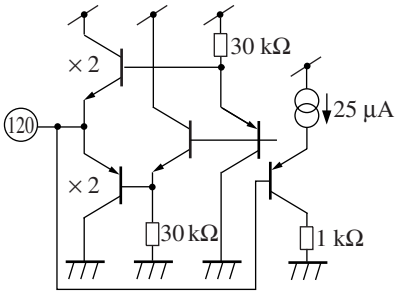
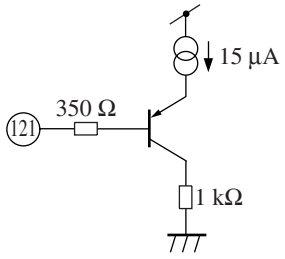
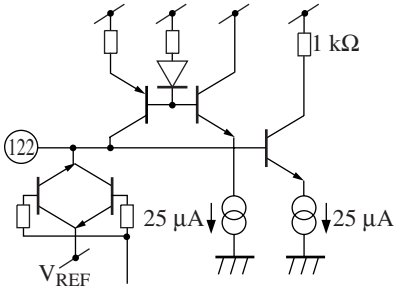
■ Terminal Equivalent Circuits (continued)

Pin No.	Pin name	Equivalent circuit	Description
108	B-Y DCC		Additional capacitor for DC control
109	1HGC IN1		Output of the amplifier for adjusting amplitude of CCD DL output (luminance)
110	CAGC TRAP		4 f_{SC} component elimination setting
111	S/H DCC1		Pin to add capacitor for DC stabilization of sample-and-hold output
112	ALC SW		ALC/ELC mode switching L: ALC mode H: ELC mode

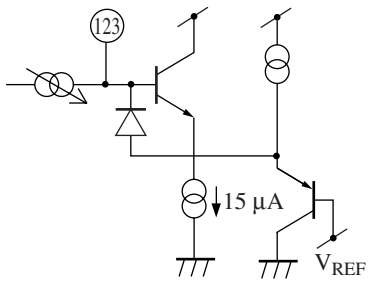
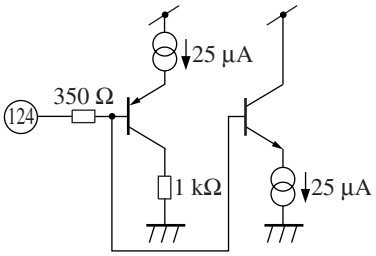
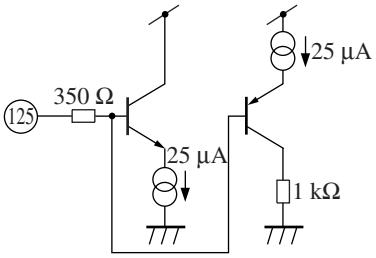
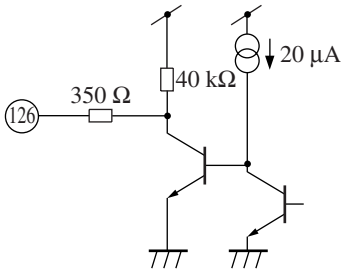
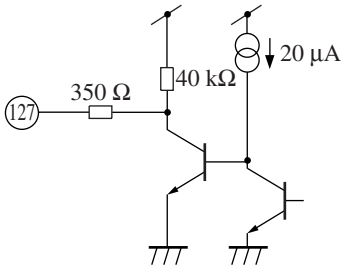
■ Terminal Equivalent Circuits (continued)

Pin No.	Pin name	Equivalent circuit	Description
113	AGC SW		AGC on/off switching L: On H: Off
114	S/H OUT		Color separation S/H output after WB
115	V_{REF} OUT		Reference voltage source: Approx. 1.75 V Impedance: Approx. 1 Ω
116	SP1		Sampling pulse input
117	SP2		Sampling pulse input

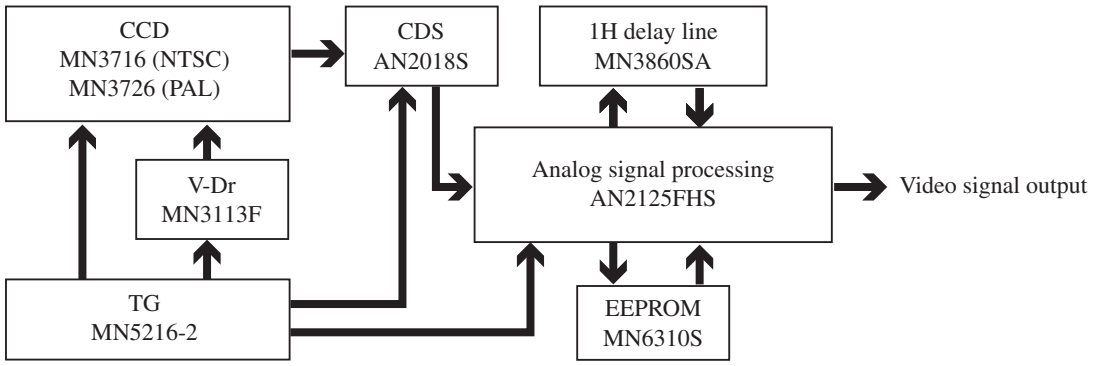
■ Terminal Equivalent Circuits (continued)

Pin No.	Pin name	Equivalent circuit	Description
118	S/H DCC 2		Pin to add capacitor for DC stabilization of sample-and-hold output
119	SIG IN		CDS signal input
120	AGC FB		FB pin of operational amplifier for AGC
121	AGC OP–		Negative input of operational amplifier for AGC
122	CDSSIG IRIS		CDS signal input (for iris)

■ Terminal Equivalent Circuits (continued)

Pin No.	Pin name	Equivalent circuit	Description
123	ALC DCC		Additional capacitor pin for stabilizing iris output
124	CPOB / HC		CPOB pulse input Luminance high-cut setting
125	CP2/PBLK/CBLK		CP2/PBLK/CBLK pulse input
126	DIST		ELC detection pulse
127	DRCT		ELC detection pulse
128	N.C.	—	—

■ Application Example (Analog CCD camera system)



Note) The AN2125FHS can provide the analog CCD camera system without microcomputers.

■ Usage Notes

1. Surge

Be careful handling the pins listed in the right-hand table since surge breakdown voltage for those pins are not so large. Those for the other pins are greater than 250 V.

	Pin No.	Surge Breakdown Voltage
+ surge	21	250 V
	30	240 V
	31	240 V
	32	230 V

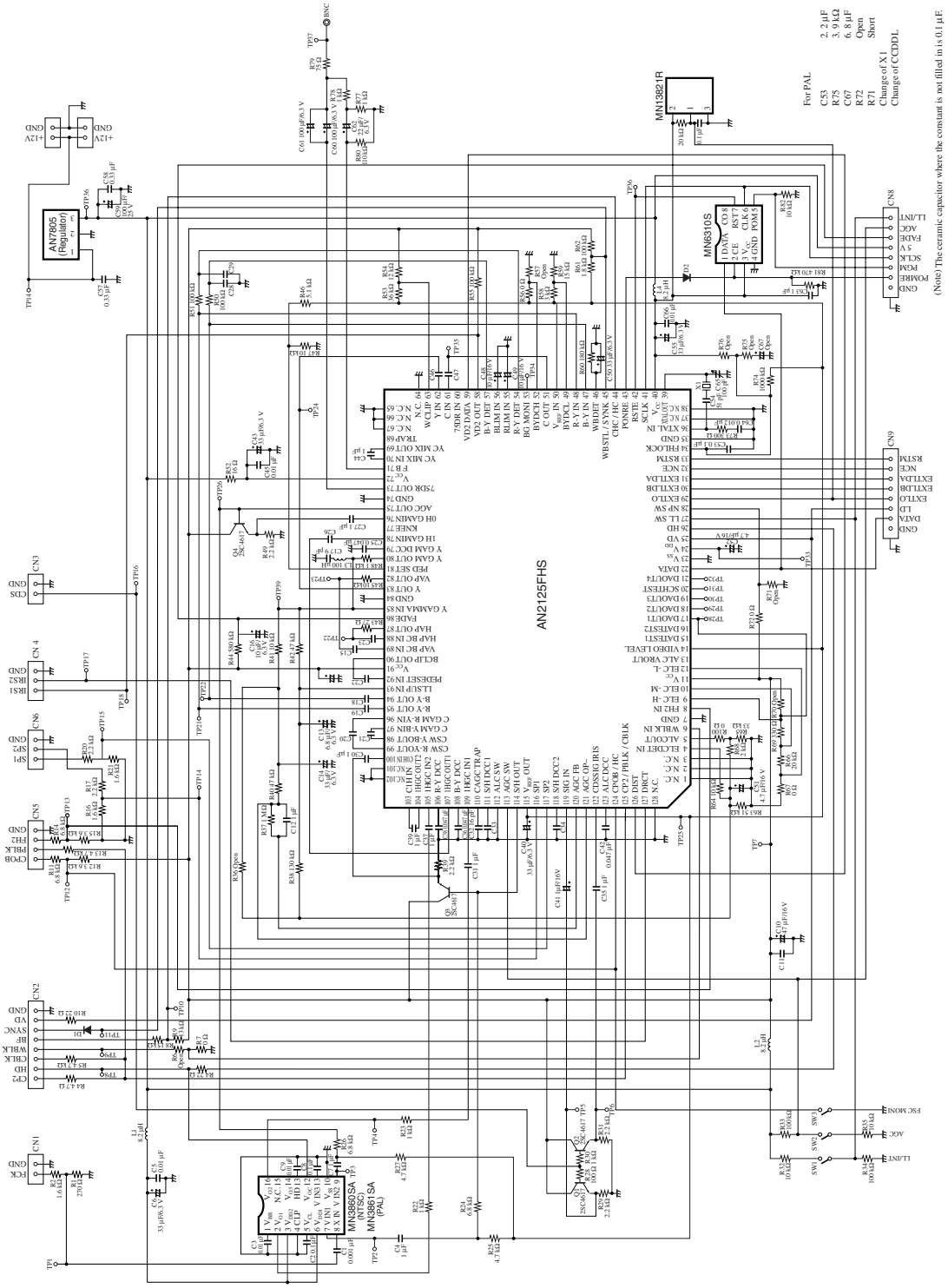
2. Power-on sequence

Apply the supply voltage to each V_{CC} pins (pins 11, 40, 72 and 91) simultaneously.

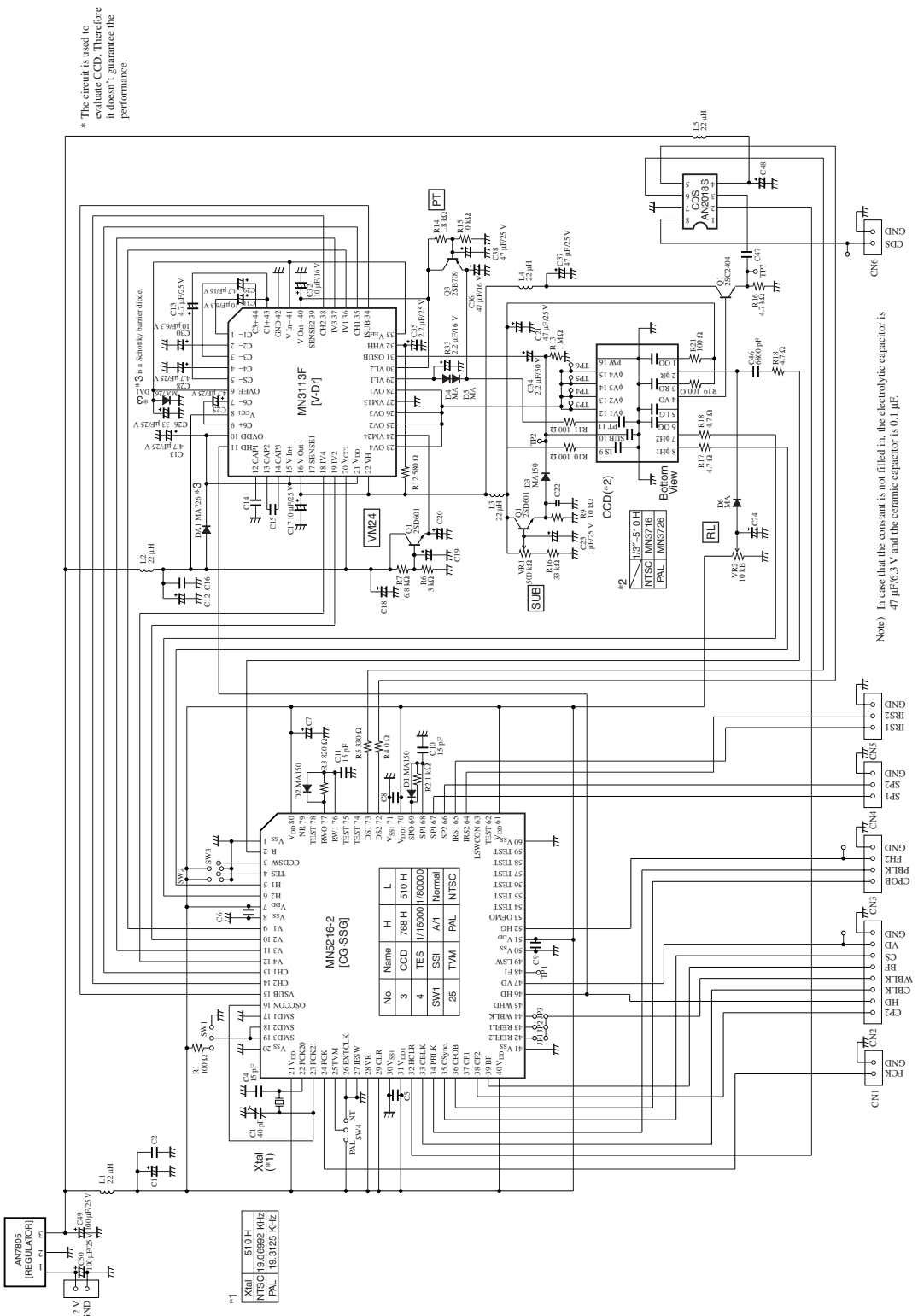
3. For external parts

1) Select and adjust a trimmer capacitor or variable capacitance diode for the 4 f_{SC} crystal oscillator so that the specified center frequency will be obtained when the crystal oscillator is in free-running operation.
2) The trap for the output on pin 80 suppresses f_{CK}/2. Select the trap by carefully considering the subject and other operating conditions.
3) Connect a power-on reset circuit to pin 29 of EXTLO against instantaneous power failure. Set the power-on reset circuit so that when the power restores, the pin 29 is surely short-circuited to GND and its voltage rises up after minimum 16 cycles of VD (VD: vertical scanning period) from having input a stable HD and VD pulses simultaneously with power application to this IC.

■ Application Circuit Examples (Board camera-1)

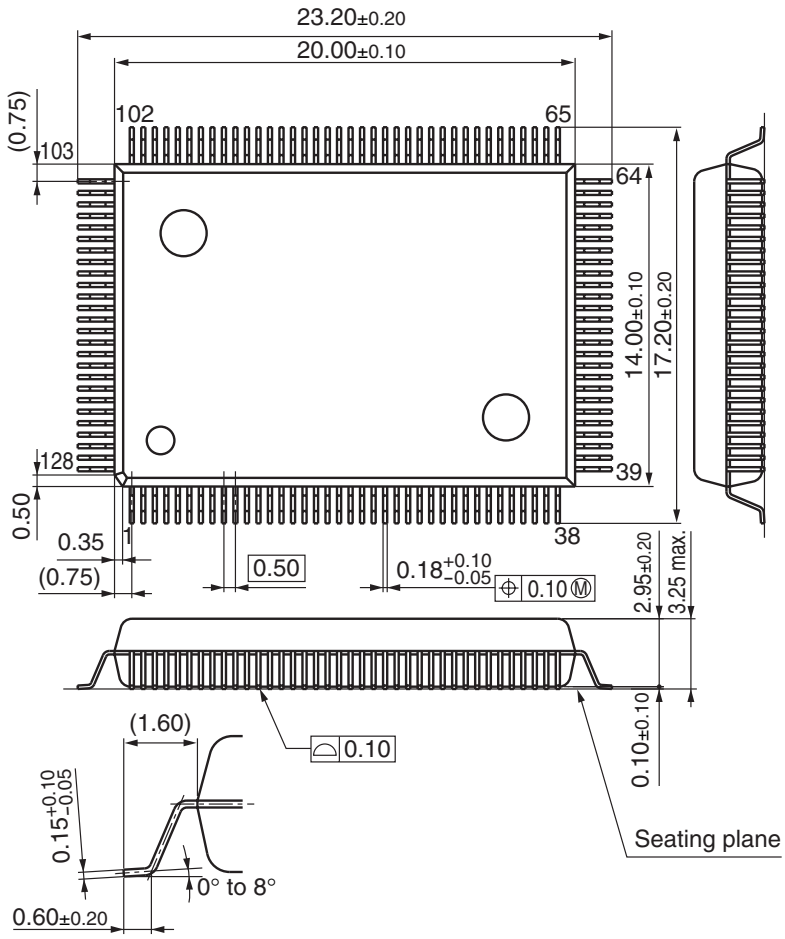


■ Application Circuit Examples (Board camera-2)



■ New Package Dimensions (Unit: mm)

• QFH128-P-1420E (Lead-free package)



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