WM2124

Dual 10-bit 40MSPS ADC

DESCRIPTION

The WM2124 is a dual channel 10-bit 40MSPS ADC which consumes only 275mW from a single 3.3V supply. The device is optimised for communications applications that require close matching between channels and a wide input bandwidth.

Input signals are differential for improved noise performance. Both A and B input channels are sampled simultaneously and are processed through matched signal paths of programmable gain amplifier (PGA) and 10-bit multistage pipeline ADC. A number of different input clock / output data formats are supported including 20-bits wide at the sampling rate or 10-bits wide at twice the sampling rate, with additional clock outputs supplied by the device to latch the output data.

System design and power requirements are further simplified by the provision of an on-chip precision voltage reference. Alternatively, external references can be used if higher precision references are required.

The device is programmed via a 3-wire serial interface which allows control of PGA gain setting (0 to 18dB range), clock / output data formatting, powerdown control and binary or two's complement number formatting.

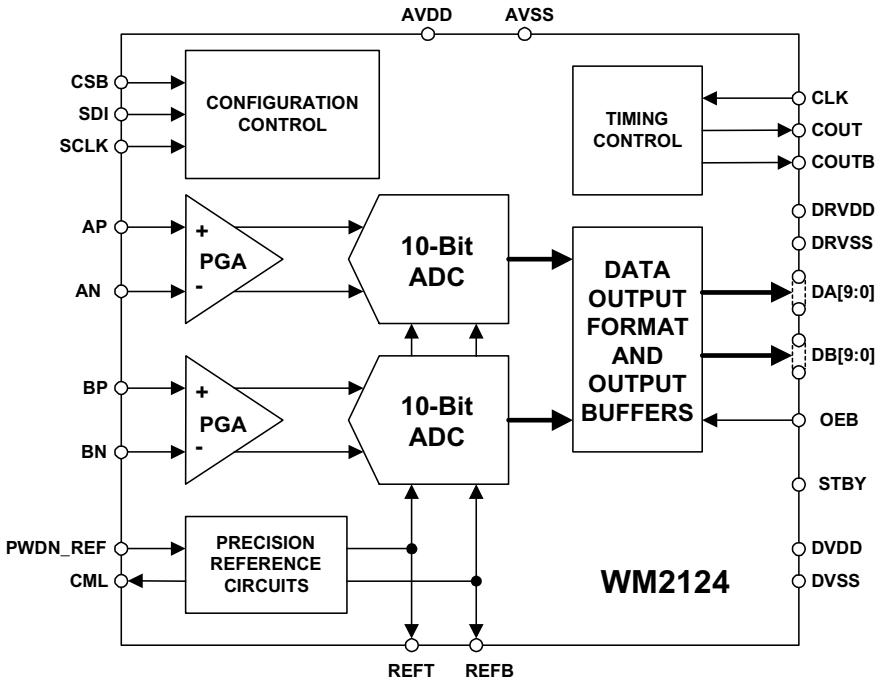
FEATURES

- Two 10-bit resolution ADCs
- 40MSPS conversion rate
- Simultaneous sampling differential input PGAs with 0 to 18dB gain
- Programmable clock / output data formats
  - 10-bit multiplexed or 20-bit wide output
  - Input clock at sample rate or twice sample rate for multiplexed output
  - Output clocks for output data sampling
- Precision internal voltage references
- Programmable via 3-wire serial interface
- Wide input bandwidth – 300MHz
- Low power – 275mW typical at 3.3V supplies
- Powerdown mode to less than 1mW
- 48-pin TQFP package

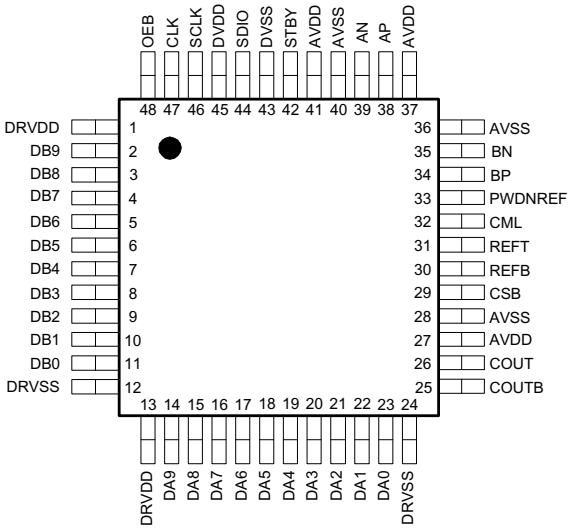
APPLICATIONS

- I/Q demodulation for
  - Wireless Local Loop (WLL)
  - Set Top Box (STB)
  - Cable Modem
- IF and Baseband Digitisation
- Test Instrumentation
- Medical Imaging

BLOCK DIAGRAM



PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMP. RANGE	PACKAGE
WM2124CFT	0 to +70°C	48-pin TQFP
WM2124IFT	-40 to +85°C	48-pin TQFP

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	DRVDD	Supply	Positive digital output driver supply
2	DB9	Digital Output	Digital output for Q channel in dual bus mode bit 9 (msb)
3	DB8	Digital Output	Digital output for Q channel in dual bus mode bit 8
4	DB7	Digital Output	Digital output for Q channel in dual bus mode bit 7
5	DB6	Digital Output	Digital output for Q channel in dual bus mode bit 6
6	DB5	Digital Output	Digital output for Q channel in dual bus mode bit 5
7	DB4	Digital Output	Digital output for Q channel in dual bus mode bit 4
8	DB3	Digital Output	Digital output for Q channel in dual bus mode bit 3
9	DB2	Digital Output	Digital output for Q channel in dual bus mode bit 2
10	DB1	Digital Output	Digital output for Q channel in dual bus mode bit 1
11	DB0	Digital Output	Digital output for Q channel in dual bus mode bit 0 (lsb)
12	DRVSS	Ground	Negative digital output driver supply
13	DRVDD	Supply	Positive digital output driver supply
14	DA9	Digital Output	Digital output for I (dual bus mode), I/Q (single bus mode) bit 9 (msb)
15	DA8	Digital Output	Digital output for I (dual bus mode), I/Q (single bus mode) bit 8
16	DA7	Digital Output	Digital output for I (dual bus mode), I/Q (single bus mode) bit 7
17	DA6	Digital Output	Digital output for I (dual bus mode), I/Q (single bus mode) bit 6
18	DA5	Digital Output	Digital output for I (dual bus mode), I/Q (single bus mode) bit 5
19	DA4	Digital Output	Digital output for I (dual bus mode), I/Q (single bus mode) bit 4
20	DA3	Digital Output	Digital output for I (dual bus mode), I/Q (single bus mode) bit 3
21	DA2	Digital Output	Digital output for I (dual bus mode), I/Q (single bus mode) bit 2
22	DA1	Digital Output	Digital output for I (dual bus mode), I/Q (single bus mode) bit 1
23	DA0	Digital Output	Digital output for I (dual bus mode), I/Q (single bus mode) bit 0 (lsb)
24	DRVSS	Ground	Negative digital output driver supply
25	COUTB	Digital Output	Inverted latch clock output for digital outputs
26	COUT	Digital Output	Latch clock output for digital outputs
27	AVDD	Supply	Positive Analogue Supply

PIN	NAME	TYPE	DESCRIPTION
28	AVSS	Ground	Negative Analogue Supply
29	CSB	Digital Input	Serial interface chip select
30	REFB	Analogue Input/Output	ADC bottom reference
31	REFT	Analogue Input/Output	ADC top reference
32	CML	Analogue Output	ADC reference common mode level output
33	PWDNREF	Digital Input	Powerdown control for internal ADC reference generator
34	BP	Analogue Input	Positive input for the B signal channel
35	BN	Analogue Input	Negative input for the B signal channel
36	AVSS	Ground	Negative Analogue Supply
37	AVDD	Supply	Positive Analogue Supply
38	AP	Analogue Input	Positive input for the A signal channel
39	AM	Analogue Input	Negative input for the A signal channel
40	AVSS	Ground	Negative Analogue Supply
41	AVDD	Supply	Positive Analogue Supply
42	STBY	Digital Input	Standby control
43	DVSS	Ground	Negative Digital Supply
44	SDIO	Digital Input	Serial interface data input/output
45	DVDD	Supply	Positive Digital Supply
46	SCLK	Digital Input	Serial interface clock
47	CLK	Digital Input	Conversion clock. The input is sampled on each rising edge of CLK when using a 40MHz input and alternate rising edges when using an 80MHz clock.
48	OEB	Digital Input	Output enable. A LOW on this terminal will enable the data output bus, COUT and COUTB

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

CONDITION	MIN	MAX
Digital supply voltage, DVDD to DVSS	-0.5V	+3.6V
Digital output driver supply voltage, DRVDD to DRVSS	-0.5V	+3.6V
Analogue supply voltage, AVDD to AVSS	-0.5V	+3.6V
Maximum ground difference between AVSS, DVSS and DRVSS	-0.5V	+0.5V
Voltage range digital inputs	DVSS – 0.5V	DVDD + 0.5V
Voltage range analogue inputs (includes CLK pin)	AVSS - 0.5V	AVDD + 0.5V
Operating temperature range, T_A	-45°C	+85°C
Storage temperature	-65°C	+150°C
Lead temperature (1.6mm from case for 10 seconds)		+300°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Power Supply						
Digital supply range	DVDD		3.0	3.3	3.6	V
Digital output driver supply range	DRVDD		3.0	3.3	3.6	V
Analogue supply range	AVDD		3.0	3.3	3.6	V
Ground	DVSS, DRVSS, AVSS			0		V
Analogue and Reference Inputs						
Reference Input Voltage (top)	VREFT	FCLK = 1MHz to 80MHz	1.9	2.0	2.15	V
Reference Input Voltage (bottom)	VREFB	FCLK = 1MHz to 80MHz	0.95	1.0	1.1	V
Reference Voltage Differential	VREFT-VREFB	FCLK = 1MHz to 80MHz	0.95	1.0	1.1	V
Reference Input Resistance	RREF	FCLK = 80MHz		1650		Ω
Reference Input Current	IREF	FCLK = 80MHz		0.62		mA
Analogue Input Voltage (differential)	VIN					V
Analogue Input Voltage (single ended) Note 1	VIN		-1		1	V
Analogue Input Capacitance	CI		CML – 1.0		CML + 1.0	pF
Clock Input Note 2				8		V
Analogue Outputs						
CML Voltage				AVDD/2		V
CML Output Resistance				2.3		kΩ
Digital Inputs						
High-Level Input Voltage			2.4		DVDD	V
Low-Level Input Voltage			DGND		0.8	V
Input Capacitance				5		pF
Clock Period			12.5			ns
Pulse Duration		Clock HIGH or LOW	5.25			ns
Clock Period			25			ns
Pulse Duration		Clock HIGH or LOW	11.25			ns

Notes

1. Applies only when the signal reference input connects to CML.
2. Clock pin is referenced to AVDD/AVSS.

ELECTRICAL CHARACTERISTICS

Test Conditions:
over recommended operation conditions with FCLK = 80MHz and use of internal voltage references, and PGA gain = 0dB, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Accuracy						
Integral nonlinearity	INL	nternal References (Note 1)	-1.5	±0.4	+1.5	LSB
Differential nonlinearity	DNL	nternal References (Note 2)	-0.9	±0.4	+1.0	LSB
Zero error (Note 3)		AVDD = DVDD = DRVDD = 3.3V External References (Note3)		0.12		% of FS
Full-Scale error				0.28		% of FS
Gain error				0.24		% of FS
Missing codes			No missing codes guaranteed			
References						
REFT output voltage	V_{REFTO}	Absolute Min/Max Values Valid and Tested for AVDD = 3.3V	1.9	2.0	2.1	V
REFB output voltage	V_{REFBO}		0.95	1.0	1.05	V
Differential Reference Voltage	REFT-RERB		0.95	1.0	1.05	V
Power Supplies						
IDD Operating Supply Current	AVDD	AVDD = DVDD = DRVDD = 3.3V, CL = 10pF, VIN = 3.5MHz, -1dBFS		64	72	mA
	DVDD			1.7	2.2	
	DRVDD			18	27	
Power Dissipation	PD	PWDN_REF = L		275	345	mW
		PWDN_REF = H		240	300	
Standby Power	PD(STBY)	STDBY = H, CLK held HIGH or LOW		95	150	uW
Power-Up Time for all references from Standby	tPD			550		ms
Wake up Time	tWU	External Reference		40		us
Digital Inputs						
High-Level Input Current on Digital Inputs incl. CLK	I_{IH}	AVDD = DVDD = DRVDD = 3.6V	-1		+1	uA
Low-Level Input Current on Digital Inputs incl. CLK	I_{IL}		-1		+1	uA
Digital Outputs						
High-Level Output Voltage	V_{OH}	AVDD = DVDD = DRVDD = 3.0V at I_{OH} = 50uA, Digital Outputs Forced HIGH	2.8	2.96		V
Low-Level Output Voltage	V_{OL}	AVDD = DVDD = DRVDD = 3.0V at I_{OH} = 50uA, Digital Outputs Forced LOW		0.04	0.2	V
Output Capacitance	C_O			5		pF
High-Impedance State Output Current to High-Level	I_{OZH}	AVDD = DVDD = DRVDD = 3.6V	-1		+1	uA
High-Impedance State Output Current to Low-Level	I_{OZL}		-1		+1	uA
Data Output Rise and Fall Time		C_{LOAD} = 10pF, Single-Bus Mode		3		ns
		C_{LOAD} = 10pF, Dual-Bus Mode		5		ns

Notes

1. INL refers to the deviation of each individual code from a line drawn from zero to full-scale. The point used as zero occurs 1/2LSB before the first code transition. The full-scale point is defined as a level 1/2LSB beyond the last code transition. The deviation is measured from the center of each particular code to the best fit line between these two points.

2. An ideal ADC exhibits code transitions that are exactly 1LSB apart. DNL is the deviation from this ideal value. Therefore this measure indicates how uniform the transfer function step sizes are. The ideal step size is defined here as the step size for the device under test, (i.e., (the last transition level-first transition level)/(2^n-2)). Using this definition for DNL separates the effects of gain and offset error. A minimum DNL better than -1LSB ensures no mission codes.
3. Zero is defined as the difference in analogue input voltage – between the ideal voltage and the actual voltage – that will switch the ADC output from code 0 to code 1. The ideal voltage level is determined by adding the voltage corresponding to 1/2LSB to the bottom reference level. The voltage corresponding to 1LSB is found from the difference of top and bottom references divided by the number of ADC output levels (1024). Full scale error is defined as the difference in analogue input voltage – between the ideal voltage and the actual voltage – that will switch the ADC output from code 1022 to 1023. The ideal voltage level is determined by subtracting the voltage corresponding to 1.5LSB from the top reference level. The voltage corresponding to 1LSB is found from the difference of top and bottom references divided by the number of ADC output levels (1024).

DYNAMIC PERFORMANCE (NOTE 1)

Test Conditions:
$T_A = T_{MIN}$ to T_{MAX}, AVDD = DVDD = DRVDD = 3.3V, f_{IN} = -1dBFS, Internal Reference, f_{CLK} = 80MHz, f_S = 40MSPS, Differential Input Range = 2Vp-p, and PGA Gain = 0dB, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dynamic Performance						
Effective number of bits	ENOB	f_{IN} = 3.5MHz		9.7		bits
		f_{IN} = 10.5MHz	9.3	9.7		
		f_{IN} = 20MHz		9.6		
Spurious free dynamic range	SFDR	f_{IN} = 3.5MHz		75		dB
		f_{IN} = 10.5MHz	69	73		
		f_{IN} = 20MHz		70.5		
Total harmonic distortion	THD	f_{IN} = 3.5MHz		-71		dB
		f_{IN} = 10.5MHz		-71	-66	
		f_{IN} = 20MHz		-68		
Signal to noise ratio	SNR	f_{IN} = 3.5MHz		60.5		dB
		f_{IN} = 10.5MHz		60.5		
		f_{IN} = 20MHz		60		
Signal to noise and distortion ratio	SINAD	f_{IN} = 3.5MHz		60		dB
		f_{IN} = 10.5MHz	57	60		
		f_{IN} = 20MHz		60		
Analogue Input Bandwidth		See Note 2		300		MHz
2-Tone Intermodulation Distortion	IMD	F1 = 9.5MHz, F2 = 9.9MHz		-68		dBc
A/B Channel Crosstalk				-75		dBc
A/B Channel Offset Mismatch				0.016	1.75	% of FS
A/B Channel Full-Scale Error Mismatch				0.025	1.0	% of FS

Notes

1. These specifications refer to a 25Ω series resistor and 15pF differential capacitor between A/B+ and A/B- inputs; any source impedance will bring the bandwidth down.
2. Analogue input bandwidth is defined as the frequency at which the sampled input signal is 3dB down on unity gain and is limited by the input switch impedance.

PGA SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PGA						
Gain Range				0 to 18		dB
Gain Step Size (Note 1)				0.5826		dB
Gain Error (Note 2)			-0.15	±0.025	+0.5	dB
Control Bits per Channel					5	Bits

Notes

1. Refer to Table 2, PGA Gain Code. Ideal step size: 18.0618dB/31 = 0.5826dB
2. Deviation from ideal. Refer to Table 2, all gain settings.

TIMING REQUIREMENTS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Clock Rate	f_{CLK}		1		80	MHz
Conversion Rate			1		40	MSPS
Clock Duty Cycle (40MHz)			45	50	55	%
Clock Duty Cycle (80MHz)			42	50	58	%
Output Delay Time	$t_{d(o)}$	C_L = 10pF		9	14	ns
Mux Setup Time	$t_{s(m)}$		9	10.4		ns
Mux Hold Time	$t_{h(m)}$	C_L = 10pF	1.7	2.1		ns
Output Setup Time	$t_{s(o)}$	C_L = 10pF	9	10.4		ns
Pipeline Delay (latency, channels A and B)	$t_{d(pipe)}$	MODE = 0, SELB = 0		8		CLK Cycles
Pipeline Delay (latency, channels A and B)	$t_{d(pipe)}$	MODE = 1, SELB = 0		4		CLK Cycles
Pipeline Delay (latency, channel A)	$t_{d(pipe)}$	MODE = 0, SELB = 1		8		CLK Cycles
Pipeline Delay (latency, channel B)	$t_{d(pipe)}$	MODE = 0, SELB = 1		9		CLK Cycles
Pipeline Delay (latency, channel A)	$t_{d(pipe)}$	MODE = 1, SELB = 1		8		CLK Cycles
Pipeline Delay (latency, channel B)	$t_{d(pipe)}$	MODE = 1, SELB = 1		9		CLK Cycles
Output Hold Time	$t_{h(o)}$	C_L = 10pF	1.5	2.2		ns
Aperture Delay Time	$t_{d(a)}$			3		ns
Aperture Jitter	$t_{j(a)}$			1.5		ps, rms
Disable Time, OEB Rising to Hi-Z	t_{dis}			5	8	ns
Enable Time, OEB Falling to Valid Data	t_{en}			5	8	ns

Notes

1. All internal operations are performed at a 40MHz clock rate.

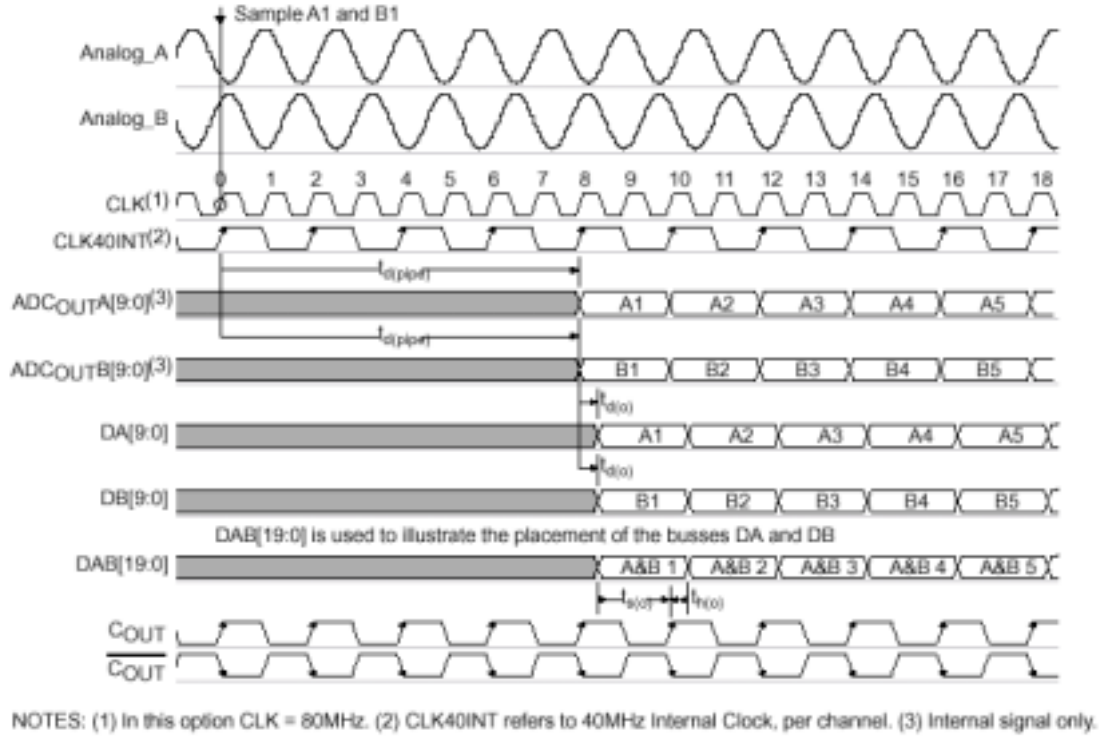
SERIAL INTERFACE TIMING

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Maximum Clock Rate	f_{SCLK}	20			MHz
SCLK Pulse Width HIGH	t_{WH}	25			ns
SCLK Pulse Width LOW	t_{WH}	25			ns
Setup Time, CSB LOW Before First Negative SCLK Edge	$t_{SU(CS\_CK)}$	5			ns
CBS High Width	$t_{WH(CS)}$	10			ns
Setup Time, 16th Negative SCLK Edge before CSB Rising Edge	$t_{SU(C16\_CK)}$	5			ns
Setup Time, Data Ready Before SCLK Falling Edge	$t_{SU(D)}$	5			ns
Hold Time, Data Held Valid after SCLK Falling Edge	$t_{SU(H)}$	5			ns

TIMING OPTIONS

OPERATING MODE	MODE	SELB	TIMING DIAGRAM FIGURE
80MHz Input Clock, Dual-Bus Output, C_{OUT} = 40MHz	0	0	1
40MHz Input Clock, Dual-Bus Output, C_{OUT} = 40MHz	1	0	2
80MHz Input Clock, Single-Bus Output, C_{OUT} = 40MHz	0	1	3
80MHz Input Clock, Single-Bus Output, C_{OUT} = 80MHz	1	1	4

TIMING DIAGRAMS



NOTES: (1) In this option CLK = 80MHz. (2) CLK40INT refers to 40MHz Internal Clock, per channel. (3) Internal signal only.

Figure 1 Timing Diagram, Dual Bus Output - Option 1

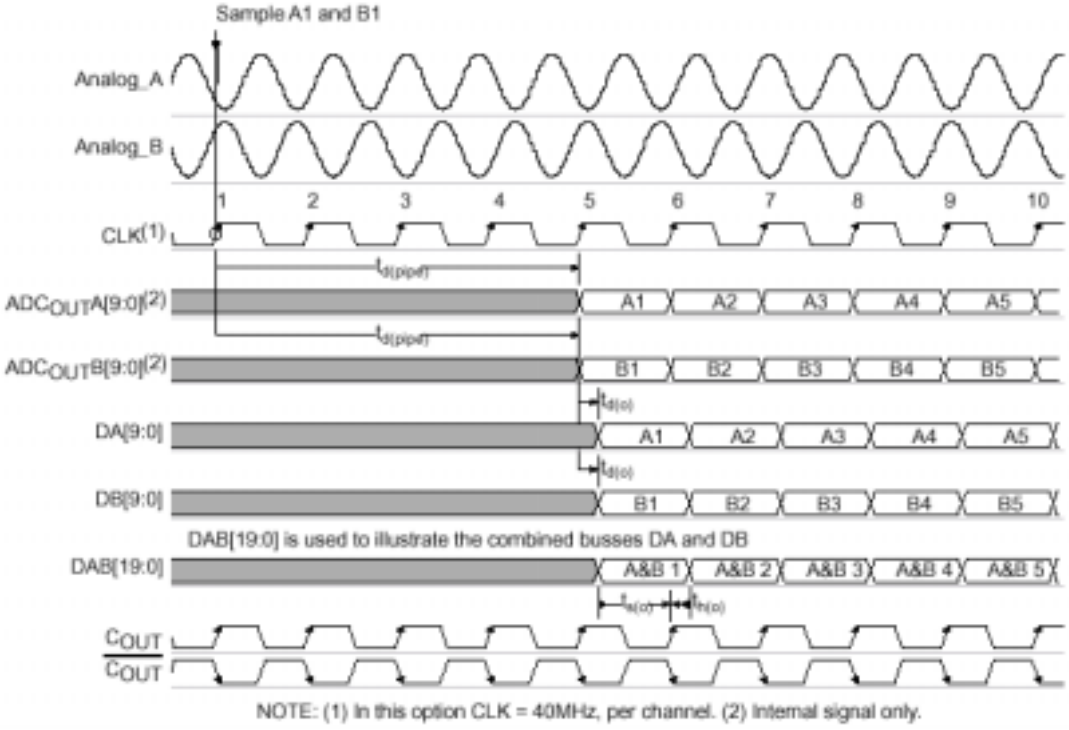


Figure 2 Timing Diagram, Dual Bus Output - Option 2

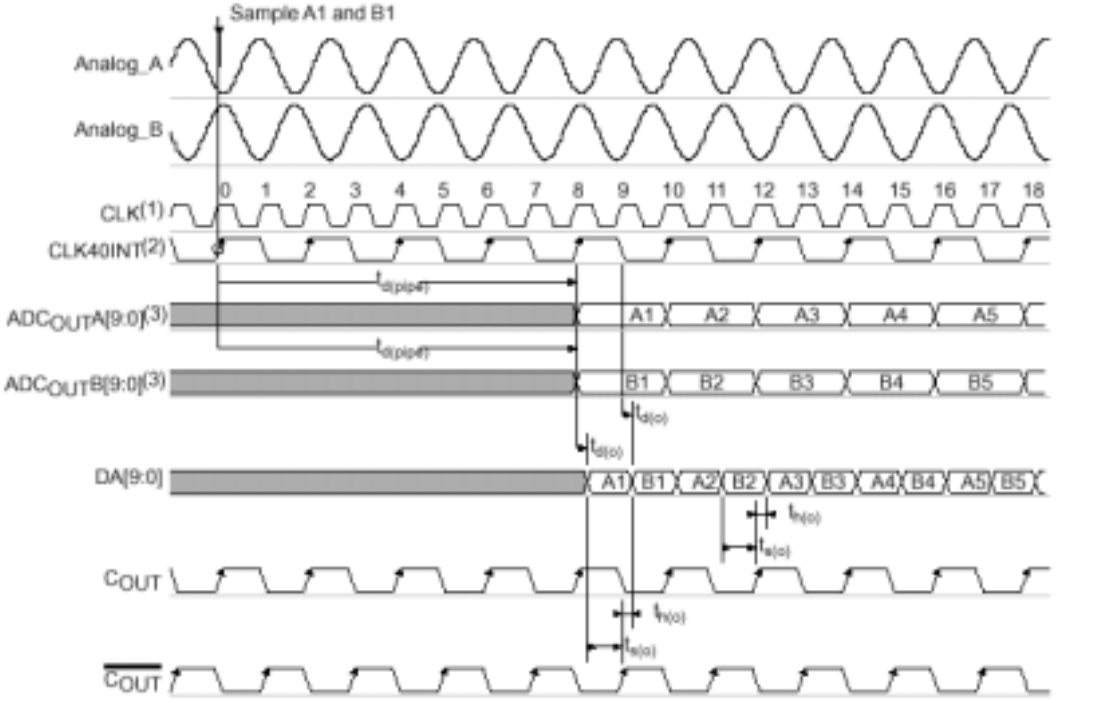
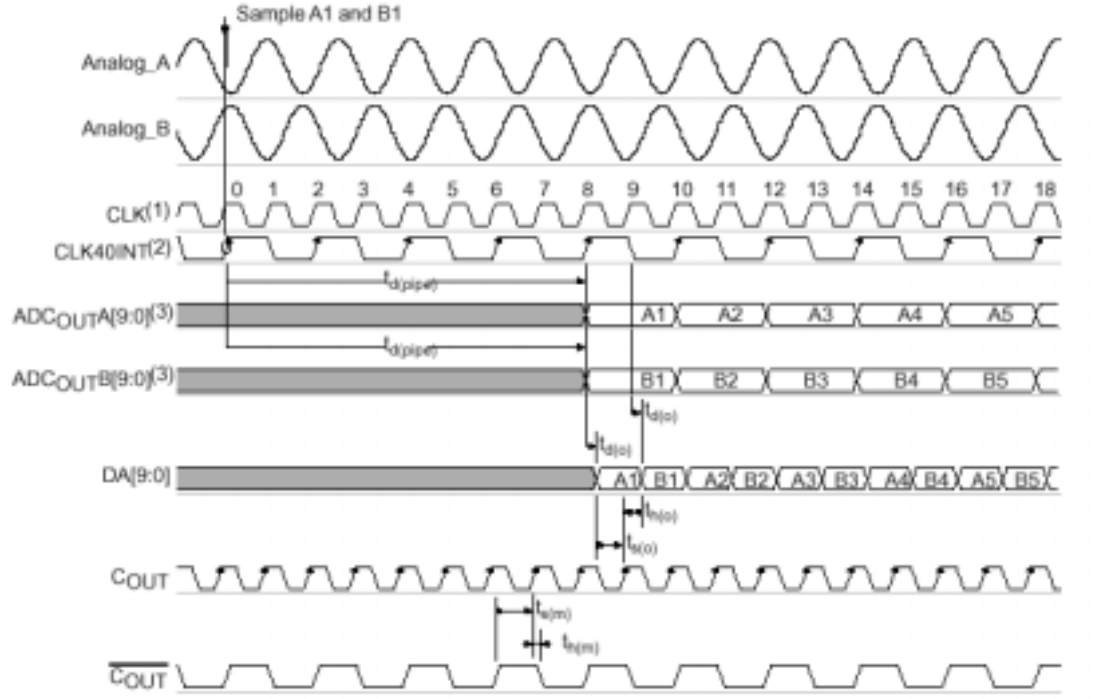


Figure 3 Timing Diagram, Single Bus Output - Option 1



NOTES: (1) In this option CLK = 80MHz. (2) CLK40INT refers to 40MHz Internal Clock, per channel. (3) Internal signal only.

Figure 4 Timing Diagram, Single Bus Output - Option 2

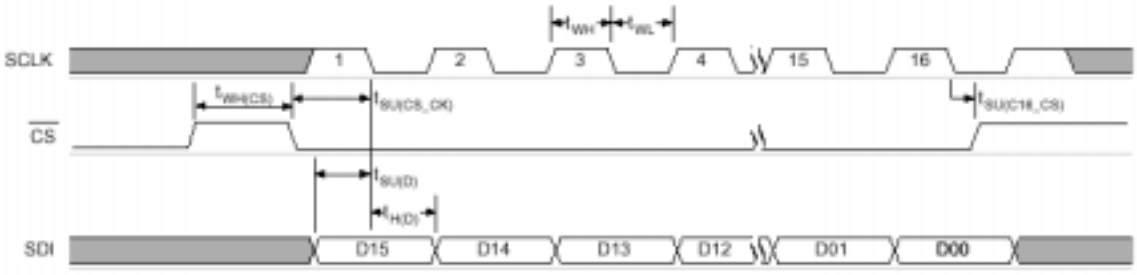


Figure 5 Serial Data Write.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	Reserved	TWOS	MODE	SELB	PGA4 B	PGA3 B	PGA2 B	PGA1 B	PGA0 B	PGA4 A	PGA3 A	PGA2 A	PGA1 A	PGA0 A

Always write 0

Table 1 Register Configuration

Default (power-up) condition for this register is all bits = 0.The user register is updated on either the first rising edge of SCLK after the 16th falling edge or CSB rising, whichever comes first. Raising CSB before 16 falling SCLK edges have been seen is an incomplete write error and no register update will occur. The PGA gain settings are resynchronised to the internal data conversion clock to avoid data glitches caused by changing gain settings while sampling the inputs.

PGA gain control data is applied to the PGAs on the second falling edge of the ADC sample clock (CLK40INT) after a successful register write. This resynchronisation ensures that no analogue glitch occurs even when SCLK is asynchronous to CLK. Note that only the PGA data is resynchronised. The TWOS, MODE, and SELB register bits take effect immediately after a successful register write.

OUTPUT DATA FORMAT

The output data format can either be in Binary Two's Complement output mode or in unsigned binary mode, which affects both A and B channels.

TWOS – Binary Two's Complement Mode:

0 – Unsigned Binary

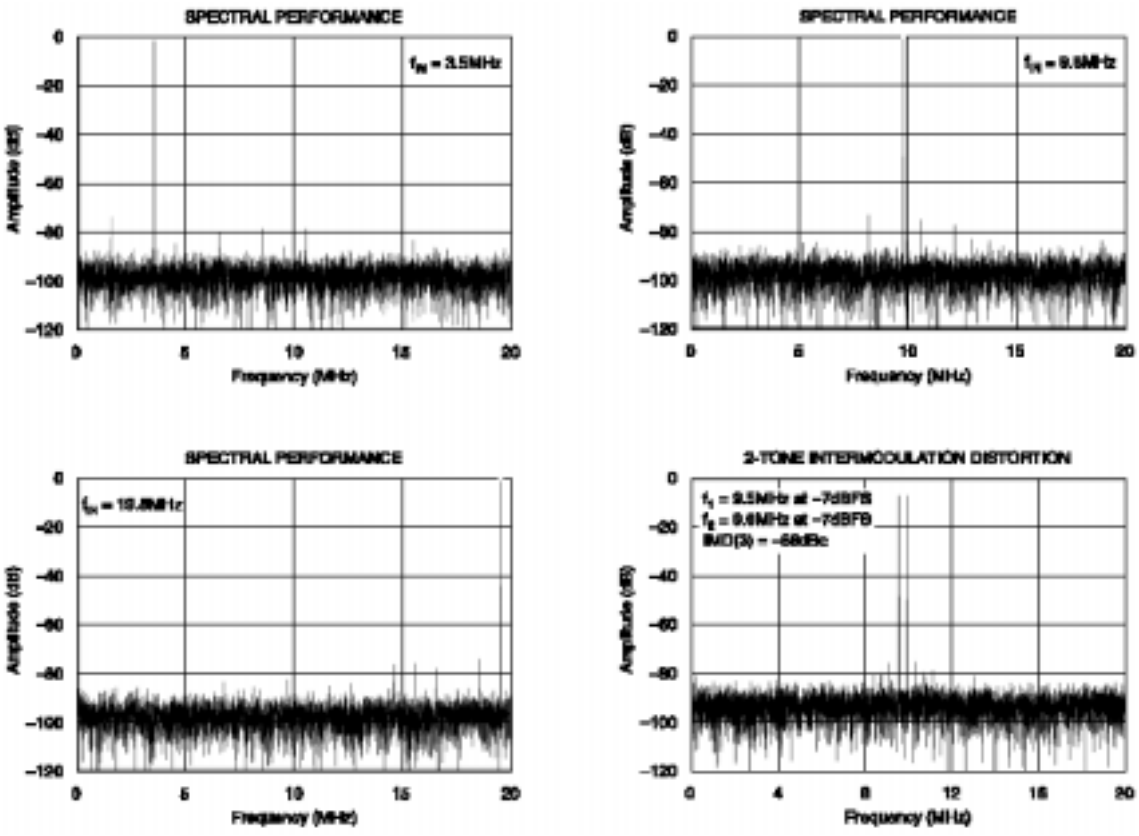
1 – Binary Two's Complement Output.

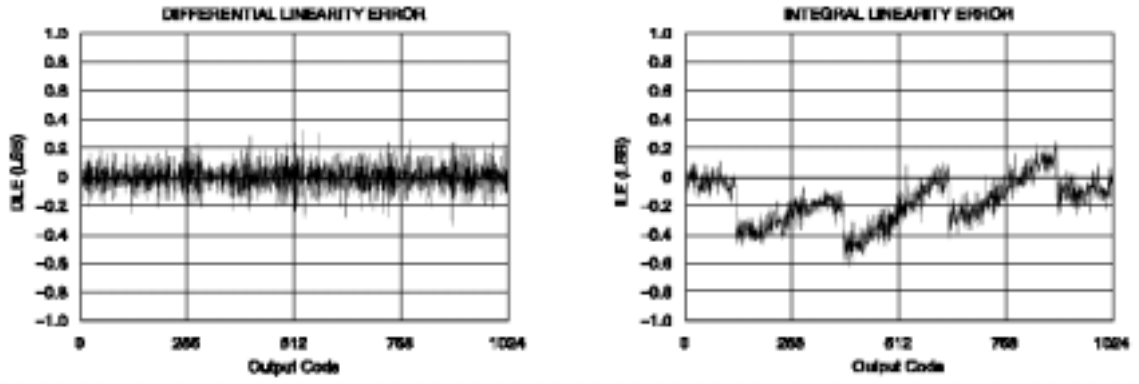
GAIN (dB)	PGx4	PGx3	PGx2	PGx1	PGX0
0	0	0	0	0	0
0.5606	0	0	0	0	1
1.1599	0	0	0	1	0
1.6643	0	0	0	1	1
2.3806	0	0	1	0	0
2.8703	0	0	1	0	1
3.5218	0	0	1	1	0
4.0824	0	0	1	1	1
4.6817	0	1	0	0	0
5.1630	0	1	0	0	1
5.8451	0	1	0	1	0
6.3903	0	1	0	1	1
6.9807	0	1	1	0	0
7.6040	0	1	1	0	1
8.0497	0	1	1	1	0
8.7712	0	1	1	1	1
9.2831	1	0	0	0	0
9.8272	1	0	0	0	1
10.4078	1	0	0	1	0
11.0301	1	0	0	1	1
11.7005	1	0	1	0	0
12.0412	1	0	1	0	1
12.7970	1	0	1	1	0
13.2208	1	0	1	1	1
14.0944	1	1	0	0	0
14.5400	1	1	0	0	1
15.0666	1	1	0	1	0
15.5630	1	1	0	1	1
15.1623	1	1	1	0	0
16.7229	1	1	1	0	1
17.4181	1	1	1	1	0
18.0618	1	1	1	1	1

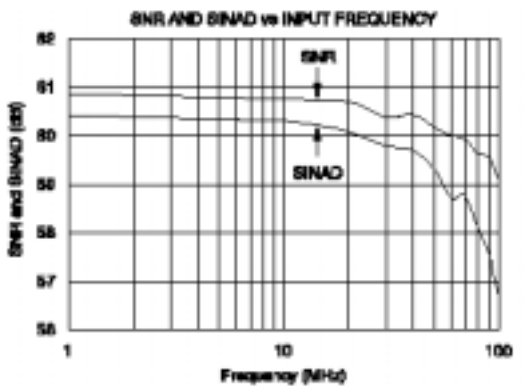
Table 2 PGA DB[0:4], 5-Bit PGA Gain Code for channel A or B

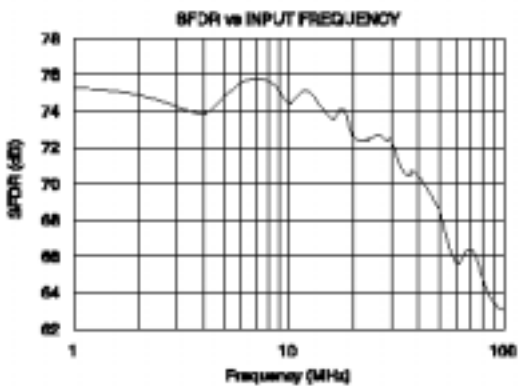
TYPICAL CHARACTERISTICS

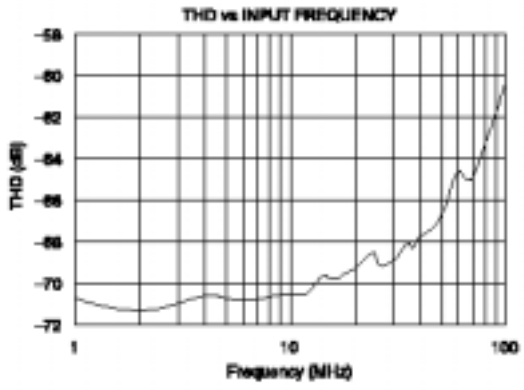
At T_A = 25°C, AVDD = DVDD = DRVDD = 3.3V, f_{IN} = -0.5dBFS, Internal Reference, f_{CLK} = 80MHz, f_S = 40MSPS, Differential Input Range = 2Vp-p, 25Ω series resistor, and 15pF differential capacitor at A/B+ and A/B- inputs, unless otherwise stated.

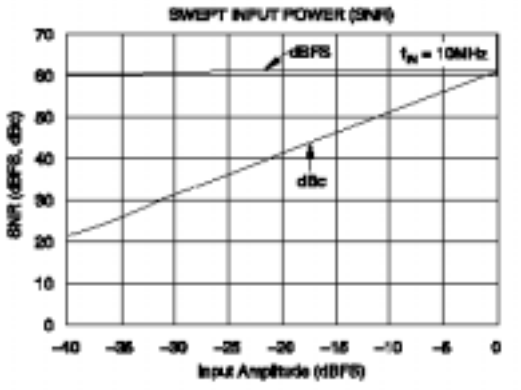





SNR AND SINAD vs INPUT FREQUENCY
SNR
SINAD
SNR and SINAD (dB)
Frequency (MHz)


SFDR vs INPUT FREQUENCY
SFDR (dB)
Frequency (MHz)


THD vs INPUT FREQUENCY
THD (dB)
Frequency (MHz)


SWEPT INPUT POWER (SNR)
dBFS
dBc
SNR (dBFS, dBc)
Input Amplitude (dBFS)

DEVICE OPERATION

INTRODUCTION

The WM2124 implements a dual high-speed 10-bit, 40MSPS converter in a cost-effective CMOS process. The differential inputs on each channel are sampled simultaneously. Signal inputs are differential and the clock signal is single-ended. The clock signal is either 80MHz or 40MHz, depending on the device configuration set by the user. Powered from 3.3V, the dual-pipeline design architecture ensures low-power operation and 10-bit resolution. The digital inputs are 3.3V TTL/CMOS compatible. Internal voltage references are included for both bottom and top voltages. Alternatively, the user may apply externally generated reference voltages. In doing so, the input range can be modified to suit the application.

The ADC is a 5-stage pipelined ADC with four stages of fully-differential switched capacitor sub-ADC/MDAC pairs and a single sub-ADC in stage five. All stages deliver two bits of the final conversion result. A digital error correction is used to compensate for modest comparator offsets in the sub-ADCs.

SAMPLE AND HOLD AMPLIFIER

Figure 6 shows the internal SHA/SHPGA architecture. The circuit is balanced and fully differential for good supply noise rejection. The sampling circuit has been kept as simple as possible to obtain good performance for high-frequency input signals.

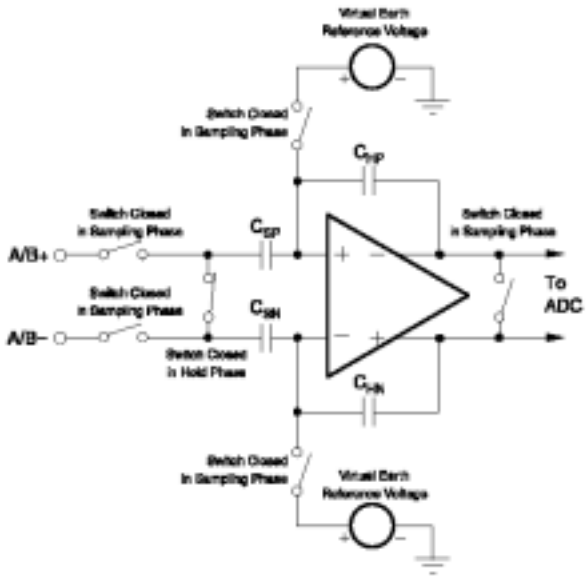


Figure 6. SHA/SHPGA Architecture

The analogue input signal is sampled on capacitors C_{SP} and C_{SN} while the internal device clock is LOW. The sampled voltage is transferred to capacitors C_{HP} and C_{HN} and held on these while the internal device clock is HIGH. The SHA can sample both single-ended and differential input signals.

The load presented to the AIN pin consists of the switched input sampling capacitor C_S (approximately 2pF) and its various stray capacitances. A simplified equivalent circuit for the switched capacitor input is shown in Figure 7. The switched capacitor circuit is modelled as a resistor R_{IN} . f_{CLK} is the clock frequency, which is 40MHz at full speed, and C_S is the sampling capacitor. The use of 25Ω series resistors and a differential 15pF capacitor at the A/B+ and A/B– inputs is recommended to reduce noise.

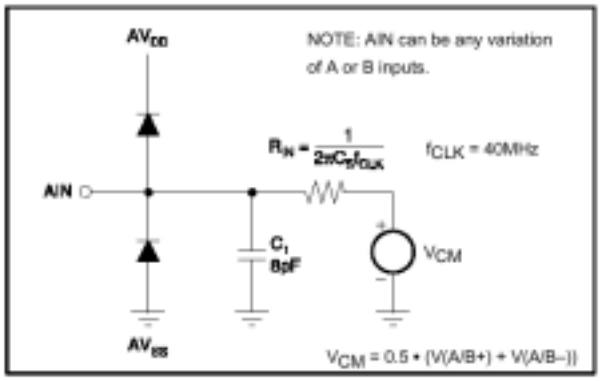


Figure 7 Equivalent Circuit for the Switched Capacitor Input

ANALOGUE INPUT, DIFFERENTIAL CONNECTION

The analogue input of the WM2124 is a differential architecture that can be configured in various ways depending on the signal source and the required level of performance. A fully differential connection will deliver the best performance from the converter. The analogue inputs must not go below AVDD or above AVDD. The inputs can be biased with any common-mode voltage provided that the minimum and maximum input voltages stay within the range AVSS to AVDD. It is recommended to bias the inputs with a common-mode voltage around AVDD/2. This can be accomplished easily with the output voltage source CML, which is equal to AVDD/2. CML is made available to the user to help simplify circuit design. This output voltage source is not designed to be a reference or to be loaded but makes an excellent DC bias source and stays well within the analogue input common-mode voltage range over temperature. Table 3 lists the digital outputs for the corresponding analogue input voltages.

DIFFERENTIAL INPUT	
V_{IN} = (A/B+) – (A/B-), REFT – REFB = 1V, PGA = 0dB	
Analogue Input Voltage	**Digital Output Code**
V_{IN} = +1V	$3FF_H$
V_{IN} = 0V	200_H
V_{IN} = -1V	000_H

Table 3 Output Format for Differential Configuration

DC-COUPLED DIFFERENTIAL ANALOGUE INPUT CIRCUIT

Driving the analogue input differentially can be achieved in various ways. Figure 8 gives an example where a single-ended signal is converted into a differential signal by using a fully differential amplifier. The input voltage applied to VOCM of the amplifier shifts the output signal into the desired common–mode level. VOCM can be connected to CML of the WM2124, the common-mode level is shifted to AVDD /2.

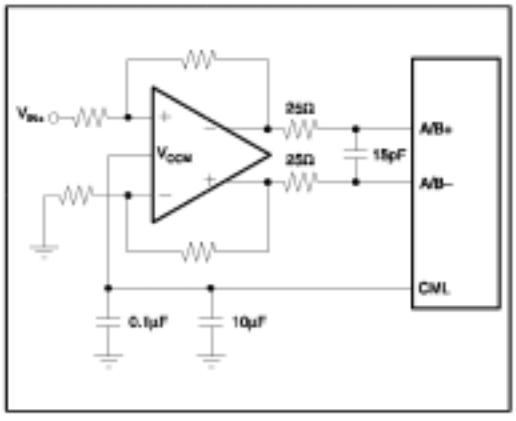


Figure 8 Single Ended to Differential Conversion

AC-COUPLED DIFFERENTIAL ANALOGUE INPUT CIRCUIT

Driving the analogue input differentially can be achieved by using a transformer coupling, as illustrated in Figure 9. The centre tap of the transformer is connected to the voltage source CML, which sets the common–mode voltage to AV DD /2. No buffer is required at the output of CML since the circuit is balanced and no current is drawn from CML.

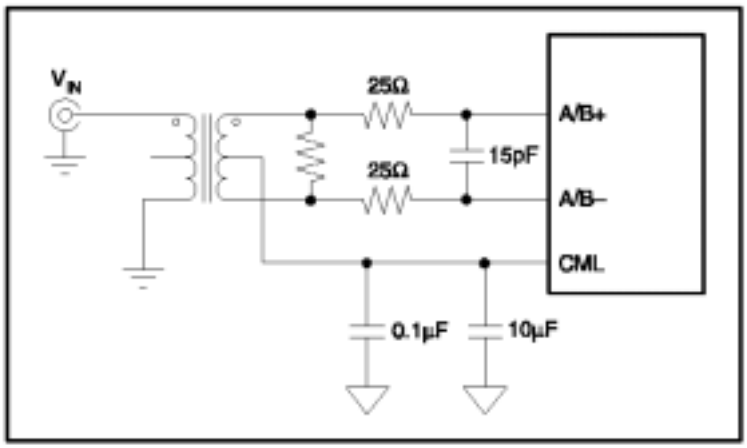


Figure 9 AC-Coupled Differential Input with Transformer

ANALOGUE INPUT, SINGLE ENDED CONFIGURATION

For a single-ended configuration, the input signal is applied to only one of the two inputs. The signal applied to the analogue input must not go below AVSS or above AVDD. The inputs can be biased with any common-mode voltage provided that the minimum and maximum input voltage stays within the range AV SS to AVDD. It is recommended to bias the inputs with a common-mode voltage around AVDD/2. This can be accomplished easily with the output voltage source CML, which is equal to AVDD/2. An example for this is shown in Figure 10.

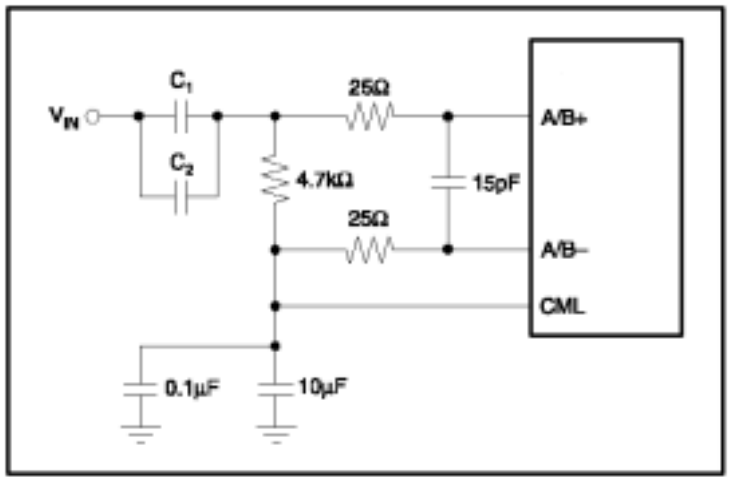


Figure 10 AC-Coupled, Single-Ended Configuration

The signal amplitude to achieve full-scale is 2Vp-p. The signal, which is applied at A/B+ is centred at the bias voltage. The input A/B– is also centred at the bias voltage. The CML output is connected via a 4.7kΩ resistor to bias the input signal. There is a direct DC–coupling from CML to A/B– while this input is AC–decoupled through the 10uF and 0.1uF capacitors. The decoupling minimizes the coupling of A/B+ into the A/B– path. Table 4 lists the digital outputs for the corresponding analogue input voltages.

Single Ended Input, REFT-REFB = 1V PGA = 0dB	
Analogue Input Voltage	**Digital Output Code**
$V(A/B+) = V_{CML} + 1V$	$3FF_H$
$V(A/B+) = V_{CML}$	200_H
$V(A/B+) = V_{CML} - 1V$	000_H

Table 4 Output Format for Single Ended Configuration

REFERENCE TERMINALS

The WM2124's input range is determined by the voltages on its REFB and REFT pins. The WM2124 has an internal voltage reference generator that sets the ADC reference voltages REFB = 1V and REFT = 2V. The internal ADC references must be decoupled to the PCB AVSS plane. The recommended decoupling scheme is shown in Figure 11. The common-mode reference voltages should be 1.5V for best ADC performance.

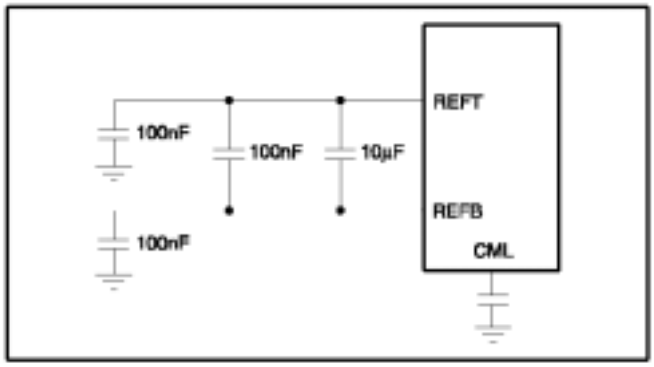


Figure 11 Recommended External Decoupling for the Internal ADC Reference

External ADC references can also be chosen. The WM2124 internal references must be disabled by tying PWDN_REF HIGH before applying the external reference sources to the REFT and REFB pins. The common-mode reference voltages should be 1.5V for best ADC performance.

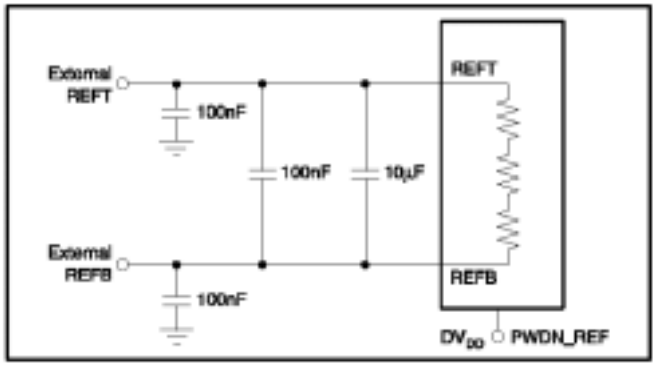


Figure 12 External ADC Reference Configuration

DIGITAL INPUTS

Digital inputs are CLK, SCLK, SDI, CSB, STDBY, PWDN_REF, and OEB. These inputs don't have a pull-down resistor to ground, therefore, they should not be left floating.

The CLK signal at high frequencies should be considered as an 'analogue' input. CLK should be referenced to AVDD and AVSS to reduce noise coupling from the digital logic. Overshoot/undershoot should be minimized by proper termination of the signal close to the WM2124. An important cause of performance degradation for a high-speed ADC is clock jitter. Clock jitter

causes uncertainty in the sampling instant of the ADC, in addition to the inherent uncertainty on the sampling instant caused by the part itself, as specified by its aperture jitter. There is a theoretical relationship between the frequency (f) and resolution (2 N) of a signal that needs to be sampled on one hand, and on the other hand the maximum amount of aperture error dt_{max} that is tolerable. It is given by the following relation:

$$dt_{\max} = \frac{1}{\Pi f 2^{(N+1)}}$$

As an example, for a 10-bit converter with a 20MHz input, the jitter needs to be kept less than 7.8ps in order not to have changes in the LSB of the ADC output due to the total aperture error.

DIGITAL OUTPUTS

The output of WM2124 is an unsigned binary or Binary Two's Complement code. Capacitive loading on the output should be kept as low as possible (a maximum loading of 10pF is recommended) to ensure best performance. Higher output loading causes higher dynamic output currents and can, therefore, increase noise coupling into the part's analogue front end. To drive higher loads, the use of an output buffer is recommended.

When clocking output data from WM2124, it is important to observe its timing relation to C_{OUT}. Please refer to the timing section for detailed information on the pipeline latency in the different modes. For safest system timing, C_{OUT} and C_{OUTB} should be used to latch the output data (see Figures 1 to 4). In Figure 4, C_{OUT} can be used by the receiving device to identify whether the data presently on the bus is from channel A or B.

LAYOUT, DECOUPLING AND GROUNDING RULES

Proper grounding and layout of the PCB on which the WM2124 is populated is essential to achieve the stated performance. It is advised to use separate analogue and digital ground planes that are spliced underneath the IC. The WM2124 has digital and analogue pins on opposite sides of the package to make this easier. Since there is no connection internally between analogue and digital grounds, they have to be joined on the PCB. It is advised to do this at one point in close proximity to the WM2124.

As for power supplies, separate analogue and digital supply pins are provided on the part (AVDD /DVDD). The supply to the digital output drivers is kept separate as well (DRVDD). Lowering the voltage on this supply to 3.0V instead of the nominal 3.3V improves performance because of the lower switching noise caused by the output buffers. Due to the high sampling rate and switched-capacitor architecture, the WM2124 generates transients on the supply and reference lines. Proper decoupling of these lines is, therefore, essential.

SERIAL INTERFACE

A falling edge on CSB enables the serial interface, allowing the 16-bit control register date to be shifted (MSB first) on subsequent falling edges of SCLK. The data is loaded into the control register on the first rising edge of SCLK after its 16th falling edge or CSB rising, whichever occurs first. CSB rising before 16 falling SCLK edges have been counted is an error and the control register will not be updated. The maximum update rate is:

$$f_{update\max} = \frac{f_{SCLK}}{16} = \frac{20MHz}{16} = 1.25MHz$$

NOTES

1. Integral Nonlinearity (INL) — Integral nonlinearity refers to the deviation of each individual code from a line drawn from zero to full-scale. The point used as zero occurs _ LSB before the first code transition. The full-scale point is defined as a level _ LSB beyond the last code transition. The deviation is measured from the centre of each particular code to the true straight line between these two endpoints.

2. Differential Nonlinearity (DNL) — An ideal ADC exhibits code transitions that are exactly 1LSB apart. DNL is the deviation from this ideal value. Therefore, this measure indicates how uniform the transfer function step sizes are. The ideal step size is defined here as the step size for the device under test (i.e., (last transition level – first transition level)/(2^n – 2)). Using this definition for DNL

separates the effects of gain and offset error. A minimum DNL better than –1LSB ensures no missing codes.

3. Zero and Full-Scale Error — Zero error is defined as the difference in analogue input voltage—between the ideal voltage and the actual voltage—that will switch the ADC output from code 0 to code 1. The ideal voltage level is determined by adding the voltage corresponding to _ LSB to the bottom reference level. The voltage corresponding to 1LSB is found from the difference of top and bottom references divided by the number of ADC output levels (1024).

Full-scale error is defined as the difference in analogue input voltage—between the ideal voltage and the actual voltage—that will switch the ADC output from code 1022 to code 1023. The ideal voltage level is determined by subtracting the voltage corresponding to 1.5LSB from the top reference level. The voltage corresponding to 1LSB is found from the difference of top and bottom references divided by the number of ADC output levels (1024).

4. Analogue Input Bandwidth — The analogue input bandwidth is defined as the max. frequency of a 1dBFS input sine that can be applied to the device for which a extra 3dB attenuation is observed in the reconstructed output signal.

5. Output Timing — Output timing $t_{d(o)}$ is measured from the 1.5V level of the CLK input falling edge to the 10%/90% level of the digital output. The digital output load is not higher than 10pF. Output hold time t h(o) is measured from the 1.5V level of the C_{OUT} input rising edge to the 10%/90% level of the digital output. The digital output is load is not less than 2pF. Aperture delay $t_{d(A)}$ is measured from the 1.5V level of the CLK input to the actual sampling instant.

The OEB signal is asynchronous. OEB timing t_{dis} is measured from the $V_{IH(MIN)}$ level of OEB to the high-impedance state of the output data. The digital output load is not higher than 10pF. OEB timing t_{en} is measured from the $V_{IL(MAX)}$ level of OEB to the instant when the output data reaches $V_{OH(min)}$ or $V_{OL(max)}$ output levels. The digital output load is not higher than 10pF.

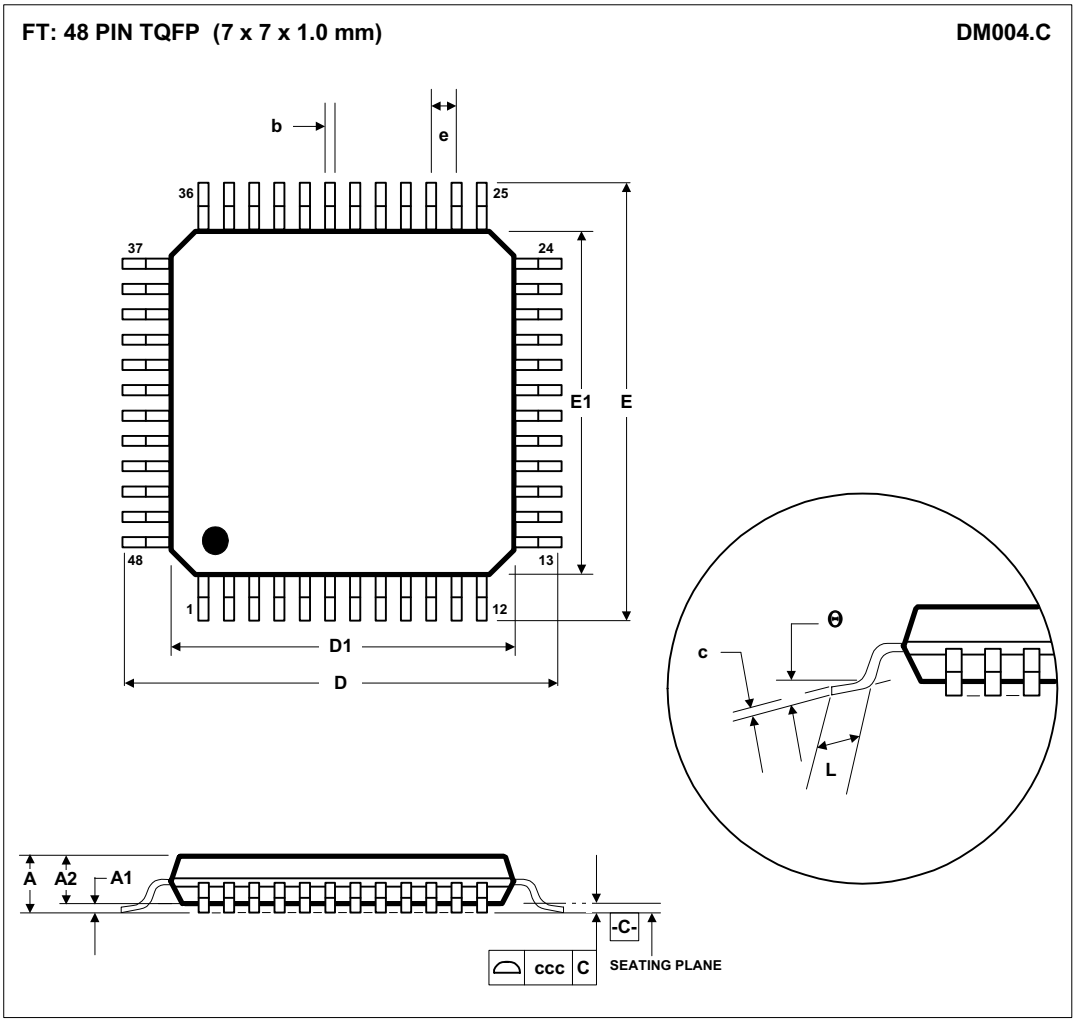
6. Pipeline Delay (latency) — The number of clock cycles between conversion initiation on an input sample and the corresponding output data being made available from the ADC pipeline. Once the data pipelines full, new valid output data is provided on every clock cycle. The first valid data is available on the output pins after the latency time plus the output delay time $t_{d(o)}$ through the digital output buffers. Note that a minimum $t_{d(o)}$ is not guaranteed because data can transition before or after a CLK edge. It is possible to use CLK for latching data, but at the risk of the prop delay varying over temperature, causing data to transition one CLK cycle earlier or later. The recommended method is to use the latch signals C_{OUT} and C_{OUTB} which are designed to provide reliable setup and hold times with respect to the data out.

7. Wake-Up Time — Wake-up time is from the power-down state to accurate ADC samples being taken, and is specified for external reference sources applied to the device and an 80MHz clock applied at the time of release of STDBY. Cells that need to power up are the bandgap, bias generator, SHAs, and ADCs.

8. Power-Up Time — Power-up time is from the power-down state to accurate ADC samples being taken with an 80MHz clock applied at the time of release of STDBY. Cells that need to power up are the bandgap, internal reference circuit, bias generator, SHAs, and ADCs

PACKAGE DIMENSIONS

FT: 48 PIN TQFP (7 x 7 x 1.0 mm) **DM004.C**



Symbols	Dimensions (mm)		
	MIN	NOM	MAX
A	-----	-----	1.20
A_1	0.05	-----	0.15
A_2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09	-----	0.20
D	9.00 BSC		
D_1	7.00 BSC		
E	9.00 BSC		
E_1	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
Θ	0^o	3.5^o	7^o
Tolerances of Form and Position			
ccc	0.08		
REF:	JEDEC.95, MS-026		

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.25MM.
D. MEETS JEDEC.95 MS-026, VARIATION = ABC. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

IMPORTANT NOTICE

Wolfson Microelectronics plc (WM) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current. All products are sold subject to the WM terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

WM warrants performance of its products to the specifications applicable at the time of sale in accordance with WM's standard warranty. Testing and other quality control techniques are utilised to the extent WM deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

In order to minimise risks associated with customer applications, adequate design and operating safeguards must be used by the customer to minimise inherent or procedural hazards.

WM assumes no liability for applications assistance or customer product design. WM does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of WM covering or relating to any combination, machine, or process in which such products or services might be or are used. WM's publication of information regarding any third party's products or services does not constitute WM's approval, license, warranty or endorsement thereof.

Reproduction of information from the WM web site or datasheets is permissable only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations and notices. Representation or reproduction of this information with alteration voids all warranties provided for an associated WM product or service, is an unfair and deceptive business practice, and WM is not responsible nor liable for any such use.

Resale of WM's products or services with statements different from or beyond the parameters stated by WM for that product or service voids all express and any implied warranties for the associated WM product or service, is an unfair and deceptive business practice, and WM is not responsible nor liable for any such use.

ADDRESS:

Wolfson Microelectronics plc

Westfield House

26 Westfield Road

Edinburgh

EH11 2QW

United Kingdom

Tel :: +44 (0)131 272 7000

Fax :: +44 (0)131 272 7001

Email :: sales@wolfsonmicro.com