TM5400/TM5600 Data Book

November 1, 2000

Confidential Information—NDA Required

TRANSMETA Corporation

Crusoe™ Processor Model TM5400/TM5600

Data Book
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Confidential Information—NDA Required

Revision History:

1.0 Initial release. (2/18/00)

1.1 Added TM5600. Changed frequency/voltage SKUs. Corrected sequential pin listing and added alphabetic pin listing. Removed S_CLK[7:4]. Updated electrical specs. (5/25/00)

1.2 Added SDR/DDR interface memory timing tables, thermal diode specs, new package drawings, updated package marking specifications. (10/23/00)

1.3 Removed 633 MHz SKU (11/1/00)

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Introduction

The Transmeta Crusoe™ Processor Model TM5400/TM5600 is a high performance, low power microprocessor based on a VLIW core architecture. When combined with Transmeta's x86 Code Morphing™ software, the TM5400/TM5600 provides x86-compatible code execution. The TM5400/TM5600 delivers a highly integrated, cost-effective solution by incorporating an L2 cache, support for single data rate (SDR) and double data rate (DDR) SDRAM, and a PCI controller. Additionally, the TM5400/TM5600 provides power management controls, SMM and thermal monitoring capability, and operates from a low voltage supply (1.2-1.6 V), making it ideal for mobile applications.

Crusoe™ Processor Model TM5400/TM5600 Feature Set

- VLIW processor and x86 Code Morphing software provides x86-compatible mobile platform solution
- 500, 533, 600, and 667 MHz operating frequencies
- Integrated 64 kByte L1 instruction and data caches, and 256 kByte (TM5400) or 512 kByte (TM5600) L2 write-back cache
- Integrated northbridge core logic features facilitate compact system designs
  - DDR SDRAM memory controller with 100-133 MHz, 2.5V interface
  - SDR SDRAM memory controller with 66-133 MHz, 3.3V interface
  - PCI bus controller (PCI 2.1 compliant) with 33 MHz, 3.3V interface
- LongRun™ advanced power management with ultra-low power operation extends battery life
  - 0.7-2.5 W @ 500-667 MHz, 1.2-1.6V running typical multimedia applications
  - 100 mW in deep sleep
- Power management controls for ACPI-compliant modes
- Full System Management Mode (SMM) support
- Compact 474-pin ceramic BGA package

The processor core operates from a 1.2-1.6 V supply, resulting in extremely low power consumption even at high operating frequencies. The processor typically consumes only 0.7-2.5 Watts under normal operating conditions. When operating in deep sleep, power consumption drops below 100 mW.

Architectural Overview

The Transmeta Crusoe Processor model TM5400/TM5600 is an ultra-low power, high-speed microprocessor based on an advanced VLIW core architecture. When used in conjunction with Transmeta's x86 Code Morphing software, the TM5400/TM5600 provides x86-compatible software execution using dynamic binary code translation, without requiring code recompilation. In addition to the VLIW core, the processor incorporates separate 64 kByte L1 instruction and data caches, a large L2 write-back cache (256 kByte on TM5400, 512 kByte on TM5600), a 64-bit DDR SDRAM memory controller, a 64-bit SDR SDRAM memory controller, and a 32-bit PCI controller. These additional functional units, which are typically part of the core system logic that surrounds the microprocessor, allow the TM5400/TM5600 to provide a highly integrated, cost-effective platform solution for the x86 mobile market.

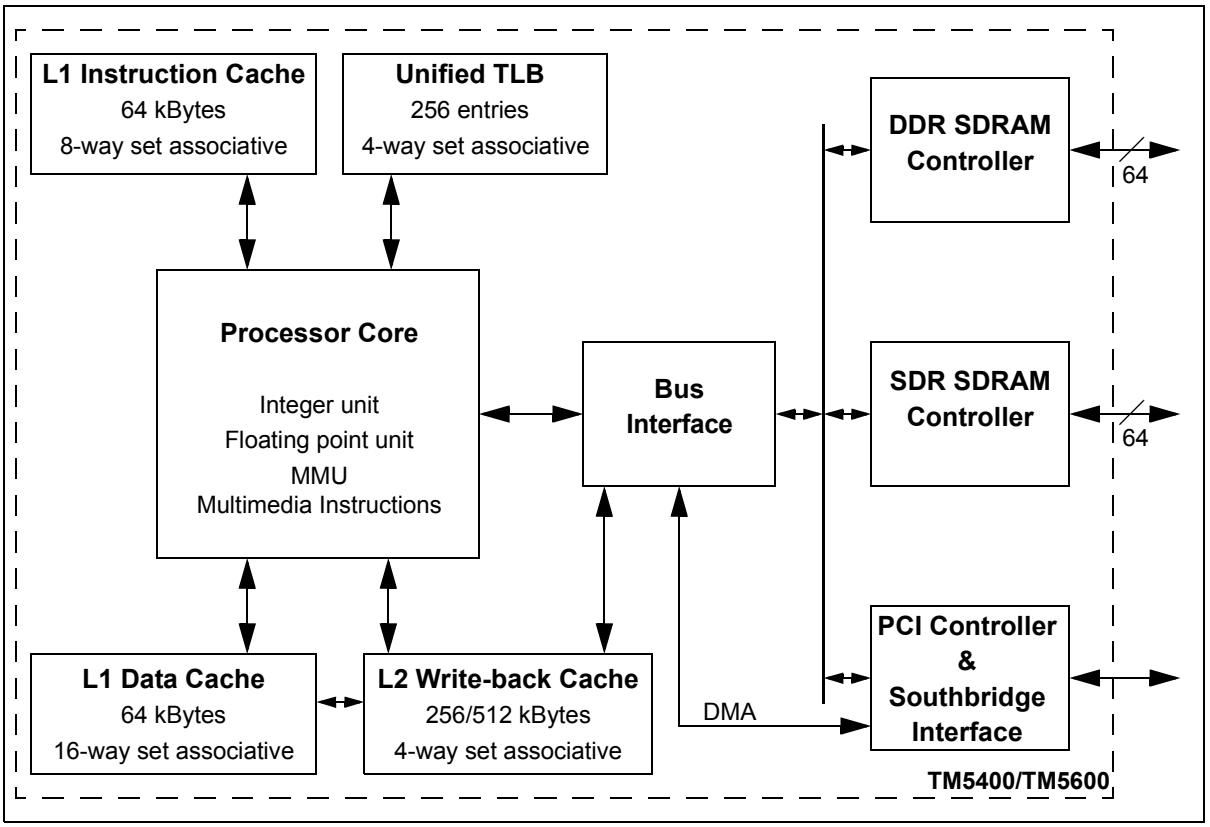
The TM5400/TM5600 processor core is relatively simple by current standards. It is based on a Very Long Instruction Word (VLIW) instruction set of 64 or 128 bits. By utilizing a VLIW architecture, the control logic of the TM5400/TM5600 is kept simple since software controls the scheduling of TM5400/TM5600 instructions. This leaves the hardware with an in-order 7-stage integer pipeline and a 10-stage floating point pipeline. By streamlining the hardware, performance can be improved over traditional x86 architectures by increasing the operating frequency.

Other than having the hardware execute arithmetic, shift, and floating point instructions similarly to an x86 processor, the TM5400/TM5600 does not have the same features as a traditional x86 design. To ease the translation process from x86 to TM5400/TM5600 code, the hardware generates the same condition codes as an x86 and it operates on the same 80-bit floating point numbers. Also, the TM5400/TM5600 Translation Look-aside Buffer (TLB) has the same protection bits and address mapping as an x86. It is up to the software to emulate all other features of the x86 architecture. The software that is tasked with converting the x86 programs into TM5400/TM5600 programs is called Code Morphing software. The combination of Code Morphing software and the TM5400/TM5600 hardware device together act as an x86-compatible microprocessor.

Block Diagram

The TM5400/TM5600 block diagram is shown in the following figure:

FIGURE 1 TM5400/TM5600 Block Diagram



Reference Documents

The following documents should be used in conjunction with this specification:

TM5400/TM5600 Package Specifications and Manufacturing Guide	Transmeta TMDFP-xx
TM5400/TM5600 System Design Guide	Transmeta TMDFS-xx
TM5400/TM5600 Thermal Design Guide	Transmeta TMDFT-xx
TM5400/TM5600 Development and Manufacturing Guide	Transmeta TMDFD-xx
TM5400/TM5600 BSDL Test Files	
TM5400/TM5600 IBIS Models	
TM5400/TM5600/Code Morphing Software Version 4.1 BIOS Programmer's Guide	Transmeta TMDFB-xx
TM5400/TM5600/Code Morphing Software Version 4.1.x Release Notes	
TM5400/TM5600/Code Morphing Software Version 4.1.x Errata	
PCI Local Bus Specification	PCI SIG Revision 2.1

Chapter 1

Functional Interface Description

1.1 DDR SDRAM Interface

The DDR SDRAM interface is the highest performance memory interface available on the TM5400/TM5600. The DDR SDRAM controller supports only double data rate (DDR) SDRAM and transfers data at a rate that is twice the clock frequency of the interface. The DDR SDRAM controller supports the equivalent of two DIMMs (up to four rows) of double data rate (DDR) SDRAM using a 64-bit wide interface.

The DDR SDRAM can be populated with 64-Mbit, 128-Mbit, or 256-Mbit devices. For the highest performance, it is recommended that the DDR SDRAM devices be soldered to the planar rather than incorporated on DIMMs. Also, to reduce signal loading, only x8, x16 or x32 devices should be used. Table 1 shows possible DDR SDRAM configurations for a TM5400/TM5600-based system.

TABLE 1 DDR SDRAM Memory Configurations

DDR Device Size (Mbits)	DDR Device Configuration	Number of Devices per Row	Memory Size per Row (MBytes)	Maximum Rows	Maximum Memory Size (MBytes)
64	2M x 32	2	16	4	64
	4M x 16	4	32	4	128
	8M x 8	8	64	4	256
128	4M x 32	2	32	4	128
	8M x 16	4	64	4	256
	16M x 8	8	128	4	512
256	8M x 32	2	64	4	256
	16M x 16	4	128	4	512
	32M x 8	8	256	4	1024

The frequency setting for the DDR SDRAM interface is initialized during the boot sequence from data stored in the configuration ROM. Although the TM5400/TM5600 can be configured for a DDR interface frequency in the range of 1/2 to 1/15 of the core frequency, the supported interface frequency is between 100 and 133 MHz as shown in Table 2.

TABLE 2 Core and DDR SDRAM Interface Frequency Configurations

Core Frequency	DDR Interface Frequency Divider	DDR Interface Frequency	DDR Data Rate
667 MHz	5	133 MHz	267 MHz
600 MHz	5	120 MHz	240 MHz
533 MHz	4	133 MHz	267 MHz
500 MHz	4	125 MHz	250 MHz

With LongRun enabled, the core frequency is lowered during times when peak performance is not required. When the core frequency changes, the DDR SDRAM interface frequency is recalculated to match the new core frequency setting. For example, a 600 MHz device with a 120 MHz memory interface may have a LongRun setting of 533 MHz with a 133 MHz memory interface. Therefore, TM5400/TM5600-based systems that use LongRun must support the entire DDR SDRAM interface frequency range of 100 to 133 MHz.

1.2 SDR SDRAM Interface

The SDR SDRAM controller supports up to two DIMMS (up to four rows) of single data rate (SDR) SDRAM that can be configured as 64-bit or 72-bit DIMMs. These DIMMs can be populated with 64-Mbit, 128-Mbit or 256-Mbit devices. All DIMMs must use the same frequency SDRAMs but there are no restrictions on mixing different DIMM configurations into each DIMM slot. Table 3 shows possible SDR SDRAM configurations for a TM5400/TM5600-based system. The maximum memory size in Table 3 assumes two double-sided DIMMs of identical configuration and a maximum of 16 total devices per DIMM.

TABLE 3 SDR SDRAM Memory Configurations

SDR Device Size (Mbits)	SDR Device Configuration	Number of Devices per Row	Memory Size per Row (MBytes)	Maximum Rows	Maximum Memory Size (MBytes)
64	4M x 16	4	32	4	128
	8M x 8	8	64	4	256
	16M x 4	16	128	2	256
128	4M x 32	2	32	4	128
	8M x 16	4	64	4	256
	16M x 8	8	128	4	512
	32M x 4	16	256	2	512
256	8M x 32	2	64	4	256
	16M x 16	4	128	4	512
	32M x 8	8	256	4	1024
	64M x 4	16	512	2	1024

The frequency setting for the SDR SDRAM interface is initialized during the boot sequence from data stored in the configuration ROM. Although the TM5400/TM5600 can be configured for an SDR interface frequency in the range of 1/2 to 1/15 of the core frequency, the supported interface frequency is between 66 and 133 MHz as shown in Table 4. It is also recommended that a maximum of 8 devices per DIMM be used in order to operate at the listed frequencies with the proper signal integrity.

TABLE 4 Core and SDR SDRAM Bus Frequency Configurations

Core Frequency	SDR Interface Frequency Divider	SDR Interface Frequency	SDR Data Rate
667 MHz	5	133 MHz	133 MHz
600 MHz	5	120 MHz	120 MHz
533 MHz	4	133 MHz	133 MHz
500 MHz	4	125 MHz	125 MHz

With LongRun enabled, the core frequency is lowered during times when peak performance is not required. When the core frequency changes, the SDR SDRAM interface frequency is recalculated to match the new core frequency setting. For example, a 600 MHz device with a 120 MHz memory interface may have a LongRun setting of 533 MHz with a 133 MHz memory interface. Therefore, TM5400/TM5600-based systems that use LongRun must support the entire SDR SDRAM interface frequency range up to 133 MHz.

1.3 PCI Interface

The TM5400/TM5600 PCI bus is revision 2.1 compliant. The PCI bus is 32 bits wide, operates at 33 MHz and is compatible with 3.3V levels (but is not 5V tolerant). The PCI controller on the TM5400/TM5600 provides a PCI host bridge, the central resource and a DMA controller.

The TM5400/TM5600 PCI bus can sustain 132 Mbytes/sec bursts for reads and writes on 4 kByte blocks. The PCI controller snoops ahead on PCI-to-DRAM reads and writes. The 16 DWORD CPU-to-PCI write buffer converts sequential memory mapped I/O writes to PCI bursts. The DMA controller handles PCI-to-DRAM reads and writes. The 16 DWORD PCI-to-DRAM write buffer converts one 16 DWORD burst to eight separate address/data pairs. The 16 DWORD DRAM-to-PCI read ahead buffer permits continuation of read ahead after hitting in the buffer. The PCI controller tri-states the PCI bus when hot docking.

1.3.1 PCI Bus Commands

The TM5400/TM5600 PCI controller, in conjunction with the Code Morphing software, supports the PCI bus commands listed in Table 5. If the CPU generates a shutdown, halt or stop grant condition, a PCI special cycle is generated. The shutdown cycle is propagated with 0000h in the message field, the halt cycle is propagated with 0001h in the message field, and the stop grant cycle is propagated with 0002h in the message field and 0012h in the message dependent data field.

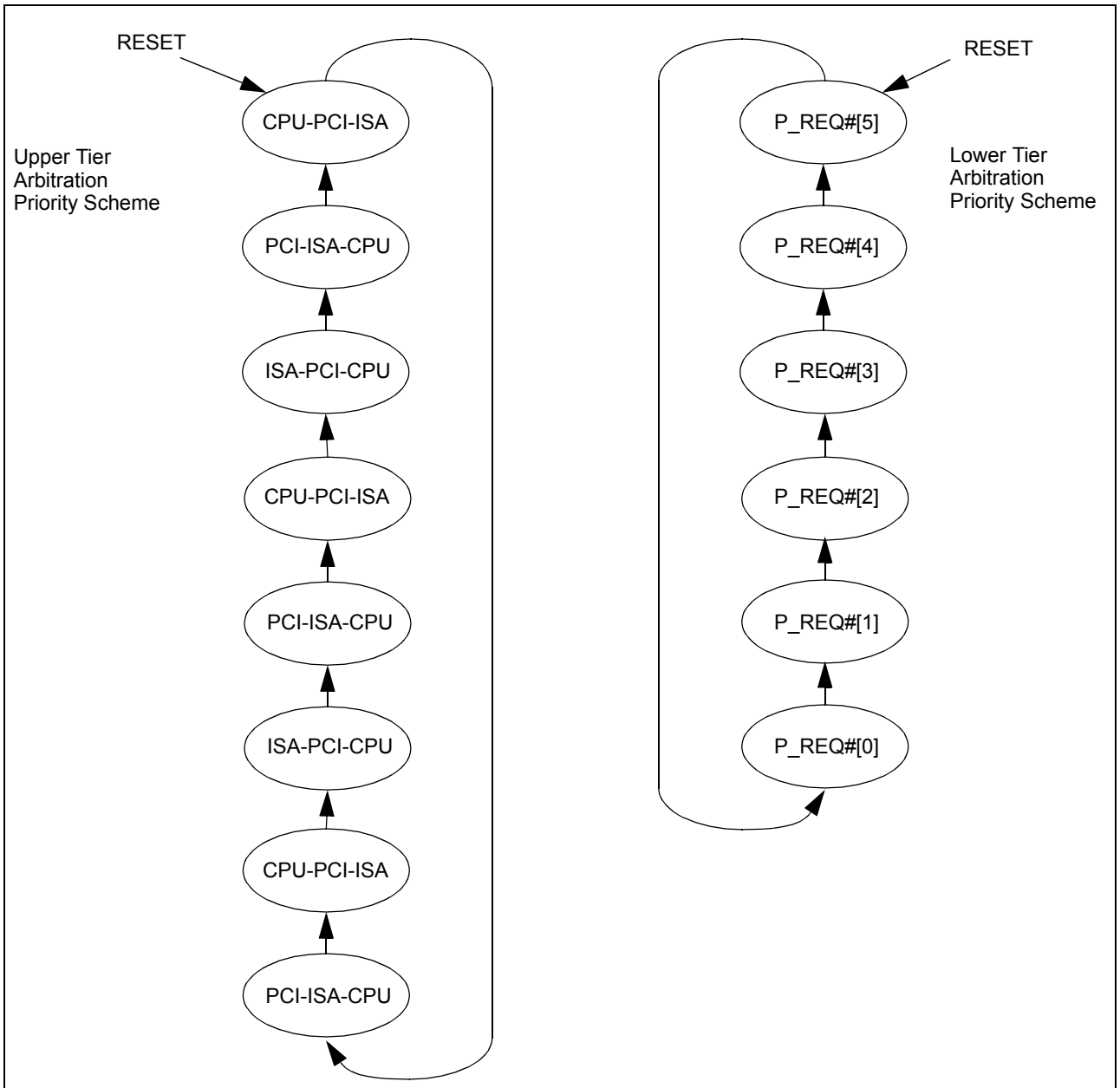
TABLE 5 PCI Bus Commands Supported

Command Encoding (P_C/BE#)	Command Type	Initiator Support	Target Support
0000	Interrupt Acknowledge	Yes	No
0001	Special Cycle	Yes	No
0010	I/O Read	Yes	No
0011	I/O Write	Yes	No
0100	--	--	--
0101	--	--	--
0110	Memory Read	Yes	Yes
0111	Memory Write	Yes	Yes
1000	--	--	--
1001	--	--	--
1010	Configuration Read	Yes	No
1011	Configuration Write	Yes	No
1100	Memory Read Multiple	No	As a memory read
1101	Dual Address Cycle	No	No
1110	Memory Read Line	No	As a memory read
1111	Memory Write and Invalidate	No	As a memory write

1.3.2 Bus Arbitration

The PCI controller central resource includes an integrated arbiter which supports up to seven PCI masters including a PCI-to-ISA bridge. P_REQ#[5:0] and P_GNT#[5:0] are the arbitration handshake signals used by PCI masters other than the PCI-to-ISA bridge. The PCI-to-ISA bridge uses the P_HOLD# and P_HLDA# signals. The arbiter, in conjunction with the Code Morphing software, implements a two-tier rotating priority-based scheme. The upper tier arbitrates among the three bus master categories of CPU, PCI devices, and PCI-to-ISA bridge. The lower tier arbitrates among the requesting PCI devices. The arbitration priority scheme is shown in Figure 2. When the PCI bus becomes idle, the arbiter “parks” the PCI bus on the CPU. If the bus is parked and the CPU and another bus master(s) request the bus simultaneously, the CPU is granted the bus regardless of the state of the upper tier priority queue.

FIGURE 2 PCI Arbitration Priority Scheme



Notes:
1. In the upper tier priority queue, upon each bus grant, the priority sequences move up one level and the top priority sequence moves to the lowest level.
2. In the upper tier priority queue, for each priority sequence, the left-most device has highest priority.
3. In the lower tier priority scheme, the last agent granted is always dropped to the bottom of the queue for the next arbitration cycle.

1.4 Southbridge Sidebands

The TM5400/TM5600 provides access to seven southbridge sideband signals. These signals are driven/monitored by a southbridge device on the base platform and are used to guarantee PC-compatible functionality for resets, interrupts, floating point errors, and processor clock control.

1.5 Serial Interfaces

The TM5400/TM5600 processor incorporates three separate serial interfaces:

- Debug interface
- Configuration ROM interface
- Code Morphing software boot ROM interface

The debug interface is a two-pin interface that may be used for debug purposes and to read configuration data from the SDR SDRAM during the boot process. The configuration data may be used to initialize the SDRAM.

The configuration ROM interface is a two-pin interface used to read data from a serial ROM device. The configuration ROM contains hardware data that is used to initialize the TM5400/TM5600 on power-up. The contents of the configuration ROM determines the settings for the CPU and the SDRAM clocks, and the memory and PCI interface timing parameters. Once the PCI and SDRAM interfaces have been initialized, the configuration ROM controls the transfer of the Code Morphing software from the Code Morphing software flash memory to the SDRAM. Control is then transferred to the Code Morphing software and the configuration ROM is disabled. Transmeta will supply programming information for the configuration ROM. The recommended ROM device is the 93LC56B-I/SN from Microchip Technology, Inc.

The Code Morphing software boot ROM interface is a five-pin interface used to read data from a serial flash ROM. This interface may also be used for in-system reprogramming. The flash ROM device stores the Code Morphing software. During the boot process, the Code Morphing software is copied from the flash memory to the SDRAM. The Code Morphing software boot ROM interface supports up to 1 MByte of total storage using either two 512 kByte devices or a single 1 MByte device. Transmeta will supply programming information for the Code Morphing software boot ROM.

1.6 Clocks

The TM5400/TM5600 input clock (CLKIN) is multiplied up by the CPU clock multiplier to generate the CPU core clock. For currently defined TM5400/TM5600 part numbers, CLKIN is assumed to be 66 MHz. With a 66 MHz CLKIN, a CPU clock multiplier of 7.5 is used for a 500 MHz core, 8 is used for a 533 MHz core, 9 is used for a 600 MHz core, and 10 is used for a 667 MHz core.

The CPU core clock is divided down by the DDR and SDR clock dividers to generate the DDR SDRAM and SDR SDRAM interface clocks. See “DDR SDRAM Interface” on page 13 for additional information on DDR frequency settings and “SDR SDRAM Interface” on page 14 for information on SDR frequency settings.

There is also a TM5400/TM5600 clock divider that must be initialized for the PCI interface. Since the PCI interface operates at 33 MHz, the PCI clock divider for a 500 MHz core is 15, for a 533 MHz core is 16, for a 600 MHz core is 18, and for a 667 MHz core is 20. The clock multiplier and divider values are programmed into the TM5400/TM5600 during initialization from data stored in the configuration ROM.

1.7 Power Management

1.7.1 Power Management States

The TM5400/TM5600 in conjunction with the Code Morphing software, supports ACPI-compliant power management modes. Table 6 lists the state of the TM5400/TM5600 processor for each of the ACPI global system states. The TM5400/TM5600 power management states listed in Table 6 are defined in greater detail in Table 7 and the following paragraphs. The processor's power management states and state transitions are shown in Figure 3.

TABLE 6 Power Management System States

ACPI System State	Processor State	SDR SDRAM	Clock Generator	Delay to Return to C0 State[1]
G0/S0/C0: Working	Normal	Normal	Running	0
G0/S0/C1: Working/Auto Halt	Normal/ Auto Halt	Normal	Running	< 260 ns
G0/S0/C2: Working/Quick Start	Normal/ Quick Start	Normal/ Self refresh	Running	< 2.8 µs
G1/S1/C1: Sleeping/Auto Halt	Auto Halt	Normal	Running	< 260 ns
G1/S1/C2: Sleeping/Quick Start	Quick Start	Self refresh	Running	<2.8 ns
G1/S1/C3: Sleeping/Deep Sleep	Deep Sleep	Self refresh	CLKIN stopped	< 20 µs
G1/S3: Sleeping/Suspend to RAM	Off	Self refresh	All clocks stopped	10 ms + BIOS
G1/S4: Sleeping/Suspend to disk	Off	Off	Off	< 30 s
G2/S5: Soft off	Off	Off	Off	
G3: Mechanical off	Off	Off	Off	

1. Delay times specified assume a 533 MHz processor and a 33 MHz PCI bus frequency.

TABLE 7 TM5400/TM5600 Power Management States

P95 State	P95 Core	SDRAM	PCI Controller	Entry Trigger	Snoops	Interrupts
Normal	Running	Running	Running	Normal operation	Serviced	Serviced
Auto Halt	Stopped	Running	Running	Executing a HLT instruction	Serviced	Serviced
Quick Start	Stopped	Self refresh	Running	Asserting STPCLK#	Serviced	Latched
Deep Sleep	Stopped	Self refresh	Stopped	Asserting SLEEP# and stopping CLKIN while in Quick Start state	Not allowed	Not allowed

Auto Halt

The Auto Halt state is a low-power mode entered through the execution of the HLT instruction. The Auto Halt state is exited upon an interrupt (INTR, INIT#, SMI# or NMI) or assertion of RESET#. Snoops are serviced while in the Auto Halt state.

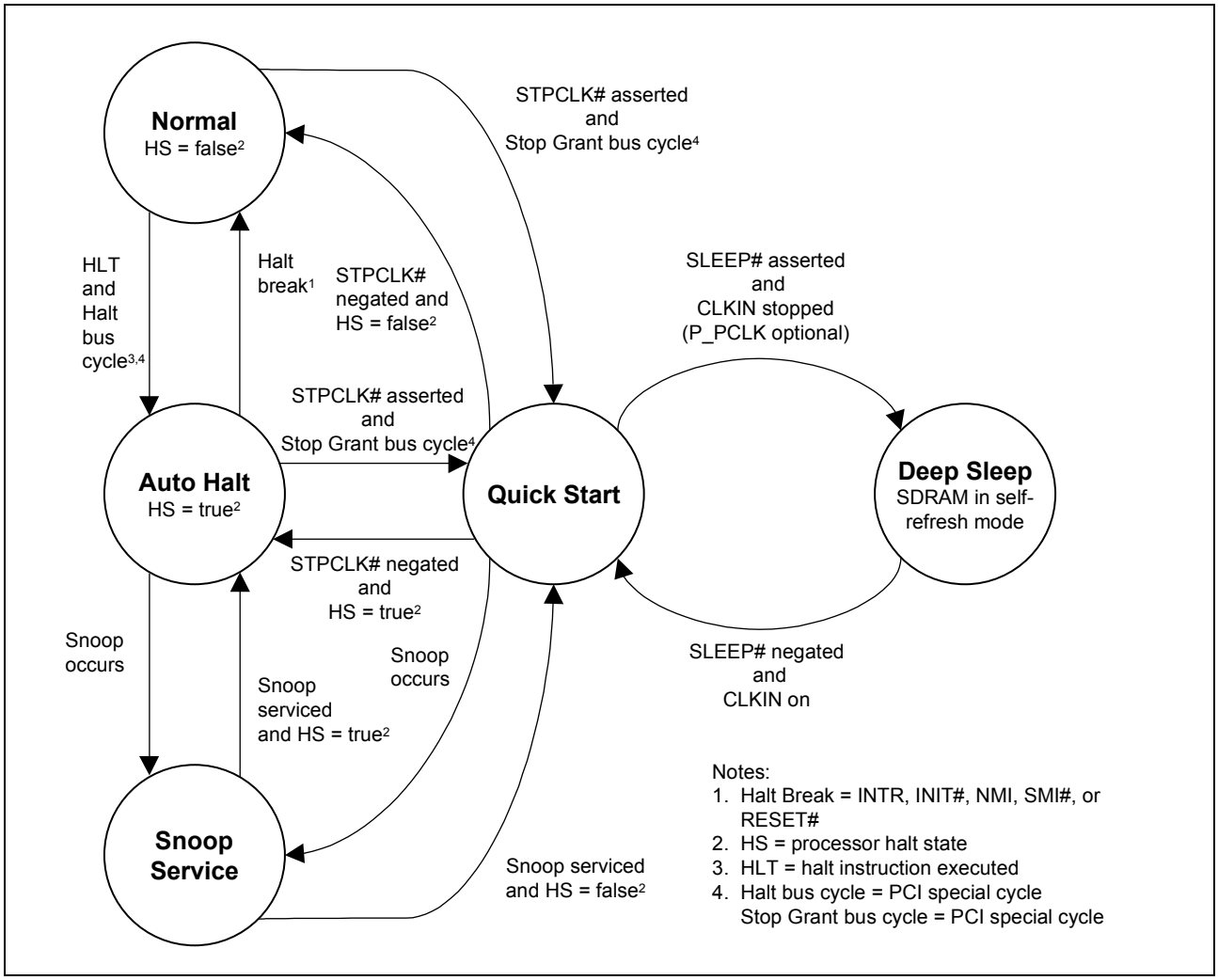
Quick Start

The Quick Start state is entered with the assertion of the STPCLK# input pin. While in Quick Start, snoops are serviced and interrupts are latched. Latched interrupts are serviced once the processor returns to the Normal state. Only one occurrence of an interrupt is latched while in Quick Start. If RESET# is asserted while in Quick Start, processor initialization occurs and then the processor returns to the Quick Start state if STPCLK# is still asserted.

Deep Sleep

The Deep Sleep state is the lowest power mode that the CPU can enter while maintaining its context. After entering Quick Start, the processor enters Deep Sleep when SLEEP# is asserted and the master clock input (CLKIN) is stopped. The PCI clock input (P_PCLK) may also be stopped. The TM5400/TM5600 internal PLL is shutdown while in Deep Sleep. Therefore, when the clocks are restarted to exit Deep Sleep, the system must allow time for PLL resynchronization to occur. Snoops are not serviced and interrupts are neither serviced nor latched while in Deep Sleep. RESET# is ignored while in Deep Sleep. CLKIN and P_PCLK should be stopped while in a logic low state.

FIGURE 3 Power Management State Machine



1.7.2 SDRAM Power Saving Mode

In addition to the power management states defined in the previous section, the TM5400/TM5600 provides an additional power saving mode for SDR SDRAM. Power Saving Mode may be enabled during normal operation by programming a TM5400/TM5600-specific PCI configuration register (`CD_MISC` for DDR SDRAM, `SD_MISC` for SDR SDRAM). In Power Saving Mode, the clock enable lines to the SDRAM are active only when the SDRAM is being accessed or refreshed. This mode decreases power dissipation, but increases the latency for a memory cycle by one SDRAM clock. Refer to the *TM5400/TM5600 BIOS Programmer's Guide* for additional information.

1.8 Test and Debug

The TM5400/TM5600 provides a 5-pin JTAG interface that can be used for TM5400/TM5600 testing. This interface supports IEEE 1149.1, EXTEST, BYPASS, and HiZ. Sample/preload instructions are implemented.

1.9 Supply Voltages

The TM5400/TM5600 processor requires four supply voltages. The core supply voltage (CVDD) varies from 1.2 to 1.6 volts nominally. Two I/O supply voltages are required: IOVDD is 3.3 volts, and IOVDD25 is 2.5 volts. There is also a single supply pin for the TM5400/TM5600 PLL circuit. The PLL supply voltage (PLLVDD) must equal the core supply voltage.

1.10 Power On Sequence

The sequence of operations required to power on the TM5400/TM5600 processor is listed below:

1. **Apply power to the system.** Allow CVDD, IOVDD, IOVDD25 and PLLVDD to reach minimum operating levels. During power up, the supplies should ramp within 250 ms of each other. See "Power On Specifications" on page 60 for additional information. RESET#, P_PCI_RST# and PWRGOOD should all be held low during this time. With PWRGOOD at a low level, the TM5400/TM5600 processor is in a self-protecting mode.

2. **Assert PWRGOOD.** Assert PWRGOOD after all power supplies achieve 95% of their final voltage.

3. **Begin toggling CLKIN.** At or before the assertion of PWRGOOD, begin toggling CLKIN.

4. **Deassert P_PCI_RST# and RESET#.** P_PCI_RST# must be held low until at least 1 ms after CLKIN begins to toggle. It also must be held low until at least 1 ms after the PWRGOOD rising edge.

5. **Load the TM5400/TM5600 mode bits from the configuration ROM.** Once P_PCI_RST# is deasserted, the TM5400/TM5600 begins reading data from the off-chip configuration ROM using the CFG_SCLK and CFG_SDATA pins. The frequency of CFG_SCLK is 920 kHz (CLKIN/72). The TM5400/TM5600 begins reading the configuration ROM by sending an eleven-bit sequence of 11000000000. This sequence tells the configuration ROM to begin supplying data starting at address 0. There is a 1 clock delay to allow the direction of the CFG_SDATA pin to change from driving to receiving. The TM5400/TM5600 then issues 112 CFG_SCLKs to read the contents of the configuration ROM. The entire sequence completes in approximately 130 µs.

6. **Complete internal reset sequence.** The TM5400/TM5600 internal reset sequence continues for approximately 800 ms plus an additional 64 internal clock cycles after the rising edge of RESET#. The TM5400/TM5600 then fetches its first instruction from either the serial boot ROM or from the PCI bus as determined by an internal mode bit.

Chapter 2

Pin Description

The following paragraphs document the signal definitions, pin assignments, and footprint for the TM5400/TM5600 processor.

2.1 Signal Definitions

Table 8 provides a summary of the TM5400/TM5600 signals. Table 9 through Table 22 describe the function of each signal on the TM5400/TM5600. Pins that are designated as "reserved" may have an internal electrical connection. Therefore, unless specified otherwise in Table 20, there should be no external electrical connection to the TM5400/TM5600 reserved pins.

Table 14 lists the memory address translation that corresponds to the various SDRAM devices supported by the TM5400/TM5600.

TABLE 8 Signal Summary

Signal Group	Quantity
SDR SDRAM	102
DDR SDRAM	109
PCI	62
Southbridge Sidebands	6
Serial Interfaces	9
Master Clock and Reset	2
Power Management	5
Miscellaneous	9
JTAG	5
Power	64
Ground	76
Reserved	25
TOTAL	474

TABLE 9 DDR SDRAM Interface Signals

Signal Name	Type	Qty	Description
C_A[12:0]	O	13	**Memory Address.** These pins carry row and column addressing information.
C_BA[1:0]	O	2	**Bank Address.** These pins carry the bank address for the DDR SDRAM devices.
C_CAS#	O	1	**Column Address Strobe.** When asserted low, enables latching of the column address on the positive edge of the next clock.
C_CKE[1:0]	O	2	**Clock Enable.** When deasserted, the SDRAMs enter power down mode. C_CKE[1] and C_CKE[0] are identical, provided for loading; each drives one block.
C_CLKA, C_CLKA#, C_CLKB, C_CLKB#	O	4	**SDRAM Clocks.** Differential clocks for the multiple banks of SDRAM. All SDRAM operations are synchronized to the clock.
C_CS#[3:0]	O	4	**Chip Select.** An SDRAM row is selected when its C_CS# pin is asserted low.
C_DQ[63:0]	I/O	64	**Memory Data.** This is the 64-bit data bus to the DDR SDRAMs.
C_DQMB[7:0]	O	8	**Data Mask.** Used during read or write operations, one C_DQMB pin per data byte.
C_DQS[7:0]	I/O	8	**Data Strobe.** Used to capture data at the processor and SDRAM. When sending data to SDRAM, the strobe signal is centered to the data. When receiving data from SDRAM, the strobe is edge aligned to the data.
C_RAS#	O	1	**Row Address Strobe.** When asserted low, enables latching of the row address on the positive edge of the next clock.
C_VREF	I	1	**Voltage Reference.** Reference voltage for the DDR SDRAM interface inputs. Used for SSTL_2 interface.
C_WE#	O	1	**Memory Write Enable.** Enables write operations to the DDR SDRAMs.

TABLE 10 Logical Alignment of DDR Byte Enables, Data Strobes and Data Bits

Byte Enable	Data Strobe	Data Bits
C_DQMB[0]	C_DQS[0]	C_DQ[7:0]
C_DQMB[1]	C_DQS[1]	C_DQ[15:8]
C_DQMB[2]	C_DQS[2]	C_DQ[23:16]
C_DQMB[3]	C_DQS[3]	C_DQ[31:24]
C_DQMB[4]	C_DQS[4]	C_DQ[39:32]
C_DQMB[5]	C_DQS[5]	C_DQ[47:40]
C_DQMB[6]	C_DQS[6]	C_DQ[55:48]
C_DQMB[7]	C_DQS[7]	C_DQ[63:56]

TABLE 11 SDR SDRAM Interface Signals

Signal Name	Type	Qty	Description
S_A[12:0]	O	13	**Memory Address.** These pins carry row and column addressing information.
S_BA[1:0]	O	2	**Bank Address.** These pins carry the bank address for the SDR SDRAM.
S_CAS#	O	1	**Column Address Strobe.** When asserted low, enables latching of the column address on the positive edge of the next clock.
S_CKE[1:0]	O	2	**Clock Enable.** When deasserted, the SDRAMs enter power down mode. Each S_CKE output drives up to 2 blocks.
S_CLK[3:0]	O	4	**SDRAM Clocks.** Clocks for the multiple rows of SDRAM. S_CLK[3:0] are identical, provided for loading; each drives one row.
S_CLKIN	I	1	**Clock input.** Return of S_CLKOUT used to calibrate the board delay of S_CLK[3:0] to the actual SDR SDRAM devices.
S_CLKOUT	O	1	**Clock output.** Clock output used in conjunction with S_CLKIN to calibrate the board delay of S_CLK[3:0] to the actual SDR SDRAM devices.
S_CS#[3:0]	O	4	**Chip Select.** An SDRAM block is selected when its S_CS# pin is asserted low. S_CS#[1:0] are used for slot 0, and S_CS#[3:2] are used for slot 1.
S_DQ[63:0]	I/O	64	**Memory Data.** This is the 64-bit data bus to the SDRAM.
S_DQMB[7:0]	O	8	**Data Mask.** Used during read or write operations, one S_DQMB pin per data byte.
S_RAS#	O	1	**Row Address Strobe.** When asserted low, enables latching of the row address on the positive edge of the next clock.
S_WE#	O	1	**Memory Write Enable.** Enables write operations to the SDRAMs.

TABLE 12 Logical Alignment of SDR Clocks, Clock Enables, and Chip Selects

Clock	Clock Enable	Chip Select
Any S_CLK	S_CKE[0]	S_CS#[0]
Any S_CLK	S_CKE[0]	S_CS#[1]
Any S_CLK	S_CKE[1]	S_CS#[2]
Any S_CLK	S_CKE[1]	S_CS#[3]

TABLE 13 Logical Alignment of SDR Byte Enables and Data Bits

Byte Enable	Data Bits
S_DQMB[0]	S_DQ[7:0]
S_DQMB[1]	S_DQ[15:8]
S_DQMB[2]	S_DQ[23:16]
S_DQMB[3]	S_DQ[31:24]
S_DQMB[4]	S_DQ[39:32]
S_DQMB[5]	S_DQ[47:40]
S_DQMB[6]	S_DQ[55:48]
S_DQMB[7]	S_DQ[63:56]

TABLE 14 Memory Address Translations

SDRAM Device Config[1]	CS#	BS1	BS0	C10[2]	C09	C08	C(07-00)	R12	R11	R(10-00)
16M / 2Bank:										
1M x 16	A23	--	A11	--	--	--	A(10-03)	--	--	A(22-12)
2M x 8	A24	--	A11	--	--	A23	A(10-03)	--	--	A(22-12)
4M x 4	A25	--	A11	--	A24	A23	A(10-03)	--	--	A(22-12)
64M / 4Bank:										
2M x 32	A24	A23	A11	--	--	--	A(10-03)	--	--	A(22-12)
4M x 16	A25	A23	A11	--	--	--	A(10-03)	--	A24	A(22-12)
8M x 8	A26	A23	A11	--	--	A25	A(10-03)	--	A24	A(22-12)
16M x 4	A27	A23	A11	--	A26	A25	A(10:03)	--	A24	A(22-12)
128M / 4Bank:										
4M x 32	A25	A23	A11	--	--	--	A(10-03)	A25	A24	A(22-12)
8M x 16	A26	A23	A11	--	--	A25	A(10-03)	A25	A24	A(22-12)
16M x 8	A27	A23	A11	--	A26	A25	A(10-03)	A25	A24	A(22-12)
32M x 4	A28	A23	A11	A27	A26	A25	A(10-03)	A25	A24	A(22-12)
256M / 4Bank:										
8M x 32	A26	A23	A11	--	--	--	A(10-03)	A25	A24	A(22-12)
16M x 16	A27	A23	A11	--	--	A26	A(10-03)	A25	A24	A(22-12)
32M x 8	A28	A23	A11	--	A27	A26	A(10-03)	A25	A24	A(22-12)
64M x 4	A29	A23	A11	A28	A27	A26	A(10-03)	A25	A24	A(22-12)

1. SDRAM device configuration is as follows: nM, xB = n Mbits, x banks.
2. Column address 10 (C10) is sent out on address pin 11 during CAS cycle rather than address pin 10.

Key:
CS# = Chip select or side select
B*n* = Bank select
C*nn* = SDRAM column address
R*nn* = SDRAM row address
A*nn* = Processor address *nn*

TABLE 15 PCI Interface Signals

Signal Name	Type	Qty	Description
P_AD[31:0]	I/O	32	**Address/Data.** The address is driven with P_FRAME#, and data is written or read with subsequent clocks.
P_C/BE#[3:0]	I/O	4	**Command/Byte Enable.** Command is driven with P_FRAME#. Byte enables correspond with the appropriate data on the PCI during read and write data cycles.
P_CLKRUN#	I/O	1	**Clock Run.** This signal is open drain, and an external 2.7K resistor is required. When asserted low, the PCI clock is enabled to run.
P_DEVSEL#	I/O	1	**Device Select.** Driven when a PCI initiator is accessing SDRAM.
P_FRAME#	I/O	1	**Frame.** Asserted active low to indicate the beginning of a PCI access (address phase). Forced inactive high to indicate that another transfer is desired by the initiator of the cycle.
P_GNT#[5:0]	O	6	**Grant.** Permission is given for a master to use the PCI bus.
P_HLDA#	O	1	**PCI Hold Acknowledge.** Driven to a bridge device in response to its P_HOLD# request to indicate that the bridge can take control of the PCI.
P_HOLD#	I	1	**PCI Hold.** Asserted by an expansion bridge to request use of the PCI bus.
P_IRDY#	I/O	1	**Initiator Ready.** Asserted by the initiator to indicate that it is ready for data transfer.
P_LOCK#	I/O	1	**Lock.** While asserted, the currently accessed PCI resource is locked.
P_PAR	I/O	1	**Parity.** Single bit representing the parity of lines P_AD[31:0] and P_C/BE#[3:0].
P_PCI_RST#	I/O	1	**Reset.** Asynchronously resets the module PCI interface and North Bridge, and puts all PCI signals into tristate.
P_PCLK	I	1	**PCI Clock.**
P_PERR#	I/O	1	**PCI Parity Error.**
P_REQ#[5:0]	I	6	**PCI Request.** A PCI master asserts this to request access to the PCI bus.
P_SERR#	I	1	**System error.**
P_STOP#	I/O	1	**Stop.** Asserted by a target device to request the master stop driving the PCI bus.
P_TRDY#	I/O	1	**Target Ready.** Asserted by the target to indicate that it is ready for a data transfer.

TABLE 16 Southbridge Sideband Interface Signals

Signal Name	Type	Qty	Description
FERR#	O	1	**Floating Point Unit Error.** Driven by the processor when a floating point error is detected.
IGNNE#	I	1	**Ignore Numeric Error.** Driven by the southbridge, this signal instructs the processor to ignore numeric exceptions and to continue to execute non-control floating point instructions.
INIT#	I	1	**Initialize.** Asserted by the southbridge for system initialization. If INIT# is asserted, the processor resets internal integer registers.
INTR	I	1	**Interrupt.** Driven by the southbridge to the processor to indicate that a maskable interrupt from a device is pending.
NMI	I	1	**Non-Maskable Interrupt.** Forces a non-maskable interrupt to the processor.
SMI#	I	1	**System Management Interrupt.** This input requests that an interrupt be serviced for system management functions such as power control.

TABLE 17 Serial Interface Signals

Signal Name	Type	Qty	Description
S_SCLK	I/O	1	**Serial Clock.** Clock for debug interface to SDR SDRAM.
S_SDATA	I/O	1	**Serial Data.** Data for debug interface to SDR SDRAM.
CFG_SCLK	O	1	**Configuration ROM Clock.** Clock for the serial interface to the configuration ROM. Reading the configuration ROM is initiated by deassertion of P_RST# and is clocked at a frequency of CLKIN x 1/72.
CFG_SDATA	I/O	1	**Configuration ROM Data.** Data for the serial interface to the configuration ROM.
SROM_CS#[1:0]	O	2	**Code Morphing Software Boot ROM Chip Selects.** When using two 512 kByte devices, SROM_CS#[0] selects the lower 512 kBytes and SROM_CS#[1] selects the upper 512 kBytes. When using a single 1 MByte device, only SROM_CS#[0] is used.
SROM_SCLK	O	1	**Code Morphing Software Boot ROM Clock.** Clock from TM5400/TM5600 to Code Morphing software boot ROM.
SROM_SIN	I	1	**Code Morphing Software Boot ROM Serial Data In.** Data from Code Morphing software boot ROM to TM5400/TM5600.
SROM_SOUT	O	1	**Code Morphing Software Boot ROM Serial Data Out.** Data from TM5400/TM5600 to Code Morphing software boot ROM.

TABLE 18 Master Clock and Reset Signals

Signal Name	Type	Qty	Description
CLKIN	I	1	**Clock In.** TM5400/TM5600 master clock input.
RESET#	I	1	**Reset.** TM5400/TM5600 master reset input.

TABLE 19 Power Management Interface Signals

Signal Name	Type	Qty	Description
PWRGOOD	I	1	**Power Good.** Indicates that the input clock and power supplies are stable.
SLEEP#	I	1	**Sleep.** Used to put the TM5400/TM5600 into a low power deep sleep mode. Turns off PCI interface by stopping PCI clock and tri-stating PCI pins. Allows P_PCLK to be stopped.
STPCLK#	I	1	**Stop Clock.** Stops the internal clocks of the TM5400/ TM5600 with the exception of the internal master controller and the PCI controller.
DIODE_CATHODE	O	1	**Thermal Diode.** Cathode for the internal thermal diode used to monitor the die temperature.
DIODE_ANODE	I	1	**Thermal Diode.** Anode for the internal thermal diode used to monitor the die temperature.

TABLE 20 Miscellaneous Signals

Signal Name	Type	Qty	Description
EPROMA[2:0]	O	3	**BIOS ROM Address Bits.** EPROMA[2:1] are used as address bits [19:18] for the BIOS EPROM. EPROMA[0] is not used, and there should be no electrical connection to it.
DEBUG_INT	I	1	**Debug Input.** This pin is used for debugging purposes only. For proper operation, DEBUG_INT should be connected to GND through a 4.7K resistor.
VRDA[4:0]	O	5	**Voltage Regulator Control.** These pins are programmable outputs intended to be used as control inputs to the system voltage regulator. They facilitate fine tuning of the core voltage supply (CVDD) to minimize power or maximize performance.
	I	12	**Reserved Test Inputs.** For proper operation, these reserved pins should be connected as follows: 4.7K pull-down: Reserved (E7) Reserved (G13) Reserved (W11) 4.7K pull-up to IOVDD: Reserved (F7) Reserved (G1) Reserved (G2) Reserved (H5) Reserved (H6) Reserved (V1) Reserved (V2) Reserved (V3) Reserved (W6) There should be no external electrical connection to all other reserved pins.

TABLE 21 JTAG Interface Signals

Signal Name	Type	Qty	Description
TCK	I	1	**Test Clock.**
TDI	I	1	**Test Data In.** This pin has an internal pull-up.
TDO	O	1	**Test Data Out.**
TMS	I	1	**Test Mode Select.** This pin has an internal pull-up.
TRST#	I	1	**Test Reset.** TRST# is an asynchronous input that resets the test logic in the TM5400/TM5600. This pin has an internal pull-up. TRST# must be connected to RESET# if the JTAG interface pins are not going to be used.

TABLE 22 Power and Ground Signals

Signal Name	Qty	Description
CVDD	23	**Core Supply.** CVDD = 1.2-1.6V nominal.
IOVDD	28	**3.3V I/O Supply.** IOVDD = 3.3V nominal.
IOVDD25	12	**2.5V I/O Supply.** IOVDD25 = 2.5V nominal.
PLLVDD	1	**PLL Supply.** PLLVDD = CVDD.
VSS	76	**Ground.**

2.2 I/O Signal Listings

The following tables summarize signal characteristics for each of the I/O signal pins. Table 23 lists the input signals, Table 24 lists the output signals and Table 25 lists the bidirectional signals.

TABLE 23 Input Only Signals

Signal Name	Internal Resistor	Active Level	Clock Domain	DC Specs	AC Specs
C_VREF	-	-	-	Table 29	-
CLKIN	-	-	-	Table 32	”3.5.2”, ”3.5.3”
DEBUG_INT	-	High	Asynchronous	Table 45	-
DIODE_ANODE	-	-	-	Table 35	-
IGNNE#	-	Low	Asynchronous	Table 32	”3.5.7”
INIT#	-	Low	Asynchronous	Table 32	”3.5.7”
INTR	-	High	Asynchronous	Table 32	”3.5.7”
NMI	-	High	Asynchronous	Table 32	”3.5.7”
P_HOLD#	-	Low	P_PCLK	Table 34	”3.5.6”
P_PCLK	-	-	-	Table 34	”3.5.2”, ”3.5.3”, ”3.5.6”
P_SERR#	-	Low	P_PCLK	Table 34	”3.5.6”
P_REQ#[5:0]	-	Low	P_PCLK	Table 34	”3.5.6”
PWRGOOD	-	High	Asynchronous	Table 32	”3.5.2”, ”3.5.7”
RESET#	-	Low	Asynchronous	Table 32	”3.5.2”
S_CLKIN	-	-	-	Table 32	”3.5.3”, ”3.5.5”
SLEEP#	-	Low	Asynchronous	Table 32	”3.5.7”
SMI#	-	Low	Asynchronous	Table 32	”3.5.7”
SROM_SIN	-	-	SROM_SCLK	Table 32	”3.5.9”
STPCLK#	-	Low	Asynchronous	Table 32	”3.5.7”
TCK	-	-	-	Table 32	”3.5.11”
TDI	Pull-up	High	TCK	Table 32	”3.5.11”
TMS	Pull-up	High	TCK	Table 32	”3.5.11”
TRST#	Pull-up	Low	Asynchronous	Table 32	”3.5.11”

TABLE 24 Output Only Signals

Signal Name	Pin Type	Active Level	Clock	Reset State	Doze State[1]	DC Specs	AC Specs
C_A[12:0]	Tri-state	-	C_CLK	1/0	Hi-Z	Table 33	”3.5.4”
C_BA[1:0]	Tri-state	High	C_CLK	1/0	Hi-Z	Table 33	”3.5.4”
C_CAS#	Tri-state	Low	C_CLK	1	Hi-Z	Table 33	”3.5.4”
C_CKE[1:0]	Tri-state	High	C_CLK	0	0	Table 33	”3.5.4”
C_CLKA, C_CLKA#, C_CLKB, C_CLKB#	Tri-state	-	-	Toggle	Hi-Z	Table 33	”3.5.4”
C_CS#[3:0]	Tri-state	Low	C_CLK	1	Hi-Z	Table 33	”3.5.4”
C_DQMB[7:0]	Tri-state	High	C_CLK	0	Hi-Z	Table 33	”3.5.4”
C_RAS#	Tri-state	Low	C_CLK	1	Hi-Z	Table 33	”3.5.4”
C_WE#	Tri-state	Low	C_CLK	1	Hi-Z	Table 33	”3.5.4”
CFG_SCLK	Tri-state	-	-	Hi-Z	Hi-Z	Table 32	”3.5.10”
DIODE_CATHODE	Tri-state	-	-	Lo-Z	Lo-Z	Table 35	-
EPROMA[2:0]	Tri-state	High	Asynch.	0	Hi-Z	Table 32	-
FERR#	Open drain	Low	Asynch.	Hi-Z	Hi-Z	Table 32	-
P_GNT#[5:0]	Tri-state	Low	P_PCLK	Hi-Z	Hi-Z	Table 34	”3.5.6”
P_HLDA#	Tri-state	Low	P_PCLK	Hi-Z	Hi-Z	Table 34	”3.5.6”
S_A[12:0]	Tri-state	-	S_CLKIN	1	Hi-Z	Table 32	”3.5.5”
S_BA[1:0]	Tri-state	High	S_CLKIN	1	Hi-Z	Table 32	”3.5.5”
S_CAS#	Tri-state	Low	S_CLKIN	1	Hi-Z	Table 32	”3.5.5”
S_CKE[1:0]	Tri-state	High	S_CLKIN	0	0	Table 32	”3.5.5”
S_CLK[3:0]	Tri-state	-	-	Toggle	Hi-Z	Table 32	”3.5.5”
S_CLKOUT	Tri-state	-	-	Toggle	Hi-Z	Table 32	”3.5.5”
S_CS#[3:0]	Tri-state	Low	S_CLKIN	1	Hi-Z	Table 32	”3.5.5”
S_DQMB[7:0]	Tri-state	High	S_CLKIN	1	Hi-Z	Table 32	”3.5.5”
S_RAS#	Tri-state	Low	S_CLKIN	1	Hi-Z	Table 32	”3.5.5”
S_WE#	Tri-state	Low	S_CLKIN	1	Hi-Z	Table 32	”3.5.5”
SROM_CS#[1:0]	Tri-state	Low	SROM_SCLK	Hi-Z	Hi-Z	Table 32	”3.5.9”
SROM_SCLK	Tri-state	-	-	Hi-Z	Hi-Z	Table 32	”3.5.9”
SROM_SOUT	Tri-state	-	SROM_SCLK	Hi-Z	Hi-Z	Table 32	”3.5.9”
TDO	Tri-state	-	TCK	Hi-Z	Hi-Z	Table 32	”3.5.11”
VRDA[4:0]	Open drain	-	-	1/0	Lo-Z	Table 32	-

1. See Table 25, Note 1.

TABLE 25 Bidirectional Signals

Signal Name	Pin Type	Active Level	Clock	Reset State	Doze State[1]	DC Specs	AC Specs
C_DQ[63:0]		-	C_CLK	Hi-Z	Hi-Z	Table 33	”3.5.4”
C_DQS[7:0]		-	C_CLK	Hi-Z	Hi-Z	Table 33	”3.5.4”
CFG_SDATA		-	CFG_SCLK	Hi-Z	Hi-Z	Table 32	”3.5.10”
P_AD[31:0]		-	P_PCLK	0	Hi-Z	Table 34	”3.5.6”
P_C/BE#[3:0]		Low	P_PCLK	0	Hi-Z	Table 34	”3.5.6”
P_CLKRUN#	Open drain	Low	P_PCLK	Hi-Z	Hi-Z	Table 34	”3.5.6”
P_DEVSEL#		Low	P_PCLK	Hi-Z	Hi-Z	Table 34	”3.5.6”
P_FRAME#		Low	P_PCLK	Hi-Z	Hi-Z	Table 34	”3.5.6”
P_IRDY#		Low	P_PCLK	Hi-Z	Hi-Z	Table 34	”3.5.6”
P_LOCK#		Low	P_PCLK	Hi-Z	Hi-Z	Table 34	”3.5.6”
P_PAR		High	P_PCLK	0	Hi-Z	Table 34	”3.5.6”
P_PCI_RST#		Low	Asynch.	-	Hi-Z	Table 34	”3.5.2”, ”3.5.6”
P_PERR#		Low	P_PCLK	Hi-Z	Hi-Z	Table 34	”3.5.6”
P_STOP#		Low	P_PCLK	Hi-Z	Hi-Z	Table 34	”3.5.6”
P_TRDY#		Low	P_PCLK	Hi-Z	Hi-Z	Table 34	”3.5.6”
S_DQ[63:0]		-	S_CLKIN	Hi-Z	Hi-Z	Table 32	”3.5.5”
S_SCLK	Open drain	-	-	Hi-Z	Hi-Z	Table 32	”3.5.8”
S_SDATA	Open drain	-	S_SCLK	Hi-Z	Hi-Z	Table 32	”3.5.8”

1. Doze state refers to the state of the signal during low-power modes when the specific interface is disabled. In the case of the SDRAM interfaces, the doze state refers to the state of the signal while the SDRAM is in self-refresh.

2.3 Footprint and Pin Assignments

Figure 4 shows the TM5400/TM5600 package footprint. Table 26 and Table 27 list the pin assignments for each signal on the TM5400/TM5600.

FIGURE 4 Package Footprint - Top Down View

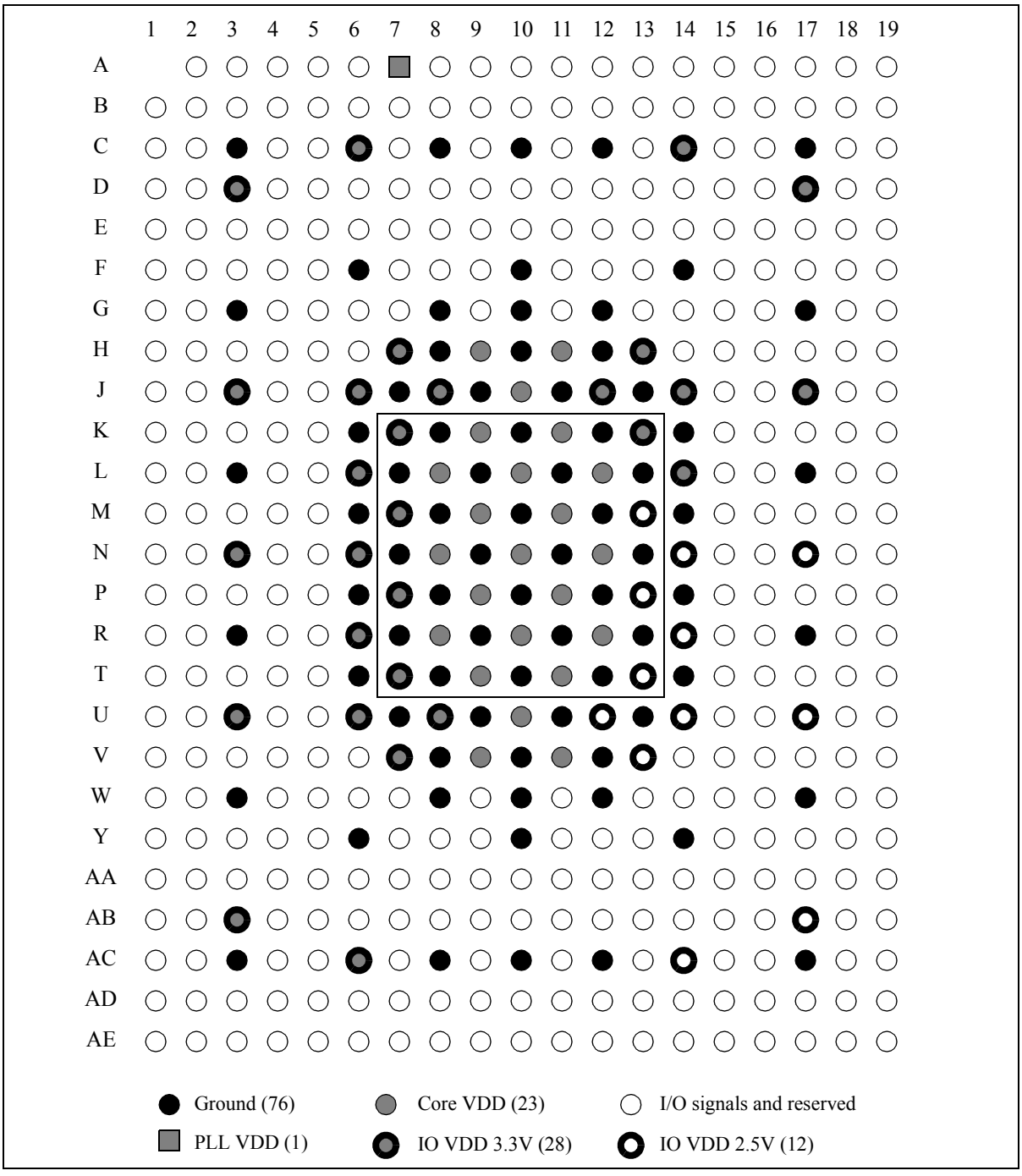


TABLE 26 TM5400/TM5600 Pin Assignments - Sorted by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
A1	No Pin	B16	DIODE_CATHODE	D12	P_AD[20]
A2	S_DQ[59]	B17	P_AD[3]	D13	P_SERR#
A3	S_DQ[57]	B18	P_AD[2]	D14	P_AD[14]
A4	S_DQ[60]	B19	P_AD[0]	D15	P_AD[10]
A5	S_DQ[56]	C1	S_DQ[53]	D16	P_AD[4]
A6	S_SCLK	C2	S_DQ[55]	D17	IOVDD
A7	PLLVDD	C3	GND	D18	P_REQ#[1]
A8	CFG_SDATA	C4	S_DQ[31]	D19	P_REQ#[0]
A9	P_AD[30]	C5	S_DQ[30]	E1	S_DQ[50]
A10	P_AD[31]	C6	IOVDD	E2	S_DQ[52]
A11	P_C/BE#[2]	C7	CLKIN	E3	S_DQ[26]
A12	P_C/BE#[0]	C8	GND	E4	S_DQ[27]
A13	P_FRAME#	C9	P_AD[28]	E5	S_DQ[22]
A14	P_LOCK#	C10	GND	E6	S_DQ[19]
A15	P_GNT#[3]	C11	P_AD[21]	E7	Reserved (E7)
A16	P_GNT#[1]	C12	GND	E8	P_PCI_RST#
A17	P_DEVSEL#	C13	P_STOP#	E9	P_AD[25]
A18	DIODE_ANODE	C14	IOVDD	E10	P_AD[22]
A19	TMS	C15	P_AD[12]	E11	P_AD[18]
B1	S_DQ[63]	C16	P_AD[7]	E12	P_AD[16]
B2	S_DQ[62]	C17	GND	E13	P_HLDA#
B3	S_DQ[61]	C18	P_AD[1]	E14	P_AD[13]
B4	S_DQ[58]	C19	P_HOLD#	E15	P_AD[9]
B5	S_DQ[29]	D1	S_DQ[51]	E16	P_AD[5]
B6	S_SDATA	D2	S_DQ[54]	E17	P_AD[6]
B7	CFG_SCLK	D3	IOVDD	E18	P_REQ#[3]
B8	P_AD[27]	D4	S_DQ[28]	E19	P_REQ#[2]
B9	P_AD[29]	D5	S_DQ[21]	F1	S_DQ[48]
B10	P_C/BE#[3]	D6	S_DQ[23]	F2	S_DQ[49]
B11	P_C/BE#[1]	D7	Reserved	F3	S_DQ[25]
B12	P_IRDY#	D8	SLEEP#	F4	S_DQ[24]
B13	P_TRDY#	D9	P_AD[26]	F5	S_DQ[20]
B14	P_PAR	D10	P_AD[23]	F6	GND
B15	P_AD[15]	D11	P_AD[19]	F7	Reserved (F7)

TABLE 26 TM5400/TM5600 Pin Assignments - Sorted by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
F8	P_PCLK	H5	Reserved (H5)	K2	S_A[12]
F9	P_AD[24]	H6	Reserved (H6)	K3	Reserved
F10	GND	H7	IOVDD	K4	Reserved
F11	P_AD[17]	H8	GND	K5	Reserved
F12	P_PERR#	H9	CVDD	K6	GND
F13	P_GNT#[2]	H10	GND	K7	IOVDD
F14	GND	H11	CVDD	K8	GND
F15	P_AD[11]	H12	GND	K9	CVDD
F16	P_AD[8]	H13	IOVDD	K10	GND
F17	P_GNT#[5]	H14	DEBUG_INT	K11	CVDD
F18	P_REQ#[5]	H15	IGNNE#	K12	GND
F19	P_REQ#[4]	H16	FERR#	K13	IOVDD
G1	Reserved (G1)	H17	NMI	K14	GND
G2	Reserved (G2)	H18	STPCLK#	K15	SROM_CS#[0]
G3	GND	H19	RESET#	K16	C_DQ[32]
G4	S_DQ[16]	J1	S_CKE[1]	K17	SROM_SIN
G5	S_DQ[18]	J2	S_CKE[0]	K18	SROM_SOUT
G6	S_DQ[17]	J3	IOVDD	K19	C_VREF
G7	PWRGOOD	J4	Reserved	L1	S_BA[1]
G8	GND	J5	Reserved	L2	S_BA[0]
G9	TRST#	J6	IOVDD	L3	GND
G10	GND	J7	GND	L4	S_CLK[3]
G11	Reserved	J8	IOVDD	L5	Reserved
G12	GND	J9	GND	L6	IOVDD
G13	Reserved (G13)	J10	CVDD	L7	GND
G14	SMI#	J11	GND	L8	CVDD
G15	P_GNT#[0]	J12	IOVDD	L9	GND
G16	P_GNT#[4]	J13	GND	L10	CVDD
G17	GND	J14	IOVDD	L11	GND
G18	INIT#	J15	EPROMA[1]	L12	CVDD
G19	INTR	J16	EPROMA[0]	L13	GND
H1	S_DQMB[7]	J17	IOVDD	L14	IOVDD
H2	S_DQMB[6]	J18	P_CLKRUN#	L15	SROM_CS#[1]
H3	S_DQMB[3]	J19	EPROMA[2]	L16	SROM_SCLK
H4	S_DQMB[2]	K1	S_A[11]	L17	GND

TABLE 26 TM5400/TM5600 Pin Assignments - Sorted by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
L18	C_DQ[31]	N15	C_DQ[36]	R12	CVDD
L19	C_DQ[30]	N16	C_DQ[37]	R13	GND
M1	S_A[5]	N17	IOVDD25	R14	IOVDD25
M2	S_A[10]	N18	C_DQ[27]	R15	C_DQMB[4]
M3	S_CLK[0]	N19	C_DQ[26]	R16	C_DQMB[5]
M4	S_CLK[1]	P1	S_A[6]	R17	GND
M5	S_CLK[2]	P2	S_A[8]	R18	C_DQS[3]
M6	GND	P3	S_A[0]	R19	C_DQMB[3]
M7	IOVDD	P4	S_A[3]	T1	S_CS#[2]
M8	GND	P5	S_WE#	T2	S_CS#[3]
M9	CVDD	P6	GND	T3	S_CS#[1]
M10	GND	P7	IOVDD	T4	S_CS#[0]
M11	CVDD	P8	GND	T5	Reserved
M12	GND	P9	CVDD	T6	GND
M13	IOVDD25	P10	GND	T7	IOVDD
M14	GND	P11	CVDD	T8	GND
M15	C_DQ[33]	P12	GND	T9	CVDD
M16	C_DQ[34]	P13	IOVDD25	T10	GND
M17	C_DQ[35]	P14	GND	T11	CVDD
M18	C_DQ[29]	P15	C_DQ[38]	T12	GND
M19	C_DQ[28]	P16	C_DQ[39]	T13	IOVDD25
N1	S_A[7]	P17	C_DQS[4]	T14	GND
N2	S_A[9]	P18	C_DQ[25]	T15	C_DQS[5]
N3	IOVDD	P19	C_DQ[24]	T16	C_DQ[40]
N4	S_A[1]	R1	Reserved	T17	C_DQ[41]
N5	S_A[4]	R2	Reserved	T18	C_DQMB[2]
N6	IOVDD	R3	GND	T19	C_DQS[2]
N7	GND	R4	Reserved	U1	S_DQMB[0]
N8	CVDD	R5	S_RAS#	U2	S_DQMB[5]
N9	GND	R6	IOVDD	U3	IOVDD
N10	CVDD	R7	GND	U4	S_DQMB[1]
N11	GND	R8	CVDD	U5	S_DQMB[4]
N12	CVDD	R9	GND	U6	IOVDD
N13	GND	R10	CVDD	U7	GND
N14	IOVDD25	R11	GND	U8	IOVDD

TABLE 26 TM5400/TM5600 Pin Assignments - Sorted by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
U9	GND	W6	Reserved (W6)	AA3	S_DQ[12]
U10	CVDD	W7	TCK	AA4	S_DQ[11]
U11	GND	W8	GND	AA5	S_DQ[3]
U12	IOVDD25	W9	TDI	AA6	S_DQ[32]
U13	GND	W10	GND	AA7	C_A[7]
U14	IOVDD25	W11	Reserved (W11)	AA8	C_A[9]
U15	C_DQ[42]	W12	GND	AA9	C_CLKB
U16	C_DQ[43]	W13	VRDA[4]	AA10	C_CLKA
U17	IOVDD25	W14	VRDA[3]	AA11	C_DQ[62]
U18	C_DQ[23]	W15	C_DQ[47]	AA12	C_DQ[60]
U19	C_DQ[22]	W16	C_DQ[48]	AA13	C_DQ[57]
V1	Reserved (V1)	W17	GND	AA14	C_DQS[7]
V2	Reserved (V2)	W18	C_DQ[19]	AA15	C_DQ[52]
V3	Reserved (V3)	W19	C_DQ[18]	AA16	C_DQ[54]
V4	S_CAS#	Y1	S_DQ[45]	AA17	C_DQ[53]
V5	S_A[2]	Y2	S_DQ[44]	AA18	C_DQ[15]
V6	S_CLKOUT	Y3	S_DQ[14]	AA19	C_DQ[14]
V7	IOVDD	Y4	S_DQ[13]	AB1	S_DQ[41]
V8	GND	Y5	S_DQ[4]	AB2	S_DQ[40]
V9	CVDD	Y6	GND	AB3	IOVDD
V10	GND	Y7	C_CKE[1]	AB4	S_DQ[1]
V11	CVDD	Y8	C_CS#[1]	AB5	S_DQ[2]
V12	GND	Y9	C_CS#[2]	AB6	S_CLKIN
V13	IOVDD25	Y10	GND	AB7	C_A[6]
V14	VRDA[2]	Y11	C_CS#[3]	AB8	C_A[8]
V15	C_DQ[44]	Y12	VRDA[0]	AB9	C_A[12]
V16	C_DQ[45]	Y13	VRDA[1]	AB10	C_CLKB#
V17	C_DQ[46]	Y14	GND	AB11	C_DQ[63]
V18	C_DQ[21]	Y15	C_DQ[49]	AB12	C_DQ[61]
V19	C_DQ[20]	Y16	C_DQ[50]	AB13	C_DQ[58]
W1	S_DQ[47]	Y17	C_DQ[51]	AB14	C_DQ[56]
W2	S_DQ[46]	Y18	C_DQ[17]	AB15	C_DQMB[6]
W3	GND	Y19	C_DQ[16]	AB16	C_DQ[55]
W4	S_DQ[15]	AA1	S_DQ[43]	AB17	IOVDD25
W5	S_DQ[0]	AA2	S_DQ[42]	AB18	C_DQ[13]

TABLE 26 TM5400/TM5600 Pin Assignments - Sorted by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
AB19	C_DQ[12]	AD1	S_DQ[10]	AE1	TDO
AC1	S_DQ[9]	AD2	S_DQ[7]	AE2	S_DQ[39]
AC2	S_DQ[8]	AD3	S_DQ[6]	AE3	S_DQ[36]
AC3	GND	AD4	S_DQ[35]	AE4	S_DQ[38]
AC4	S_DQ[5]	AD5	S_DQ[34]	AE5	S_DQ[37]
AC5	S_DQ[33]	AD6	C_A[4]	AE6	C_CKE[0]
AC6	IOVDD	AD7	C_A[2]	AE7	C_A[3]
AC7	C_A[5]	AD8	C_A[0]	AE8	C_A[1]
AC8	GND	AD9	C_BA[1]	AE9	C_A[10]
AC9	C_A[11]	AD10	C_CS#[0]	AE10	C_BA[0]
AC10	GND	AD11	C_CAS#	AE11	C_RAS#
AC11	C_CLKA#	AD12	C_DQ[0]	AE12	C_WE#
AC12	GND	AD13	C_DQ[2]	AE13	C_DQ[1]
AC13	C_DQ[59]	AD14	C_DQ[4]	AE14	C_DQ[3]
AC14	IOVDD25	AD15	C_DQ[6]	AE15	C_DQ[5]
AC15	C_DQMB[7]	AD16	C_DQS[0]	AE16	C_DQ[7]
AC16	C_DQS[6]	AD17	C_DQMB[1]	AE17	C_DQMB[0]
AC17	GND	AD18	C_DQ[9]	AE18	C_DQS[1]
AC18	C_DQ[11]	AD19	C_DQ[8]	AE19	Reserved
AC19	C_DQ[10]				

TABLE 27 TM5400/TM5600 Pin Assignments - Sorted by Signal Name

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
C_A[0]	AD8	C_DQ[8]	AD19	C_DQ[42]	U15
C_A[1]	AE8	C_DQ[9]	AD18	C_DQ[43]	U16
C_A[2]	AD7	C_DQ[10]	AC19	C_DQ[44]	V15
C_A[3]	AE7	C_DQ[11]	AC18	C_DQ[45]	V16
C_A[4]	AD6	C_DQ[12]	AB19	C_DQ[46]	V17
C_A[5]	AC7	C_DQ[13]	AB18	C_DQ[47]	W15
C_A[6]	AB7	C_DQ[14]	AA19	C_DQ[48]	W16
C_A[7]	AA7	C_DQ[15]	AA18	C_DQ[49]	Y15
C_A[8]	AB8	C_DQ[16]	Y19	C_DQ[50]	Y16
C_A[9]	AA8	C_DQ[17]	Y18	C_DQ[51]	Y17
C_A[10]	AE9	C_DQ[18]	W19	C_DQ[52]	AA15
C_A[11]	AC9	C_DQ[19]	W18	C_DQ[53]	AA17
C_A[12]	AB9	C_DQ[20]	V19	C_DQ[54]	AA16
C_BA[0]	AE10	C_DQ[21]	V18	C_DQ[55]	AB16
C_BA[1]	AD9	C_DQ[22]	U19	C_DQ[56]	AB14
C_CAS#	AD11	C_DQ[23]	U18	C_DQ[57]	AA13
C_CKE[0]	AE6	C_DQ[24]	P19	C_DQ[58]	AB13
C_CKE[1]	Y7	C_DQ[25]	P18	C_DQ[59]	AC13
C_CLKA	AA10	C_DQ[26]	N19	C_DQ[60]	AA12
C_CLKA#	AC11	C_DQ[27]	N18	C_DQ[61]	AB12
C_CLKB	AA9	C_DQ[28]	M19	C_DQ[62]	AA11
C_CLKB#	AB10	C_DQ[29]	M18	C_DQ[63]	AB11
C_CS#[0]	AD10	C_DQ[30]	L19	C_DQMB[0]	AE17
C_CS#[1]	Y8	C_DQ[31]	L18	C_DQMB[1]	AD17
C_CS#[2]	Y9	C_DQ[32]	K16	C_DQMB[2]	T18
C_CS#[3]	Y11	C_DQ[33]	M15	C_DQMB[3]	R19
C_DQ[0]	AD12	C_DQ[34]	M16	C_DQMB[4]	R15
C_DQ[1]	AE13	C_DQ[35]	M17	C_DQMB[5]	R16
C_DQ[2]	AD13	C_DQ[36]	N15	C_DQMB[6]	AB15
C_DQ[3]	AE14	C_DQ[37]	N16	C_DQMB[7]	AC15
C_DQ[4]	AD14	C_DQ[38]	P15	C_DQS[0]	AD16
C_DQ[5]	AE15	C_DQ[39]	P16	C_DQS[1]	AE18
C_DQ[6]	AD15	C_DQ[40]	T16	C_DQS[2]	T19
C_DQ[7]	AE16	C_DQ[41]	T17	C_DQS[3]	R18

TABLE 27 TM5400/TM5600 Pin Assignments - Sorted by Signal Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
C_DQS[4]	P17	DIODE_CATHODE	B16	GND	L17
C_DQS[5]	T15	EPROMA[0]	J16	GND	M6
C_DQS[6]	AC16	EPROMA[1]	J15	GND	M8
C_DQS[7]	AA14	EPROMA[2]	J19	GND	M10
C_RAS#	AE11	FERR#	H16	GND	M12
C_VREF	K19	GND	C3	GND	M14
C_WE#	AE12	GND	C8	GND	N7
CFG_SCLK	B7	GND	C10	GND	N9
CFG_SDATA	A8	GND	C12	GND	N11
CLKIN	C7	GND	C17	GND	N13
CVDD	H9	GND	F6	GND	P6
CVDD	H11	GND	F10	GND	P8
CVDD	J10	GND	F14	GND	P10
CVDD	K9	GND	G3	GND	P12
CVDD	K11	GND	G8	GND	P14
CVDD	L8	GND	G10	GND	R3
CVDD	L10	GND	G12	GND	R7
CVDD	L12	GND	G17	GND	R9
CVDD	M9	GND	H8	GND	R11
CVDD	M11	GND	H10	GND	R13
CVDD	N8	GND	H12	GND	R17
CVDD	N10	GND	J7	GND	T6
CVDD	N12	GND	J9	GND	T8
CVDD	P9	GND	J11	GND	T10
CVDD	P11	GND	J13	GND	T12
CVDD	R8	GND	K6	GND	T14
CVDD	R10	GND	K8	GND	U7
CVDD	R12	GND	K10	GND	U9
CVDD	T9	GND	K12	GND	U11
CVDD	T11	GND	K14	GND	U13
CVDD	U10	GND	L3	GND	V8
CVDD	V9	GND	L7	GND	V10
CVDD	V11	GND	L9	GND	V12
DEBUG_INT	H14	GND	L11	GND	W3
DIODE_ANODE	A18	GND	L13	GND	W8

TABLE 27 TM5400/TM5600 Pin Assignments - Sorted by Signal Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
GND	W10	IOVDD	T7	P_AD[15]	B15
GND	W12	IOVDD	U3	P_AD[16]	E12
GND	W17	IOVDD	U6	P_AD[17]	F11
GND	Y6	IOVDD	U8	P_AD[18]	E11
GND	Y10	IOVDD	V7	P_AD[19]	D11
GND	Y14	IOVDD	AB3	P_AD[20]	D12
GND	AC3	IOVDD	AC6	P_AD[21]	C11
GND	AC8	IOVDD25	M13	P_AD[22]	E10
GND	AC10	IOVDD25	N14	P_AD[23]	D10
GND	AC12	IOVDD25	N17	P_AD[24]	F9
GND	AC17	IOVDD25	P13	P_AD[25]	E9
IGNNE#	H15	IOVDD25	R14	P_AD[26]	D9
INIT#	G18	IOVDD25	T13	P_AD[27]	B8
INTR	G19	IOVDD25	U12	P_AD[28]	C9
IOVDD	C6	IOVDD25	U14	P_AD[29]	B9
IOVDD	C14	IOVDD25	U17	P_AD[30]	A9
IOVDD	D3	IOVDD25	V13	P_AD[31]	A10
IOVDD	D17	IOVDD25	AB17	P_C/BE#[0]	A12
IOVDD	H7	IOVDD25	AC14	P_C/BE#[1]	B11
IOVDD	H13	NMI	H17	P_C/BE#[2]	A11
IOVDD	J3	P_AD[0]	B19	P_C/BE#[3]	B10
IOVDD	J6	P_AD[1]	C18	P_CLKRUN#	J18
IOVDD	J8	P_AD[2]	B18	P_DEVSEL#	A17
IOVDD	J12	P_AD[3]	B17	P_FRAME#	A13
IOVDD	J14	P_AD[4]	D16	P_GNT#[0]	G15
IOVDD	J17	P_AD[5]	E16	P_GNT#[1]	A16
IOVDD	K7	P_AD[6]	E17	P_GNT#[2]	F13
IOVDD	K13	P_AD[7]	C16	P_GNT#[3]	A15
IOVDD	L6	P_AD[8]	F16	P_GNT#[4]	G16
IOVDD	L14	P_AD[9]	E15	P_GNT#[5]	F17
IOVDD	M7	P_AD[10]	D15	P_HLDA#	E13
IOVDD	N3	P_AD[11]	F15	P_HOLD#	C19
IOVDD	N6	P_AD[12]	C15	P_IRDY#	B12
IOVDD	P7	P_AD[13]	E14	P_LOCK#	A14
IOVDD	R6	P_AD[14]	D14	P_PAR	B14

TABLE 27 TM5400/TM5600 Pin Assignments - Sorted by Signal Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
P_PCI_RST#	E8	Reserved (V3)	V3	S_DQ[2]	AB5
P_PCLK	F8	Reserved (W6)	W6	S_DQ[3]	AA5
P_PERR#	F12	Reserved (W11)	W11	S_DQ[4]	Y5
P_REQ#[0]	D19	Reserved	AE19	S_DQ[5]	AC4
P_REQ#[1]	D18	RESET#	H19	S_DQ[6]	AD3
P_REQ#[2]	E19	S_A[0]	P3	S_DQ[7]	AD2
P_REQ#[3]	E18	S_A[1]	N4	S_DQ[8]	AC2
P_REQ#[4]	F19	S_A[2]	V5	S_DQ[9]	AC1
P_REQ#[5]	F18	S_A[3]	P4	S_DQ[10]	AD1
P_SERR#	D13	S_A[4]	N5	S_DQ[11]	AA4
P_STOP#	C13	S_A[5]	M1	S_DQ[12]	AA3
P_TRDY#	B13	S_A[6]	P1	S_DQ[13]	Y4
PLLVDD	A7	S_A[7]	N1	S_DQ[14]	Y3
PWRGOOD	G7	S_A[8]	P2	S_DQ[15]	W4
Reserved	D7	S_A[9]	N2	S_DQ[16]	G4
Reserved (E7)	E7	S_A[10]	M2	S_DQ[17]	G6
Reserved (F7)	F7	S_A[11]	K1	S_DQ[18]	G5
Reserved (G1)	G1	S_A[12]	K2	S_DQ[19]	E6
Reserved (G2)	G2	S_BA[0]	L2	S_DQ[20]	F5
Reserved	G11	S_BA[1]	L1	S_DQ[21]	D5
Reserved (G13)	G13	S_CAS#	V4	S_DQ[22]	E5
Reserved (H5)	H5	S_CKE[0]	J2	S_DQ[23]	D6
Reserved (H6)	H6	S_CKE[1]	J1	S_DQ[24]	F4
Reserved	J4	S_CLK[0]	M3	S_DQ[25]	F3
Reserved	J5	S_CLK[1]	M4	S_DQ[26]	E3
Reserved	K3	S_CLK[2]	M5	S_DQ[27]	E4
Reserved	K4	S_CLK[3]	L4	S_DQ[28]	D4
Reserved	K5	S_CLKIN	AB6	S_DQ[29]	B5
Reserved	L5	S_CLKOUT	V6	S_DQ[30]	C5
Reserved	R1	S_CS#[0]	T4	S_DQ[31]	C4
Reserved	R2	S_CS#[1]	T3	S_DQ[32]	AA6
Reserved	R4	S_CS#[2]	T1	S_DQ[33]	AC5
Reserved	T5	S_CS#[3]	T2	S_DQ[34]	AD5
Reserved (V1)	V1	S_DQ[0]	W5	S_DQ[35]	AD4
Reserved (V2)	V2	S_DQ[1]	AB4	S_DQ[36]	AE3

TABLE 27 TM5400/TM5600 Pin Assignments - Sorted by Signal Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
S_DQ[37]	AE5	S_DQ[56]	A5	S_WE#	P5
S_DQ[38]	AE4	S_DQ[57]	A3	SLEEP#	D8
S_DQ[39]	AE2	S_DQ[58]	B4	SMI#	G14
S_DQ[40]	AB2	S_DQ[59]	A2	SROM_CS#[0]	K15
S_DQ[41]	AB1	S_DQ[60]	A4	SROM_CS#[1]	L15
S_DQ[42]	AA2	S_DQ[61]	B3	SROM_SCLK	L16
S_DQ[43]	AA1	S_DQ[62]	B2	SROM_SIN	K17
S_DQ[44]	Y2	S_DQ[63]	B1	SROM_SOUT	K18
S_DQ[45]	Y1	S_DQMB[0]	U1	STPCLK#	H18
S_DQ[46]	W2	S_DQMB[1]	U4	TCK	W7
S_DQ[47]	W1	S_DQMB[2]	H4	TDI	W9
S_DQ[48]	F1	S_DQMB[3]	H3	TDO	AE1
S_DQ[49]	F2	S_DQMB[4]	U5	TMS	A19
S_DQ[50]	E1	S_DQMB[5]	U2	TRST#	G9
S_DQ[51]	D1	S_DQMB[6]	H2	VRDA[0]	Y12
S_DQ[52]	E2	S_DQMB[7]	H1	VRDA[1]	Y13
S_DQ[53]	C1	S_RAS#	R5	VRDA[2]	V14
S_DQ[54]	D2	S_SCLK	A6	VRDA[3]	W14
S_DQ[55]	C2	S_SDATA	B6	VRDA[4]	W13

Chapter 3

Electrical Specifications

3.1 Absolute Maximum Ratings

TABLE 28 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum
CVDD	Core voltage	-0.2 V	2.35 V
IOVDD	3.3V I/O voltage	-0.2 V	3.6 V
IOVDD25	2.5V I/O voltage	-0.2 V	3.6 V
PLLVDD	PLL voltage	-0.2 V	2.35 V
-	IOVDD, IOVDD25 relative to CVDD, PLLVDD	0.0 V	3.465 V
V_{in}	Input voltage	-0.5 V	3.96 V
I_{in}	Input current	-100 mA	100 mA
$T_{storage}$	Storage temperature	-55°C	150°C

3.2 Recommended Operating Conditions

TABLE 29 Recommended Operating Conditions

Symbol	Parameter	Minimum	Nominal	Maximum
CVDD, PLLVDD	Core voltage, PLL voltage			
	500 MHz	1.52 V	1.6 V	1.68 V
	533 MHz			
	600 MHz			
	667 MHz			
	Minimum LongRun setting			
	300 MHz	1.14 V	1.2 V	1.26 V
IOVDD	3.3V I/O voltage	3.135 V	3.3 V	3.465 V
IOVDD25	2.5V I/O voltage	2.375 V	2.5 V	2.625 V
C_VREF	DDR SDRAM interface voltage reference	1.187 V	0.5 x IOVDD25	1.312 V
V_{in}	Input voltage	GND	-	IOVDD
T_j	Junction temperature	0°C	-	85°C

3.3 Power and Current Specifications

TABLE 30 TM5400/TM5600 Power Specifications

Parameter	CVDD Nominal [1]	Typical Power [1]	Maximum Power [1]	Notes
Thermal design power				
500 MHz	1.6 V	-	5.7 W	Thermal design power is the maximum average power measured over a 30 second interval, while running commercially available software.
533 MHz	1.6 V	-	5.9 W	
600 MHz	1.6 V	-	6.4 W	
667 MHz	1.6 V	-	7.3 W	
Typical operating power				
300-500 MHz	1.2-1.6 V	0.7 W	-	Typical operating power is measured while playing MP3 files with Windows Media Player under Windows™ 98 with LongRun power management enabled.
300-533 MHz	1.2-1.6 V	0.7 W	-	
300-600 MHz	1.2-1.6 V	0.7 W	-	
300-667 MHz	1.2-1.6 V	0.7 W	-	
Auto Halt power				
300-500 MHz	1.2-1.6 V	0.3 W	-	Auto Halt mode is entered by executing a HLT instruction. Typical Auto Halt power is measured with LongRun power management enabled.
300-533 MHz	1.2-1.6 V	0.3 W	-	
300-600 MHz	1.2-1.6 V	0.3 W	-	
300-667 MHz	1.2-1.6 V	0.3 W	-	
Quick Start power				
300-500 MHz	1.2-1.6 V	0.2 W	-	Quick Start mode is entered by asserting STPCLK#. Typical Quick Start power is measured with LongRun power management enabled.
300-533 MHz	1.2-1.6 V	0.2 W	-	
300-600 MHz	1.2-1.6 V	0.2 W	-	
300-667 MHz	1.2-1.6 V	0.2 W	-	
Deep Sleep power				
300-500 MHz	1.2-1.6 V	0.1 W	-	Deep Sleep mode is entered by asserting SLEEP# and stopping CLKIN while in Quick Start. Deep Sleep typical power is measured with LongRun power management enabled.
300-533 MHz	1.2-1.6 V	0.1 W	-	
300-600 MHz	1.2-1.6 V	0.1 W	-	
300-667 MHz	1.2-1.6 V	0.1 W	-	
Maximum Deep Sleep power				
500 MHz	1.2 V	-	0.18 W	Deep Sleep mode is entered by asserting SLEEP# and stopping CLKIN while in Quick Start. Deep Sleep maximum power is specified at CVDD = 1.2V at a 45°C junction temperature.
533 MHz	1.2 V	-	0.18 W	
600 MHz	1.2 V	-	0.18 W	
667 MHz	1.2 V	-	0.18 W	

1. All power supplies at their nominal values. All power values are the total of core power and I/O power.

TABLE 31 TM5400/TM5600 Peak Current Specifications

Operating Frequency	Supply	Maximum Voltage	Peak Current	Notes
500 MHz	CVDD	1.68 V	3.7 A	All supplies at their maximum values.
	PLLVDD	1.68 V	20 mA	
	IOVDD25	2.625 V	300 mA	
	IOVDD	3.465 V	300 mA	
533 MHz	CVDD	1.68 V	3.8 A	All supplies at their maximum values.
	PLLVDD	1.68 V	20 mA	
	IOVDD25	2.625 V	300 mA	
	IOVDD	3.465 V	300 mA	
600 MHz	CVDD	1.68 V	4.2 A	All supplies at their maximum values.
	PLLVDD	1.68 V	20 mA	
	IOVDD25	2.625 V	300 mA	
	IOVDD	3.465 V	300 mA	
667 MHz	CVDD	1.68 V	4.7 A	All supplies at their maximum values.
	PLLVDD	1.68 V	20 mA	
	IOVDD25	2.625 V	300 mA	
	IOVDD	3.465 V	300 mA	

3.4 DC Specifications for I/O Signals

TABLE 32 DC Specs for All Signals Except PCI and DDR SDRAM Interfaces

Symbol	Description	Condition	Minimum	Maximum	Notes
V_{oh}	Output high voltage	I_{out} = -1 mA	2.4 V	-	
V_{ol}	Output low voltage	I_{out} = 1 mA	-	0.4 V	
V_{ih}	Input high voltage (excluding 2.5V inputs)		2.0 V	IOVDD	The 2.5V input pins are: CLKIN, IGNNE#, INTR, INIT#, NMI, SMI#, and STPCLK#. The 2.5V input pins are 3.3V tolerant.
	Input high voltage for 2.5V inputs		1.7 V	IOVDD	
V_{il}	Input low voltage		-0.3 V	0.7 V	
I_{ih}	Input high leakage current	V_{in} = IOVDD	-	10 uA	Pins loaded at 2.4 pF
I_{il}	Input low leakage current	V_{in} = 0 V	-	-100 uA	Pins loaded at 2.4 pF
I_{ihz}	Hi-Z high leakage current	V_{in} = IOVDD	-	10 uA	Pins loaded at 2.4 pF
I_{ilz}	Hi-Z low leakage current	V_{in} = 0 V	-	-10 uA	Pins loaded at 2.4 pF
C_{in}	Input pin capacitance		-	10 pF	

TABLE 33 DC Specifications for DDR SDRAM Interface

Symbol	Description	Condition	Minimum	Maximum
V_{oh}	Output high voltage	I_{out} = -5.0 mA	1.85 V	-
V_{ol}	Output low voltage	I_{out} = 7.5 mA	-	0.35 V
V_{ih} [1]	Input high voltage		C_VREF + 0.18V	IOVDD25 + 0.3V
V_{il}	Input low voltage		-0.3 V	C_VREF - 0.18V
I_{ih}	Input high leakage current	V_{in} = IOVDD25	-	10 uA
I_{il}	Input low leakage current	V_{in} = 0 V	-	-100 uA
C_{in}	Input pin capacitance		-	10 pF

1. The DDR SDRAM interface inputs are not 3.3V tolerant.

TABLE 34 DC Specifications for PCI Interface

Symbol	Description	Condition	Minimum	Maximum
V_{oh}	Output high voltage	I_{out} = -0.5 mA	0.9 x IOVDD	-
V_{ol}	Output low voltage	I_{out} = 1.5 mA	-	0.1 x IOVDD
V_{ih}	Input high voltage (excluding P_PCLK)		0.5 x IOVDD	IOVDD + 0.5V
	Input high voltage (P_PCLK only)		2.0 V	IOVDD + 0.5V
V_{il}	Input low voltage (excluding P_PCLK)		-0.5 V	0.3 x IOVDD
	Input low voltage (P_PCLK only)		-0.5 V	0.8 V
I_{ih}	Input high leakage current	V_{in} = IOVDD	-	10 µA
I_{il}	Input low leakage current	V_{in} = 0 V	-	- 100 µA
C_{in}	Input pin capacitance		-	10 pF

TABLE 35 Thermal Diode Specifications

Symbol	Description	Minimum	Typical	Maximum
V100 [1]	Forward biased diode drop forcing 100 uA	-	0.68 V	-
V10 [1]	Forward biased diode drop forcing 10 uA	-	0.62 V	-

1. V100 and V10 typical values are measured at 25°C while DIODE_CATHODE is biased at 0.7 V.

3.5 Timing Specifications for I/O Signals

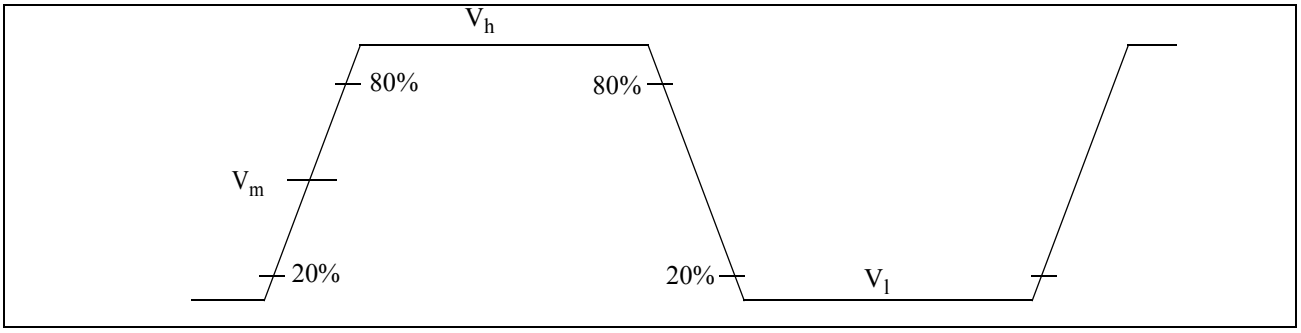
3.5.1 General AC Testing Conditions

Table 36 and Figure 5 specify the general AC test and measurement conditions. These conditions apply unless specified otherwise.

TABLE 36 General AC Testing Conditions

Parameter	Description	Value
V_l	3.3V input low drive level	0.4 V
	2.5V input low drive level	0.4 V
	DDR interface input low drive level	C_VREF - 0.35 V
V_h	3.3V input high drive level	2.4 V
	2.5V input high drive level	2.0 V
	DDR interface input high drive level	C_VREF + 0.35 V
V_m	3.3 V I/O timing specification measurement level	1.4 V
	2.5 V I/O timing specification measurement level	1.2 V
t_{edge}	Input signal edge rate measured between 20% and 80% of drive levels	1 V/ns

FIGURE 5 General AC Test and Measurement Conditions



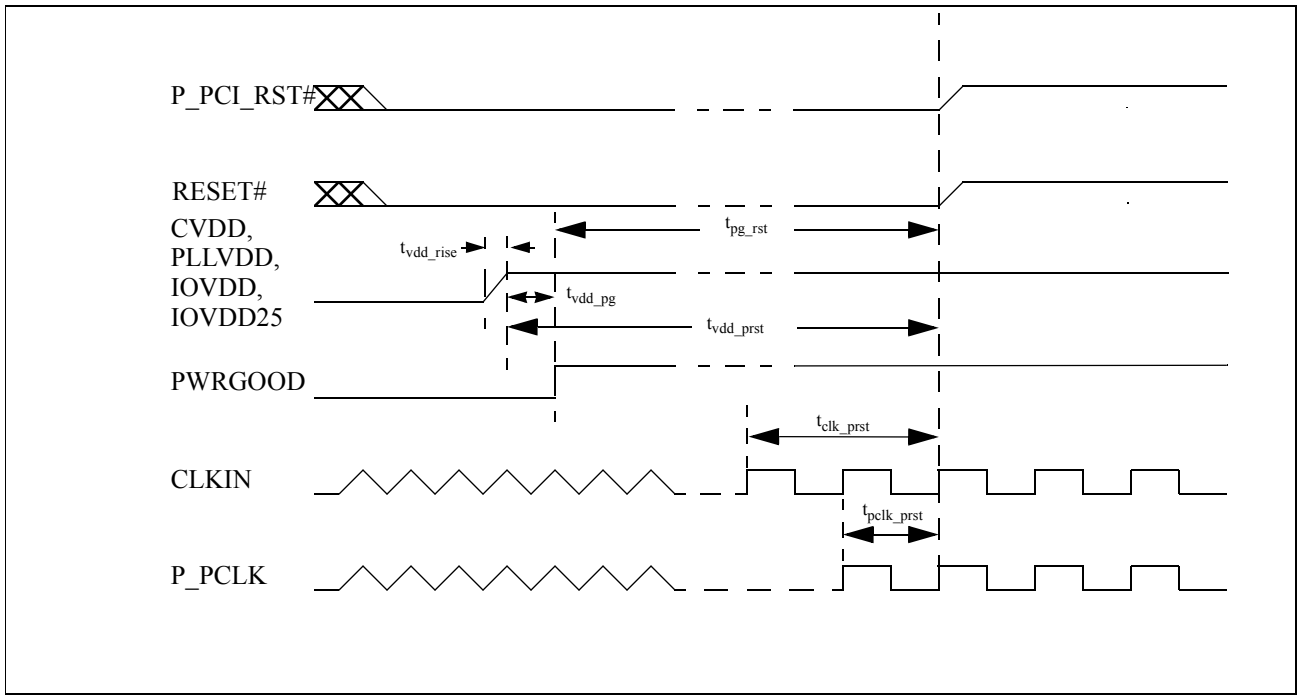
3.5.2 Power On Specifications

Table 37 and Figure 6 document the timing specifications for powering on the TM5400/ TM5600.

TABLE 37 Power On Specifications

Parameter	Description	Minimum	Maximum	Notes
t_{vdd_rise}	Supply rise time	-	250 ms	All supplies must rise from zero to recommended operating levels within the same 250 ms window.
t_{vdd_pg}	PWRGOOD asserted after supplies reach 95% of final value	0 s	-	P_PCI_RST# and RESET# should be active prior to PWRGOOD asserted.
t_{vdd_prst}	Supplies stable prior to P_PCI_RST# deasserted	1 ms	-	
t_{pclk_prst}	P_PCLK stable prior to P_PCI_RST# deasserted	100 µs	-	
t_{clk_prst}	CLKIN stable prior to P_PCI_RST# deasserted	1 ms	-	
t_{prst_rst}	P_PCI_RST# deasserted to RESET# deasserted	0 s	-	
t_{pg_rst}	PWRGOOD asserted to RESET#, P_PCI_RST# deasserted	1 ms	-	
t_{pg_low}	PWRGOOD inactive pulse width	10 CLKINs	-	

FIGURE 6 Power On Timing



3.5.3 Input Clocks

Table 38 and Figure 7 document the timing specifications for the input clocks.

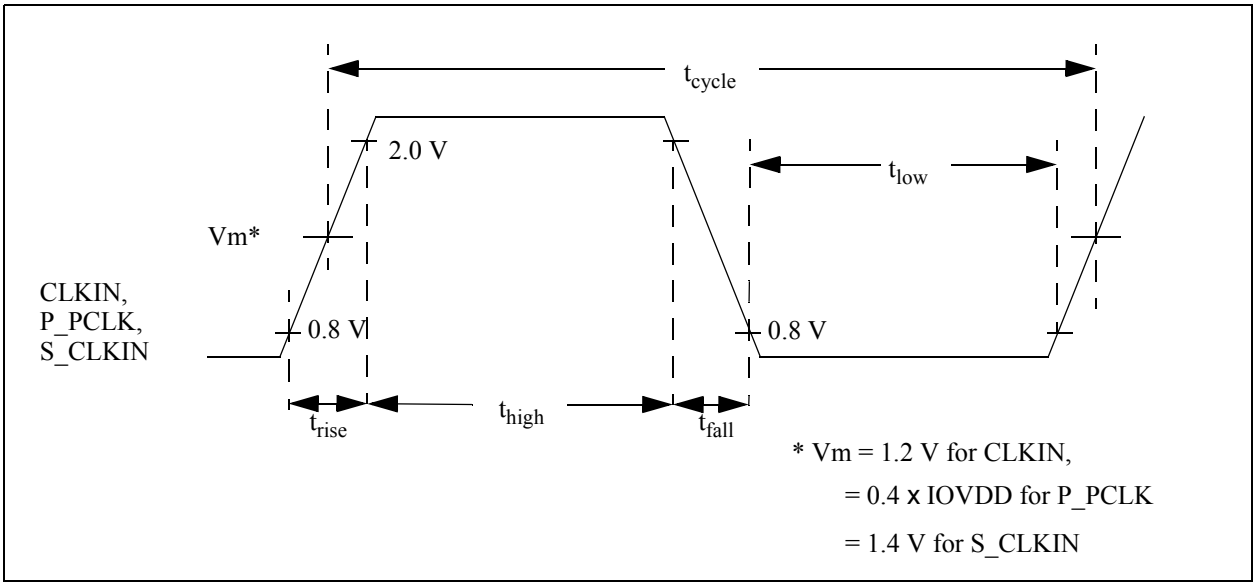
TABLE 38 Timing Specifications for Input Clocks

Parameter	Minimum	Maximum	Notes
f_{clk} (Clock frequency)			
CLKIN	60.0 MHz	66.66 MHz	Clocks may be stopped. Not 100% tested. Guaranteed by design/ characterization.
P_PCLK	30.0 MHz	33.33 MHz	
S_CLKIN	-	133.33 MHz	
t_{cycle} (Clock period)			
CLKIN	15.0 ns	16.67 ns	
P_PCLK	30 ns	-	
S_CLKIN	7.5 ns	-	
t_{high} (Clock high time)			
CLKIN	5.2 ns	-	Not 100% tested. Guaranteed by design/ characterization.
P_PCLK	11 ns	-	
S_CLKIN	3.375 ns	-	
t_{low} (Clock low time)			
CLKIN	5.0 ns	-	Not 100% tested. Guaranteed by design/ characterization.
P_PCLK	11 ns	-	
S_CLKIN	3.375 ns	-	
t_{jitter} (Clock jitter)			
CLKIN	-	250 ps	Spread spectrum clock generation (SSCG) is supported under the following conditions: • 66.67 MHz nominal input frequency • +0% / -5.0% maximum upspread / downspread • 30 kHz maximum modulation frequency • 250 ps max. clock jitter
P_PCLK	-	500 ps	
$t_{rise/fall}$ (Clock rise and fall time)			
CLKIN	0.4 ns	1.6 ns	
P_PCLK	1.0 ns	4.0 ns	

TABLE 38 Timing Specifications for Input Clocks (Continued)

Parameter	Minimum	Maximum	Notes
t_{offset} (CLKIN to P_PCLK offset)	1.5 ns	4.0 ns	
t_{pll_lock} (PLL relock time)	-	20 µs	

FIGURE 7 Timing Specifications for Input Clocks



3.5.4 DDR SDRAM Interface

Table 39 and Table 40, along with Figure 8 and Figure 9 document the timing specifications for the DDR SDRAM interface.

TABLE 39 Timing Specifications for DDR SDRAM Interface

Parameter	Description	Minimum	Maximum	Notes
f_{clk}	C_CLK frequency	-	133 MHz	
t_{cycle}	C_CLK period	7.5 ns	-	1
t_{low}, t_{high}	C_CLK low time, high time	0.45 bus clks	0.55 bus clks	1
t_{jitter}	C_CLK jitter	-	150 ps	1
V_x	Differential cross pt. voltage	1.1 V	1.4 V	1
t_{valid}	Output valid delay: C_DQS CMD signals	 0.75 bus clks	 see Table 40	2,3,4
t_{ohold}	Output hold time CMD signals	see Table 40	-	2,3,4
t_{valid_dqs}	C_DQ, C_DQMB valid from C_DQS (writes)	-	3.05 ns	
t_{ohold_dqs}	C_DQ, C_DQMB hold from C_DQS (writes)	0.76 ns	-	
t_{dqs_skew}	C_DQS to C_DQ, C_DQMB skew	-0.76 ns	+0.76 ns	
t_{dqs_low}, t_{dqs_high}	C_DQS input low time, C_DQS input high time	0.45 bus clks	0.55 bus clks	
$t_{dqs\_preamble}$	C_DQS preamble valid time	0.9 bus clks	1.1 bus clks	
t_{off}	Active to float delay C_DQ C_DQS	 0 ns -0.5 ns	 2.5 ns +0.5 ns	2
n_{ras_cas}	C_RAS# to C_CAS# latency	1 bus clock	16 bus clocks	5
n_{cas_read}	C_CAS# to read latency	1 bus clock	16 bus clocks	5
n_{read_pchg}	Read precharge delay	1 bus clock	16 bus clocks	5
n_{wr_pchg}	Write precharge delay	1 bus clock	16 bus clocks	5
n_{row_pchg}	Row precharge time	1 bus clock	16 bus clocks	5,6
n_{idmrs}	Idle cycles after MRS	2 bus clocks	17 bus clocks	5,7
n_{ras_ras}	Row cycle time	2 bus clocks	17 bus clocks	5,8
n_{burst}	Burst length	4 transfers	4 transfers	9
$n_{refresh}$	Refresh rate	128 bus clocks	16k bus clocks	5

Notes for Table 39:

1. Clock specifications apply to C_CLKA, C_CLKA#, C_CLKB, C_CLKB#. C_CLKA and C_CLKA# are 180 degrees out of phase. C_CLKB and C_CLKB# are 180 degrees out of phase. C_CLKA and C_CLKB are copies of each other.
2. These parameters measured relative to C_CLK/C_CLK# differential cross point voltage.
3. CMD signals are: C_A[12:0], C_BA[1:0], C_CAS#, C_CKE[1:0], C_CS#[3:0], C_RAS#, C_WE#.
4. Assumes 80 pF maximum load on each CMD signal and 10 pF maximum load on each of C_DQ[63:0].
5. These parameters are programmable within the TM5400/TM5600 processor.
6. Row precharge time is the number of bus clocks between the power on precharge and the next time RAS can be asserted.
7. MRS stands for Mode Register Set operation.
8. Row cycle time is the number of bus clocks between refresh and the next time RAS can be asserted for other SDRAM operations. This also is the number of cycles the DDR SDRAM controller waits before starting any SDRAM access after it exits clock off mode.
9. The DDR SDRAM controller always performs burst operations.

Table 40 provides the DDR SDRAM interface output hold time (t_{ohold}) minimum timing and output valid delay (t_{valid}) maximum timing specifications for each TM5400/TM5600 SKU and LongRun step. The table covers three DDR memory speeds. Refer to *TM5400/TM5600 Development and Manufacturing Guide* for additional information on memory configuration.

TABLE 40 t_{ohold} and t_{valid} Timing Specifications for DDR SDRAM Interface

SKU	LongRun Settings		DDR Interface CLK Divisor / Frequency (MHz) / t_{ohold} min (ns) / t_{valid} max (ns)											
			TM_DDR266CL25				TM_DDR250CL25				TM_DDR200CL25			
	MHz	V	Div	Mclk	t_{ohold}	t_{valid}	Div	Mclk	t_{ohold}	t_{valid}	Div	Mclk	t_{ohold}	t_{valid}
500 1.6V	500	1.6	÷ 4	125	TBD	TBD	÷ 4	125	TBD	TBD	÷ 5	100	TBD	TBD
	400	1.4	÷ 3	133	TBD	TBD	÷ 4	100	TBD	TBD	÷ 4	100	TBD	TBD
	300	1.2	÷ 3	100	TBD	TBD	÷ 3	100	TBD	TBD	÷ 3	100	TBD	TBD
533 1.6V	533	1.6	÷ 4	133	TBD	TBD	÷ 5	107	TBD	TBD	÷ 6	89	TBD	TBD
	467	1.5	÷ 4	117	TBD	TBD	÷ 4	117	TBD	TBD	÷ 5	93	TBD	TBD
	400	1.35	÷ 3	133	TBD	TBD	÷ 4	100	TBD	TBD	÷ 4	100	TBD	TBD
	300	1.2	÷ 3	100	TBD	TBD	÷ 3	100	TBD	TBD	÷ 3	100	TBD	TBD
600 1.6V	600	1.6	÷ 5	120	TBD	TBD	÷ 5	120	TBD	TBD	÷ 6	100	TBD	TBD
	500	1.4	÷ 4	125	TBD	TBD	÷ 4	125	TBD	TBD	÷ 5	100	TBD	TBD
	400	1.225	÷ 4	100	TBD	TBD	÷ 4	100	TBD	TBD	÷ 4	100	TBD	TBD
	300	1.2	÷ 3	100	TBD	TBD	÷ 3	100	TBD	TBD	÷ 3	100	TBD	TBD
667 1.6V	667	1.6	÷ 5	133	TBD	TBD	÷ 6	111	TBD	TBD	÷ 7	95	TBD	TBD
	600	1.5	÷ 5	120	TBD	TBD	÷ 5	120	TBD	TBD	÷ 6	100	TBD	TBD
	533	1.35	÷ 4	133	TBD	TBD	÷ 5	107	TBD	TBD	÷ 6	89	TBD	TBD
	400	1.225	÷ 4	100	TBD	TBD	÷ 4	100	TBD	TBD	÷ 4	100	TBD	TBD
	300	1.2	÷ 3	100	TBD	TBD	÷ 3	100	TBD	TBD	÷ 3	100	TBD	TBD

FIGURE 8 Timing Specifications for DDR SDRAM Interface - Read Cycle

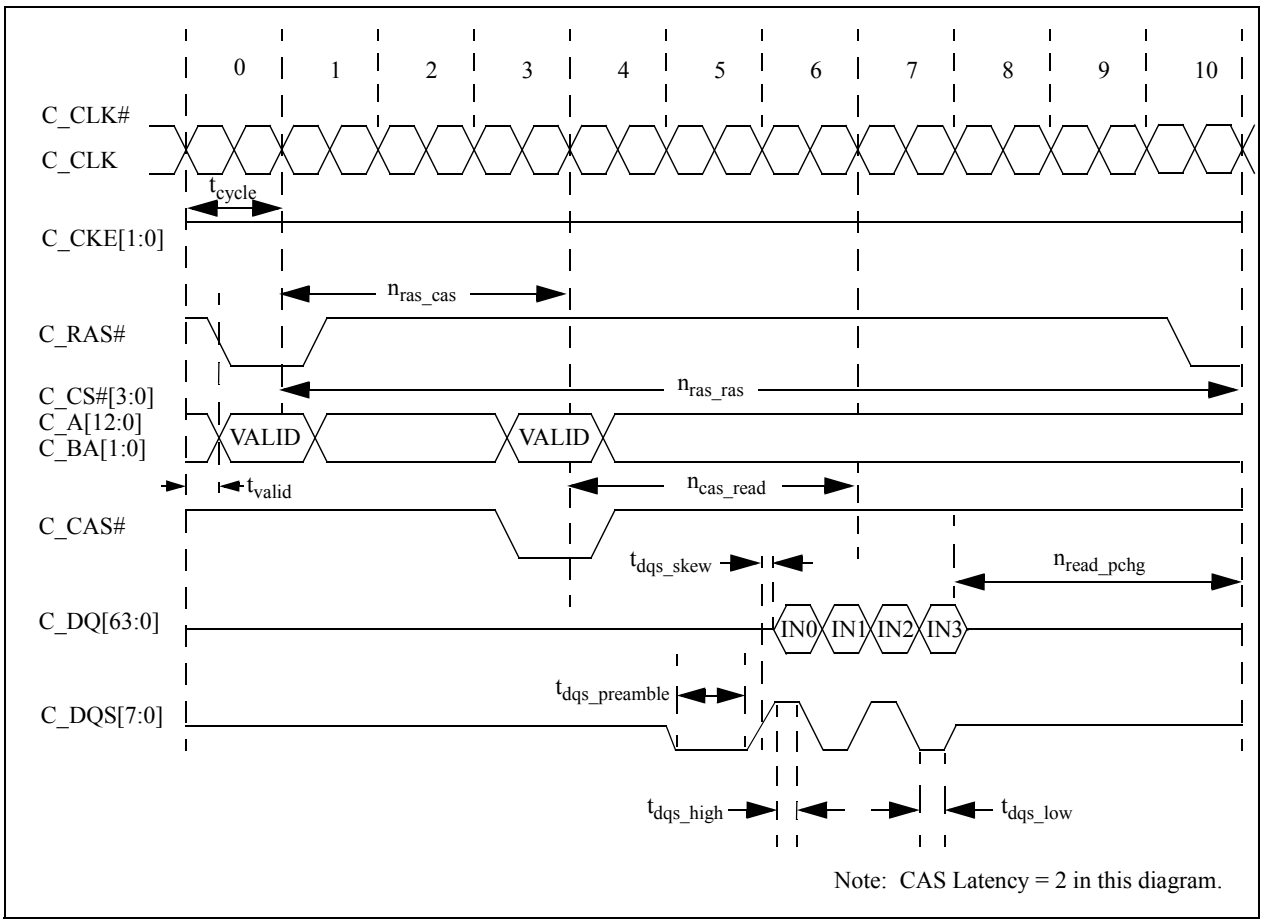
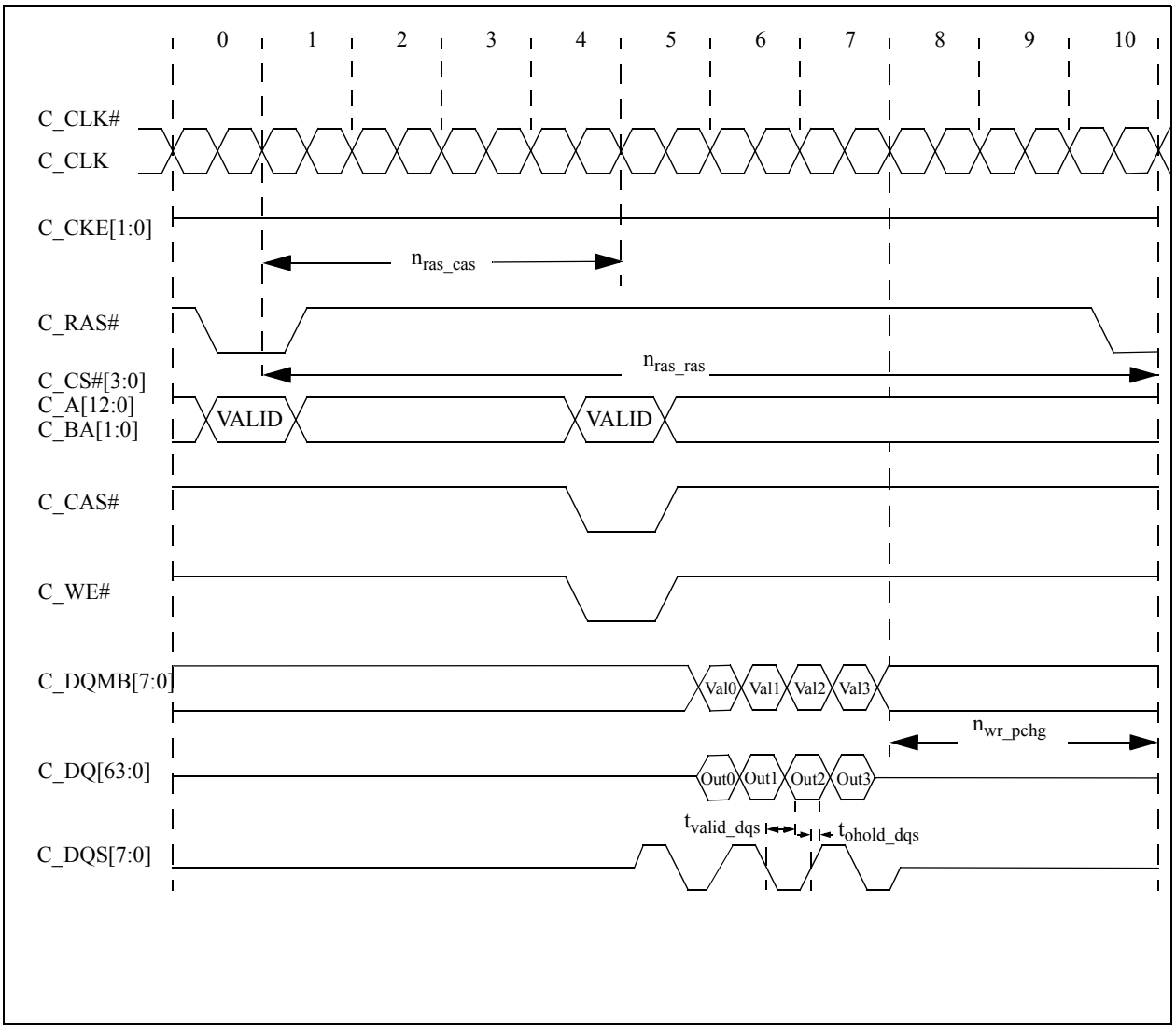


FIGURE 9 Timing Specifications for DDR SDRAM Interface - Write Cycle



3.5.5 SDR SDRAM Interface

Table 41 and Table 42, along withFigure 10, Figure 11, and Figure 12, document the timing specifications for the SDR SDRAM interface.

TABLE 41 Timing Specifications for SDR SDRAM Interface

Parameter	Description	Minimum	Maximum	Notes
f_{clk}	S_CLKIN, S_CLKOUT, S_CLK frequency	-	133 MHz	1
t_{setup}	Input setup time	1.7 ns	-	2, 3
t_{ihold}	Input hold time	1.9 ns	-	2, 3
t_{valid}	Output valid delay	-	see Table 42	2, 4, 5
t_{ohold}	Output hold time	see Table 42	-	2, 4, 5, 6
n_{ras_cas}	S_RAS# to S_CAS# latency	1 bus clock	16 bus clocks	6
n_{cas_read}	S_CAS# to read latency	1 bus clock	16 bus clocks	6
n_{read_pchg}	Read precharge delay	1 bus clock	16 bus clocks	6
n_{wr_pchg}	Write precharge delay	1 bus clock	16 bus clocks	6
n_{row_pchg}	Row precharge time	1 bus clock	16 bus clocks	6, 7
n_{idmrs}	Idle cycles after MRS	2 bus clocks	17 bus clocks	6, 8
n_{ras_ras}	Row cycle time	2 bus clocks	17 bus clocks	6, 9
n_{burst}	Burst length	4 transfers	4 transfers	10
$n_{refresh}$	Refresh rate	128 bus clocks	16K bus clocks	6

Notes for Table 41:

1. S_CLK[3:0] are copies of S_CLKOUT.
2. These parameters measured relative to S_CLKIN rising edge at 1.4 volt level.
3. Input signals are: S_DQ[63:0].
4. Output signals are:
   Data= S_DQ[63:0], S_DQMB[7:0]
   Address= S_A[12:0], S_BA[1:0], S_CAS#, S_RAS#, S_WE#
   Enables = S_CKE[1:0], S_CS#[3:0]
5. Assumes 50 pF load for output pins. For every 10 pF above a 50 pF load, add 170 pS for the data and enable pins, and 90 pS for the address pins. For every 10 pF below a 50 pF load, subtract 170 pS for the data and enable pins, and 90 pS for the address pins.
6. These parameters are programmable within the TM5400/TM5600 processor.
7. Row precharge time is the number of bus clocks between the power on precharge and the next time RAS can be asserted.
8. MRS stands for Mode Register Set operation.
9. Row cycle time is the number of bus clocks between refresh and the next time RAS can be asserted for other SDRAM operations. This also is the number of cycles the SDR SDRAM controller waits before starting any SDRAM access after it exits clock off mode.

10. The SDR SDRAM controller always performs burst operations.

FIGURE 10 SDR SDRAM Input Setup/Hold and Output Valid Delay/Hold Timing

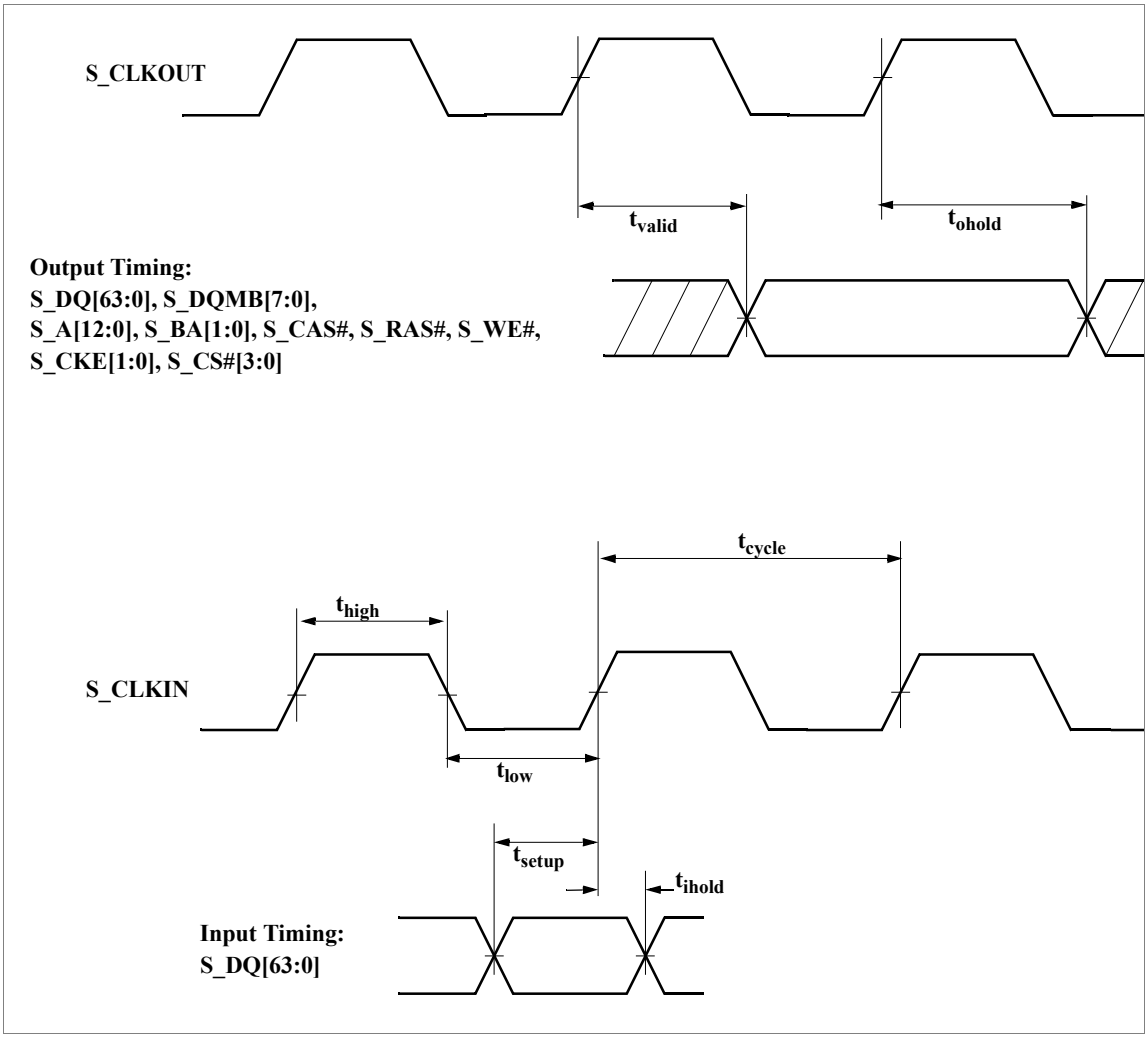


Table 42 provides the SDR SDRAM interface output hold time (t_{ohold}) minimum timing and output valid delay (t_{valid}) maximum timing specifications for each TM5400/TM5600 SKU and LongRun step. The table covers three SDR memory speeds. Refer to *TM5400/TM5600 Development and Manufacturing Guide* for additional information on memory configuration.

TABLE 42 t_{ohold} and t_{valid} Timing Specifications for SDR SDRAM Interface

SKU	LongRun Settings		SDR Interface CLK Divisor / Frequency (MHz) / t_{ohold} min (ns) / t_{valid} max (ns)											
			TM_SDR133CL3				TM_SDR125CL3				TM_SDR100CL3			
	MHz	V	Div	Mclk	t_{ohold}	t_{valid}	Div	Mclk	t_{ohold}	t_{valid}	Div	Mclk	t_{ohold}	t_{valid}
500 1.6V	500	1.6	÷ 4	125	1.4	4.0	÷ 4	125	1.4	4.0	÷ 5	100	1.4	4.0
	400	1.4	÷ 3	133	2.0	4.0	÷ 4	100	2.0	4.0	÷ 4	100	2.0	4.0
	300	1.2	÷ 3	100	2.4	5.4	÷ 3	100	2.4	5.4	÷ 3	100	2.4	5.4
533 1.6V	533	1.6	÷ 4	133	1.25	3.9	÷ 5	107	2.2	3.8	÷ 6	89	2.2	3.8
	467	1.5	÷ 4	117	1.6	3.7	÷ 4	117	1.6	3.7	÷ 5	93	1.6	3.7
	400	1.35	÷ 3	133	2.0	4.0	÷ 4	100	2.0	4.0	÷ 4	100	2.0	4.0
	300	1.2	÷ 3	100	2.4	5.4	÷ 3	100	2.4	5.4	÷ 3	100	2.4	5.4
600 1.6V	600	1.6	÷ 5	120	1.9	4.5	÷ 5	120	1.9	4.5	÷ 6	100	1.9	4.5
	500	1.4	÷ 4	125	1.5	3.5	÷ 4	125	1.5	3.5	÷ 5	100	1.5	3.5
	400	1.225	÷ 3	133	1.6	4.6	÷ 4	100	1.6	4.6	÷ 4	100	1.6	4.6
	300	1.2	÷ 3	100	2.5	5.4	÷ 3	100	2.5	5.4	÷ 3	100	2.5	5.4
667 1.6V	667	1.6	÷ 5	133	1.6	4.2	÷ 6	111	1.6	4.2	÷ 7	95	1.6	4.2
	600	1.5	÷ 5	120	2.0	4.0	÷ 5	120	2.0	4.0	÷ 6	100	2.0	4.0
	533	1.35	÷ 4	133	1.35	3.4	÷ 5	107	2.3	4.3	÷ 6	89	2.3	4.3
	400	1.225	÷ 3	133	1.65	4.6	÷ 4	100	1.65	4.6	÷ 4	100	1.65	4.6
	300	1.2	÷ 3	100	2.5	5.4	÷ 3	100	2.5	5.4	÷ 3	100	2.5	5.4

FIGURE 11 Timing Specifications for SDR SDRAM Interface - Read Cycle

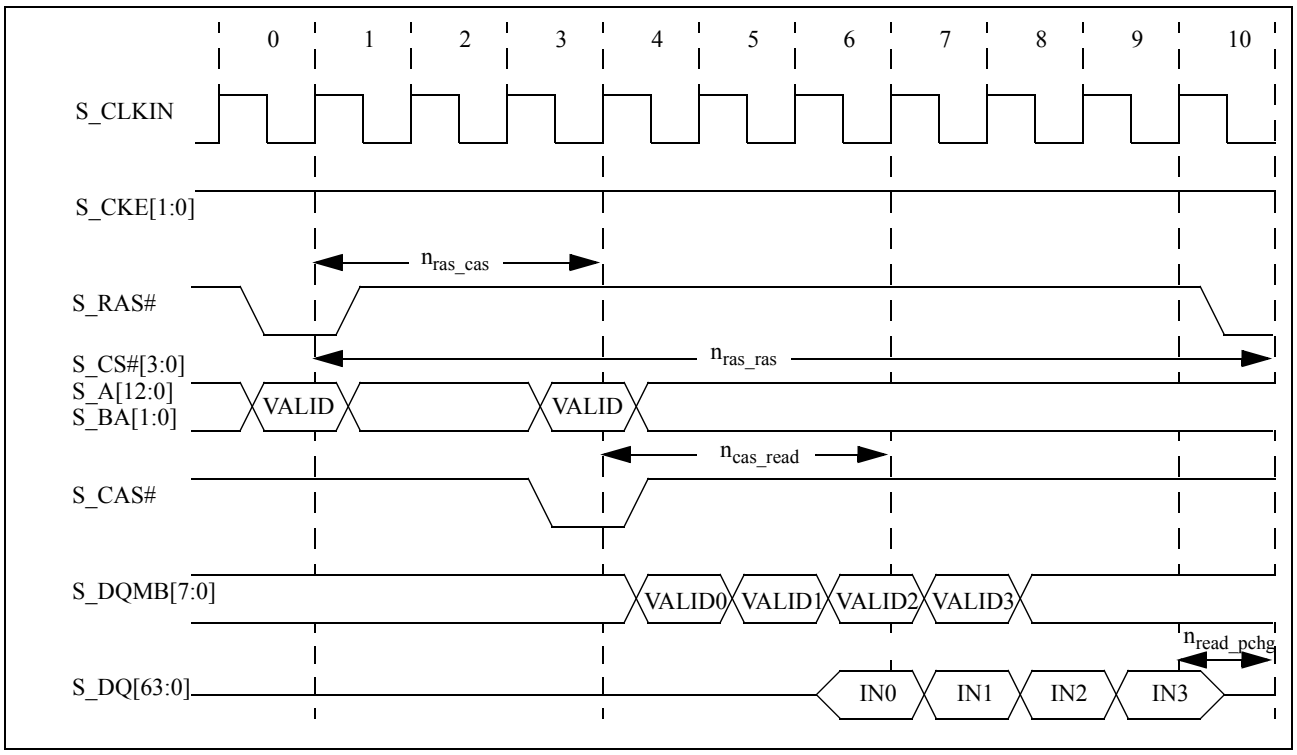
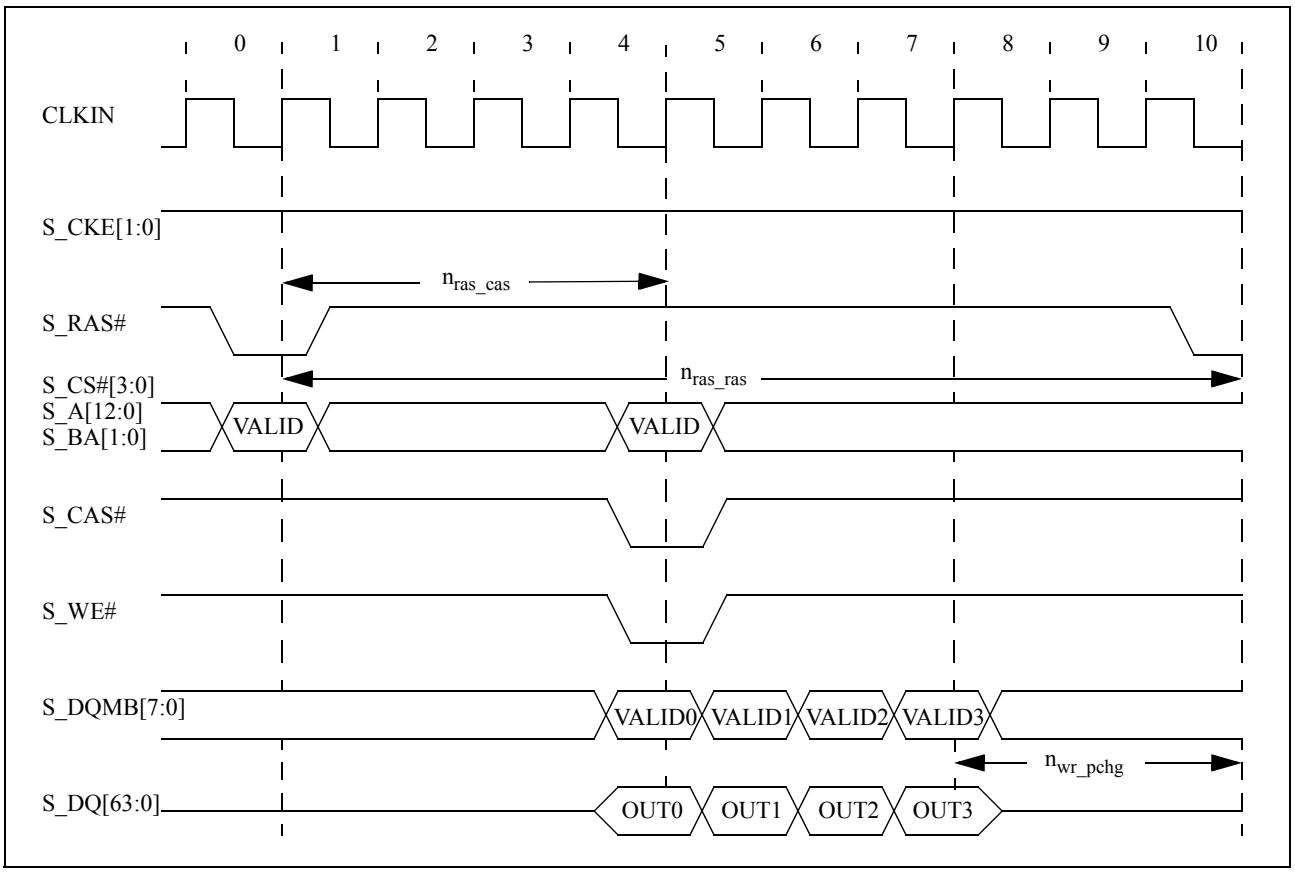


FIGURE 12 Timing Specifications for SDR SDRAM Interface - Write Cycle



3.5.6 PCI Interface

Table 43 documents the timing specifications for the PCI interface. The TM5400/TM5600 PCI interface is compliant with revision 2.1 of the PCI Local Bus Specification. Refer to the PCI specification for additional information.

TABLE 43 Timing Specifications for PCI Interface

Parameter	Description	Minimum	Maximum	Notes
f_{clk}	P_PCLK frequency	30.0 MHz	33.33 MHz	
t_{setup}	Input setup time			
	P_REQ#[5:0]	12 ns	-	1, 2
	All other inputs	7 ns	-	
t_{ihold}	Input hold time	0 ns	-	1, 2
t_{valid}	Output valid delay			
	P_GNT#[5:0]	2 ns	12 ns	1, 3
	All other outputs	2 ns	11 ns	
t_{off}	Active to float delay	-	28 ns	
t_{rst_off}	P_PCI_RST# asserted to output float delay	-	40 ns	

Notes for Table 43:

1. These parameters measured relative to P_PCLK rising edge at 0.4*IOVDD level.
2. Input signals are: P_AD[31:0], P_C/BE#[3:0], P_CLKRUN#, P_DEVSEL#, P_FRAME#, P_HOLD#, P_IRDY#, P_LOCK#, P_PAR, P_PCI_RST#, P_PERR#, P_REQ#[5:0], P_SERR#, P_STOP#, P_TRDY#.
3. Output signals are: P_AD[31:0], P_C/BE#[3:0], P_CLKRUN#, P_DEVSEL#, P_FRAME#, P_GNT#[5:0], P_HLDA#, P_IRDY#, P_LOCK#, P_PAR, P_PERR#, P_STOP#, P_TRDY#.

3.5.7 Southbridge Sidebands and Power Management Interface

IGNNE#, INIT#, INTR, NMI, PWRGOOD, SLEEP#, SMI# and STPCLK# are asynchronous input signals. Therefore, these inputs are not required to meet any setup and hold specifications.

3.5.8 Debug Interface

Table 44 and Figure 13 document the timing specifications for the debug serial interface.

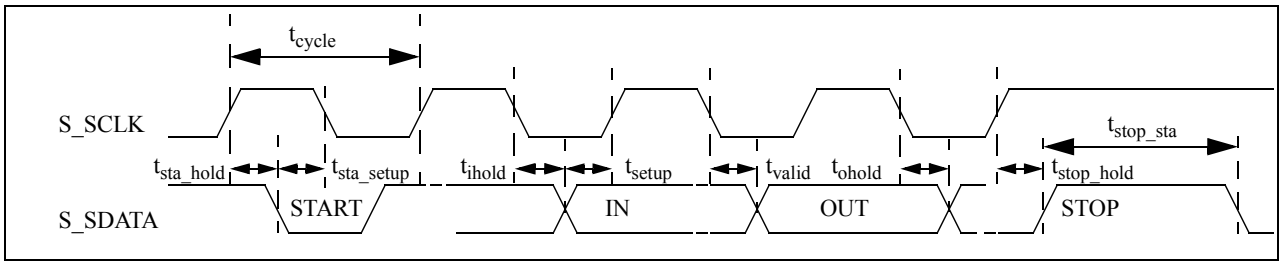
TABLE 44 Timing Specifications for Debug Interface

Parameter	Description	Minimum	Maximum	Notes
f_{clk}	S_SCLK frequency	0	400 KHz	1
t_{cycle}	S_SCLK period	2.5 µs	-	
t_{high}	S_SCLK high time	600 ns	-	1
t_{low}	S_SCLK low time	1.3 µs	-	1
t_{rise}	S_SCLK, S_SDATA rise time	-	1 µs	2
t_{fall}	S_SCLK, S_SDATA fall time	-	300 ns	2
t_{stop_sta}	Bus free to new transaction	1.3 µs	-	
t_{sta_setup}	Start condition setup time	600 ns	-	3, 4
t_{sta_hold}	Start condition hold time	600 ns	-	3, 5
t_{stop_hold}	Stop condition setup time	600 ns	-	4, 6
t_{setup}	S_SDATA input setup time	100 ns	-	4
t_{ihold}	S_SDATA input hold time	0 ns	-	5
t_{valid}	S_SDATA output valid delay	-	350 ns	5
t_{ohold}	S_SDATA output hold time	250 ns	-	5

Notes for Table 44:

1. Not 100% tested. Guaranteed by design/characterization.
2. Rise and fall times are measured from 20% to 80%.
3. Start condition occurs when S_SDATA transitions from high to low while S_SCLK is high.
4. These conditions measured relative to S_SCLK rising edge at 1.5 volt level. Assumed loading is 400 pF.
5. These conditions measured relative to S_SCLK falling edge at 1.5 volt level. Assumed loading is 400 pF.
6. Stop condition occurs when S_SDATA transitions from low to high while S_SCLK is high.

FIGURE 13 Timing Specifications for Debug Interface



3.5.9 Code Morphing Software Boot ROM Interface

Table 45 and Figure 14 document the timing specifications for the Code Morphing software boot ROM serial interface.

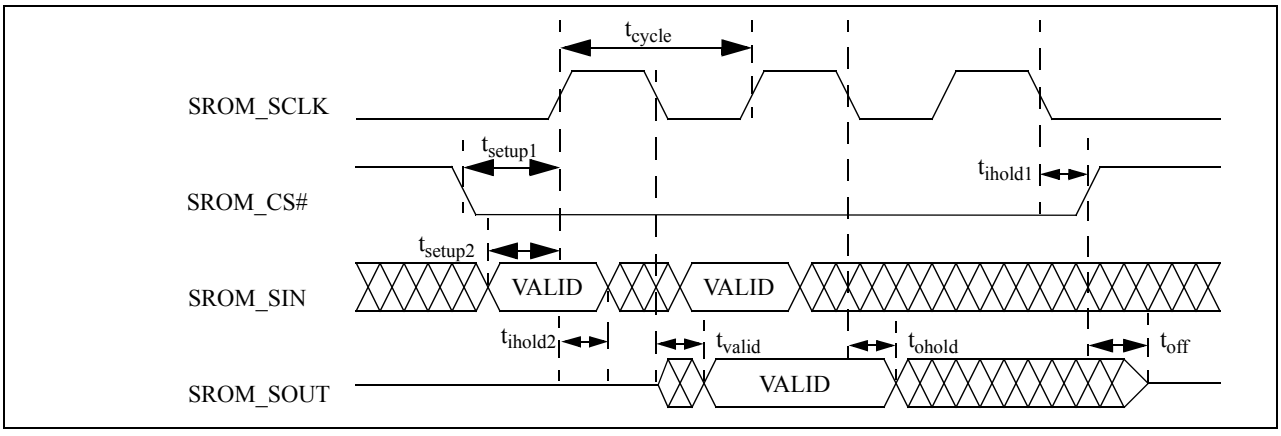
TABLE 45 Code Morphing Software Boot ROM Interface Timing Specifications

Parameter	Description	Minimum	Maximum	Notes
f_{clk}	SROM_SCLK frequency	-	11 MHz	
t_{cycle}	SROM_SCLK period	90 ns	-	
t_{high}	SROM_SCLK high time	40 ns	-	
t_{low}	SROM_SCLK low time	40 ns	-	
t_{setup1}	SROM_CS# input setup time	350 ns	-	1
t_{ihold1}	SROM_CS# input hold time	350 ns	-	2
t_{cs_high}	SROM_CS# high time	100 ns	-	
t_{setup2}	SROM_SIN input setup time	20 ns	-	1
t_{ihold2}	SROM_SIN input hold time	0 ns	-	1
t_{valid}	SROM_SOUT output valid delay	-	85 ns	2
t_{ohold}	SROM_SOUT output hold time	35 ns	-	2
t_{off}	SROM_SOUT active to float delay	-	100 ns	

Notes for Table 45:

1. These conditions measured relative to SROM_SCLK rising edge at 1.4 volt level.
2. These conditions measured relative to SROM_SCLK falling edge at 1.4 volt level.

FIGURE 14 Code Morphing Software Boot ROM Interface Timing Specifications



3.5.10 Configuration ROM Interface

Table 46 and Figure 15 document the timing specifications for the configuration ROM interface.

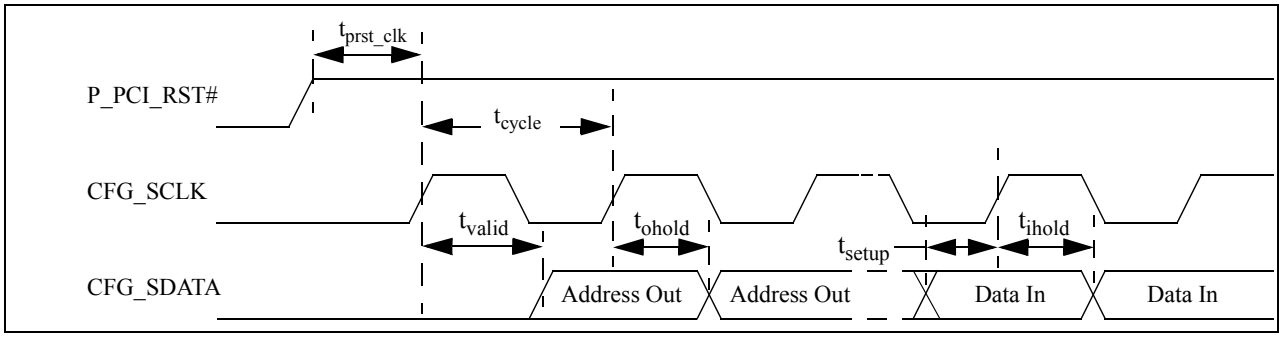
TABLE 46 Timing Specifications for Configuration ROM Interface

Parameter	Description	Minimum	Maximum	Notes
f_{clk}	CFG_SCLK frequency	-	2 MHz	
t_{cycle}	CFG_SCLK clock period	0.5 µs	2 µs	1
t_{high}	CFG_SCLK high time	250 ns	-	
t_{low}	CFG_SCLK low time	250 ns	-	
t_{prst_clk}	P_PCI_RST# to CFG_SCLK active high	100 ns	-	
t_{setup}	CFG_SDATA input setup time	600 µs	-	2
t_{ihold}	CFG_SDATA input hold time	0 s	-	2
t_{valid}	CFG_SDATA output valid delay	-	900 µs	2
t_{ohold}	CFG_SDATA output hold time	100 ns	-	2

Notes for Table 46:

1. CFG_SCLK period is CLKIN period × 72. For 66 MHz CLKIN, CFG_SCLK period is 1.08 µs.
2. These parameters measured relative to CFG_SCLK rising edge at 1.4 volt level.

FIGURE 15 Timing Specifications for Configuration ROM Interface



3.5.11 JTAG Interface

Table 47 and Figure 16 document the timing specifications for the JTAG interface. TRST# is an asynchronous pin. Therefore there is no setup or hold time specified for TRST# in Table 47.

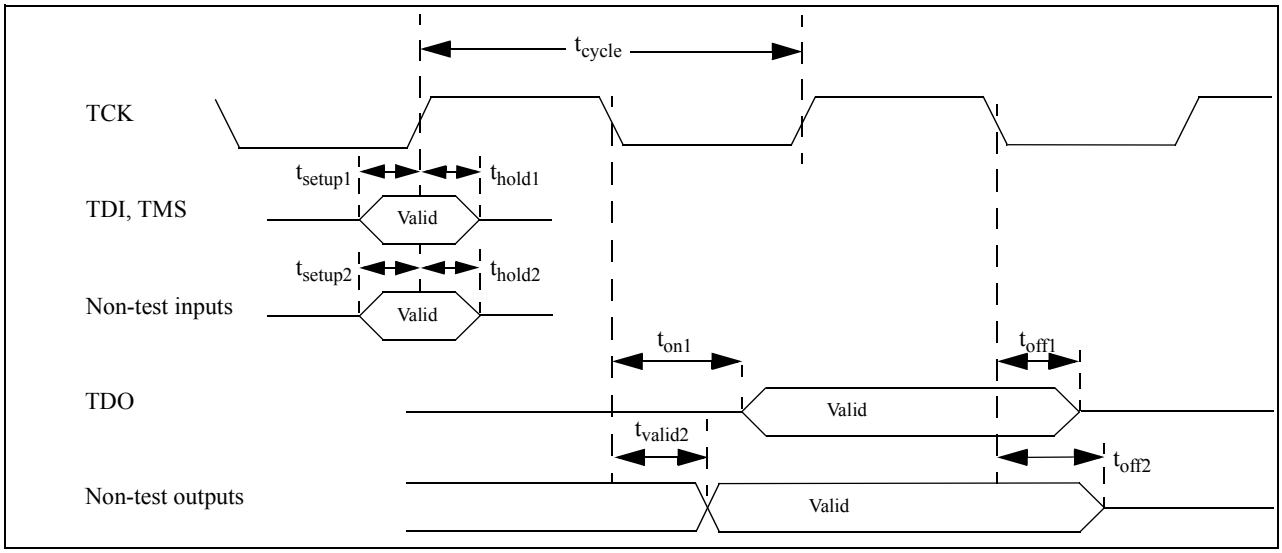
TABLE 47 Timing Specifications for JTAG Interface

Parameter	Description	Minimum	Maximum	Notes
f_{clk}	TCK frequency		50 MHz	
t_{cycle}	TCK clock period	20 ns	-	
t_{low}	TCK low time	8 ns	-	
t_{high}	TCK high time	8 ns	-	
t_{rise}	TCK rise time	-	2 ns	
t_{fall}	TCK fall time	-	2 ns	
t_{reset}	TRST# pulse width	200 ns	-	
t_{setup1}	TDI, TMS input setup time	10 ns	-	1
t_{hold1}	TDI, TMS input hold time	10 ns	-	1
t_{on1}	TDO float to active delay	5 ns	10 ns	2
t_{off1}	TDO active to float delay	-	10 ns	2
t_{setup2}	Non-test inputs setup time	10 ns	-	1
t_{hold2}	Non-test inputs hold time	-	10 ns	1
t_{valid2}	Non-test outputs valid delay	-	10 ns	2
t_{off2}	Non-test outputs active to float delay	-	20 ns	2

Notes for Table 47:

1. These parameters measured relative to TCK rising edge at 1.4 volt level.
2. These parameters measured relative to TCK falling edge at 1.4 volt level.

FIGURE 16 Timing Specifications for JTAG Interface



Chapter 4

Mechanical Specifications

4.1 Thermal Specifications

The maximum junction temperature for the TM5400/TM5600 is 85°C. The junction-to-package top (exposed silicon die) thermal resistance (θ_{jp}) is 0.075°C/W, and the junction-to-PCB thermal resistance (θ_{jb}) is 3.3°C/W. For detailed information on processor thermal characteristics and thermal solution design, please refer to the *TM5400/TM5600 Thermal Design Guide*.

4.1.1 Thermal Diode

TM5400/TM5600 Version 1.2

The TM5400/TM5600 v1.2 on-die thermal diode, when used in conjunction with a Maxim MAX1617MEE (standard part) temperature sensor, will provide a temperature accuracy of +/- 3°C from 0-to-100°C.

The system BIOS will provide an offset of 1°C for temperature correction when it recognizes a TM5400/TM5600 version 1.2 device.

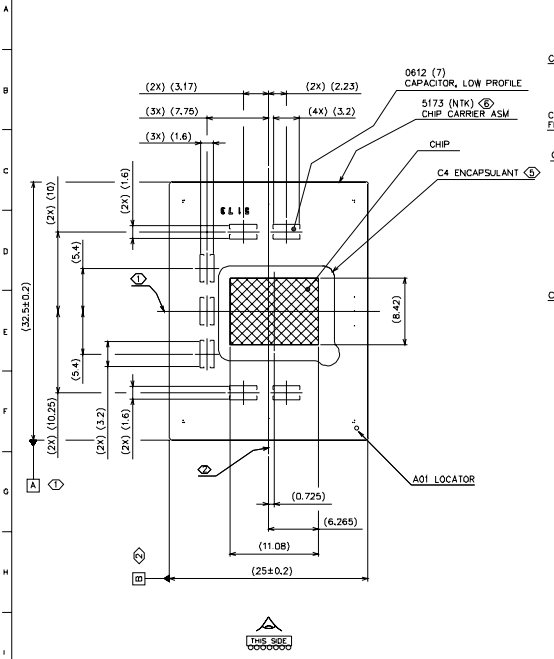
TM5400/TM5600 Versions 1.0 and 1.1

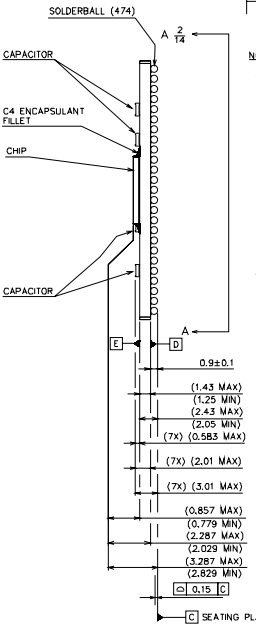
The TM5400/TM5600 v1.0 and v1.1on-die thermal diodes, when used in conjunction with a Maxim MAX1617TMEE (Transmeta-specific) temperature sensor, will provide a temperature accuracy of +/- 3°C from 0-to-100°C. The Transmeta-specific MAX1617TMEE must be used for TM5400/TM5600 version 1.0 and 1.1 devices - the standard MAX1617MEE will not provide any guaranteed level of accuracy.

The system BIOS will provide an offset of 6°C for temperature correction when it recognizes TM5400/TM5600 version 1.0 and 1.1 devices.

4.2 Package Dimensions

The TM5400/TM5600 processor is packaged in a 474-pin ceramic ball-grid array. The dimensions for this package are shown in the drawings on the following pages. For more information on the TM5400/TM5600 package, see the *Crusoe Processor Model TM5400/ TM5600 Package Specifications and Manufacturing Guide*.





REVISIONS/ENGINEERING CHANGE ORDER			
REV	ECO #	DESCRIPTION	DATE BY
A	–	updates	06/00 BF

NOTES:

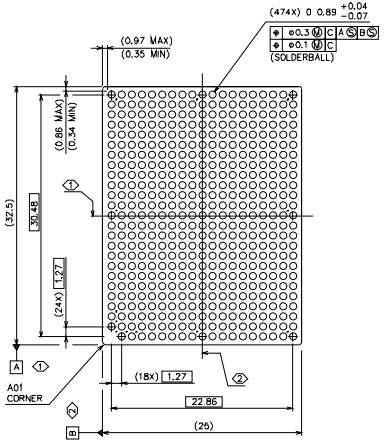
1. DATUM A IS THE CENTER PLANE OF FEATURE LABELED DATUM A.
2. DATUM B IS THE CENTER PLANE OF FEATURE LABELED DATUM B.
3. UNLESS OTHERWISE SPECIFIED PART IS SYMMETRICAL ABOUT CENTERLINES DEFINED BY DATUMS A & B.
4. WHERE NOT OTHERWISE DEFINED. CENTERLINES INDICATED ARE TO BE INTERPRETED AS A DATUM FRAME WORK ESTABLISHED BY DATUMS D, A & B RESPECTIVELY.
5. THIS LINE DEFINES THE APPROXIMATE BOUNDARY CONFIGURATION OF ENCAPSULANT AS DISPENSED. ENCAPSULANT IS NOT TO TOUCH SURFACE MOUNT CAPACITORS.
6. OPTIONAL CHIP CARRIER P/N IS 07P5766 (KYOCERA).

Transmeta Corporation

3940 FREEDOM CIRCLE SANTA CLARA, CLIFORNIA 95054

		TITLE: MODULE ASSEMBLY 25mm x 32.5mm	
TOLERANCES UNLESS NOTED		SCALE: NONE	PART NUMBER: 5173
LINEAR ±	0.5	THIRD ANGLE PROJECTION	SHEET: 1 OF 2
ANGLES ±	0° 30'		DESIGNER: GARY KIPP
RADII UNLESS NOTED			CHECKED BY: BF
EDGE/CORNER OUTSIDE MAX			APPROVED: BF
BREAKS INSIDE MAX		ACAD#: Transmeta\xsection1\xsection1_1.dwg	

REVISIONS/ENGINEERING CHANGE ORDER				
REV	ECO #	DESCRIPTION	DATE	BY
–	–	–	–	–



VIEW A–A $\frac{1}{B7}$

THIS SIDE

CONFIDENTIAL

Transmeta Corporation

3940 FREEDOM CIRCLE SANTA CLARA, CLIFORNIA 95054

		TITLE: MODULE ASSEMBLY 25mm x 32.5mm	
TOLERANCES UNLESS NOTED		SCALE: NONE	PART NUMBER: 5173
LINEAR ±	0.5		SHEET: 2 OF 2
ANGLES ±	0° 30'	THIRD ANGLE PROJECTION	DESIGNER: GARY KIPP
RADII UNLESS NOTED			CHECKED BY: BF
EDGE/CORNER	OUTSIDE MAX		APPROVED: BF
BREAKS	INSIDE MAX	ACAD#	Transmeta\vsection1\vsection1_2.dwg

4.3 Package Marking

Figure 17 shows the location of the TM5400/TM5600 package markings. The fields shown are described in detail in Table 48.

FIGURE 17 Package Marking Locations - Top View

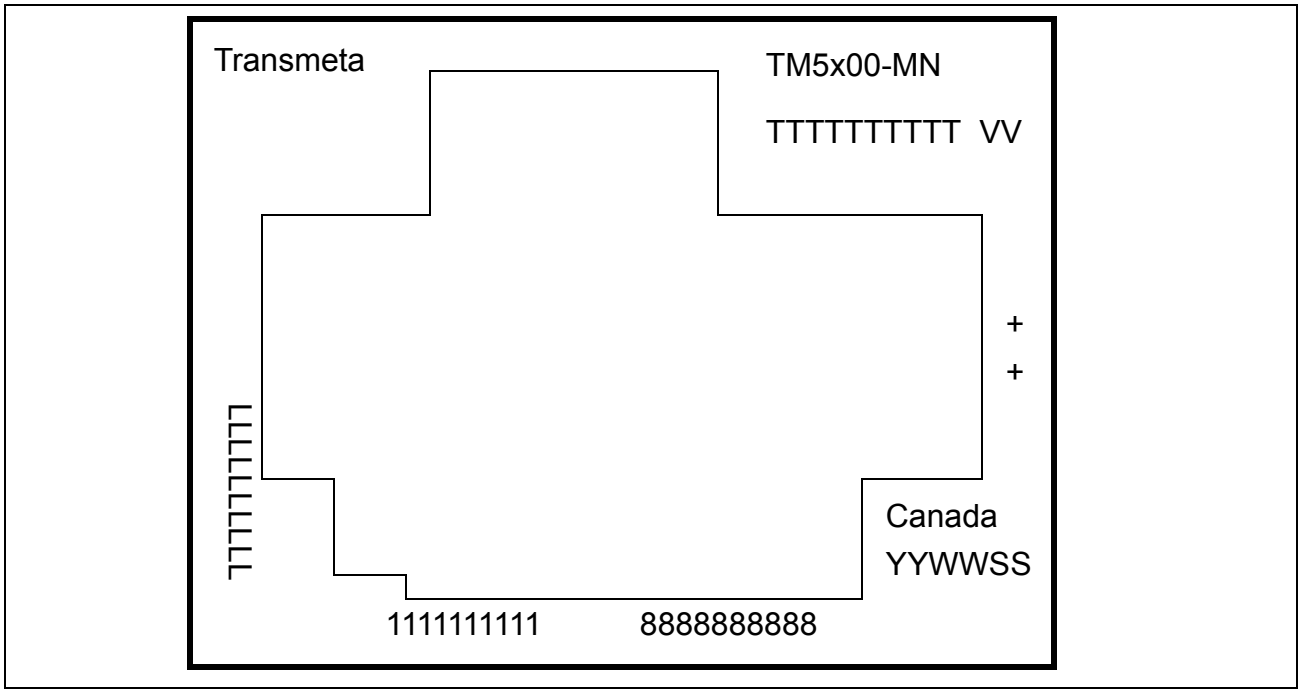


TABLE 48 Package Marking Descriptions

Field	Description
TM5x00-MN	Part name and revision number TM5400 Part name or TM5600 M Major revision number N Minor revision number
1111111111	Level 01 lot number - associated with the speed sort lot.
8888888888	Level 08 lot number - associated with the assembly lot.
TTTTTTTTTT	Transmeta manufacturing part number - identifies product SKU.
VV	Quality level indicator - ES for engineering sample, MS for mechanical sample; if left blank, the quality level is pre-production (PP) or mass (MP).
Canada	Country of origin - currently all TM5400/TM5600 parts are assembled in Canada.
YYWWSS	Date code/modification code - year (YY) and workweek (WW) the part was assembled; SS is a product modification code for modifications not indicated by major and minor revision numbers.
LLLLLLLLLL	Substrate part number - assigned by the substrate manufacturer.
+	Balling rework status - each + indicates one BGA balling rework cycle.