

**TC74HC390AP, TC74HC390AF, TC74HC390AFN**

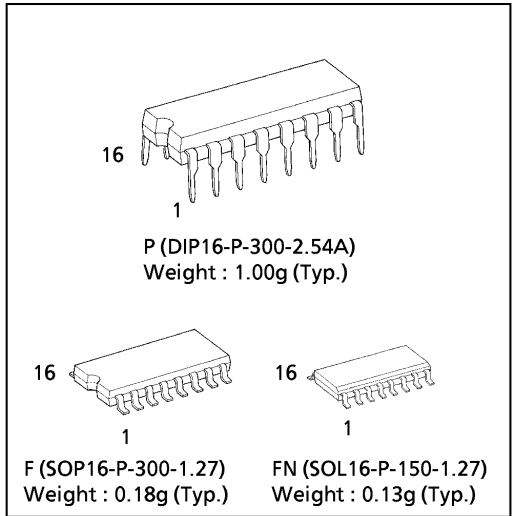
**DUAL DECADE COUNTER**

The TC74HC390A is a high speed CMOS DUAL DECADE COUNTER fabricated with silicon gate C<sup>2</sup>MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. It consists of two independent 4 - bit counters, each composed of a divide - by - two and a divide - by - five counter. The divide - by - two counter is incremented on the negative going transition of clock A( $\overline{CKA}$ ). The divided - by - five counter is incremented on the negative going transition of clock B( $\overline{CKB}$ ). The counter can be cascaded to form decade, bi - quinary, or various combinations up to a divide - by - 100 counter. When the CLR input is set high, the Q outputs are set to low independent of the clock inputs. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

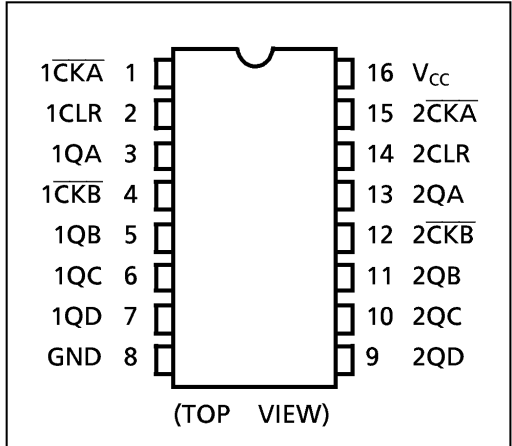
**FEATURES :**

- High Speed..... $f_{MAX} = 84\text{MHz}(\text{typ.})$   
at  $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 4\mu\text{A}(\text{Max.})$  at  $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC}(\text{Min.})$
- Output Drive Capability..... 10 LSTTL Loads
- Symmetrical Output Impedance...  $|I_{OH}| = I_{OL} = 4\text{mA}(\text{Min.})$
- Balanced Propagation Delays.....  $t_{PLH} \approx t_{PHL}$
- Wide Operating Voltage Range...  $V_{CC}(\text{opr.}) = 2\text{V} \sim 6\text{V}$
- Pin and Function Compatible with 74LS390

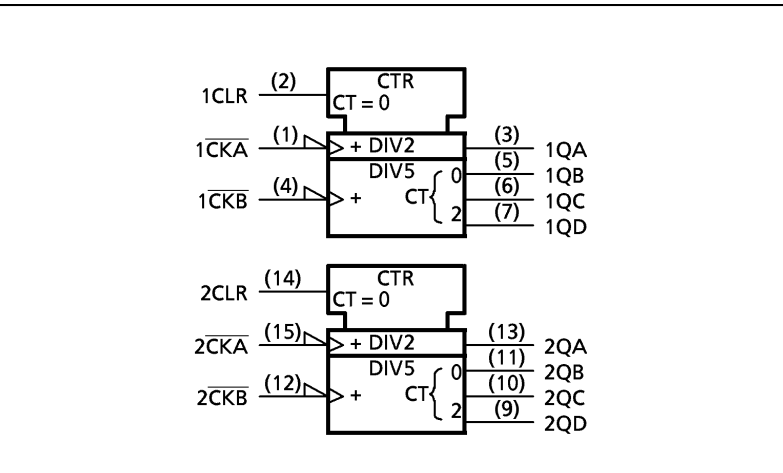
(Note) The JEDEC SOP (FN) is not available in Japan.



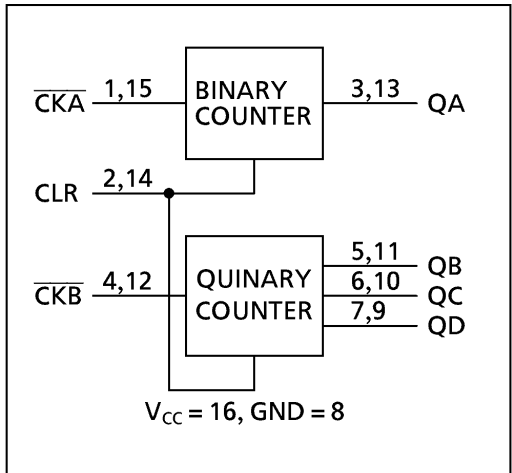
**PIN ASSIGNMENT**



**IEC LOGIC SYMBOL**



**BLOCK DAIGRAM**



961001EBA2

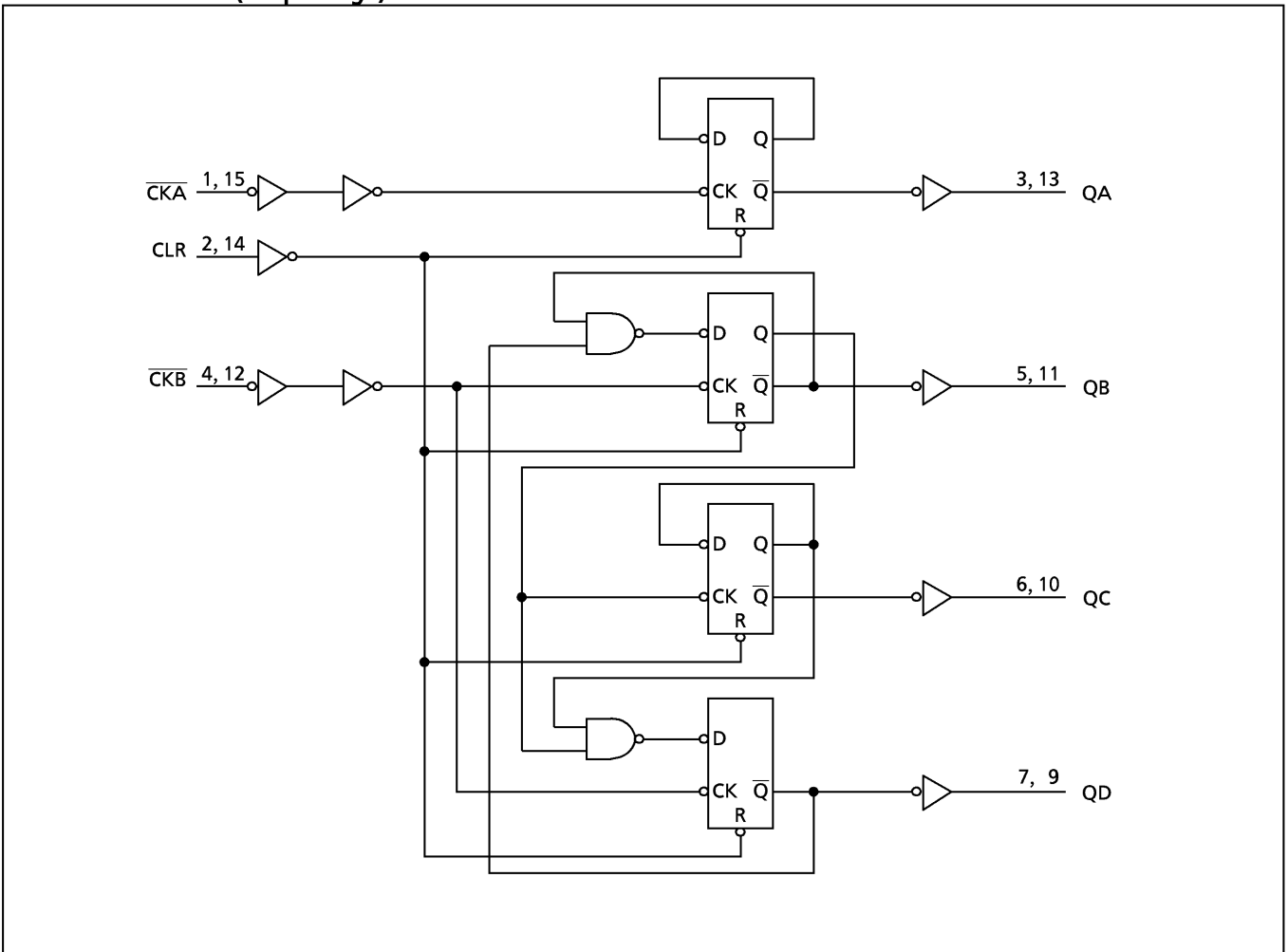
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**TRUTH TABLE**

INPUTS			OUTPUTS			
$\overline{CKA}$	$\overline{CKB}$	CLR	QA	QB	QC	QD
X	X	H	L	L	L	L
$\downarrow$	X	L	BINARY COUNT UP			
X	$\downarrow$	L	QUINARY COUNT UP			

X : Don't Care

**SYSTEM DIAGRAM (1/2 package)**

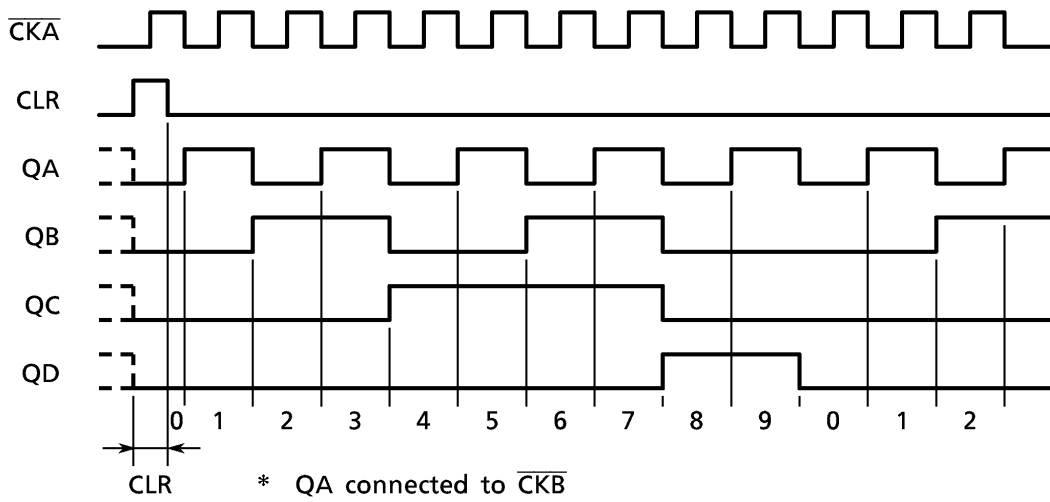


961001EBA2'

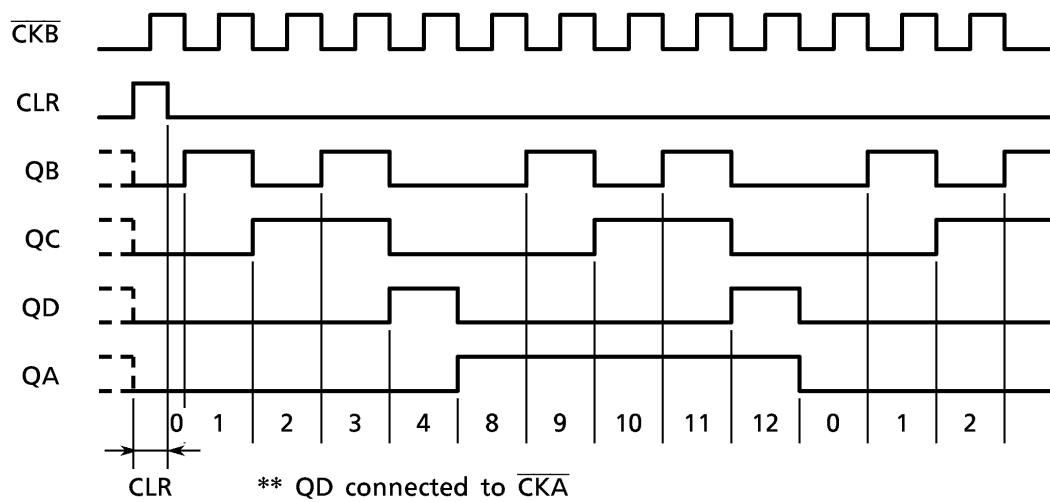
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TIMING CHART

(1) BCD COUNT SEQUENCE\*



(2) BI-QUINARY COUNT SEQUENCE\*\*



## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	$V_{CC}$	-0.5~7	V
DC Input Voltage	$V_{IN}$	-0.5~ $V_{CC}+0.5$	V
DC Output Voltage	$V_{OUT}$	-0.5~ $V_{CC}+0.5$	V
Input Diode Current	$I_{IK}$	$\pm 20$	mA
Output Diode Current	$I_{OK}$	$\pm 20$	mA
DC Output Current	$I_{OUT}$	$\pm 25$	mA
DC $V_{CC}$ /Ground Current	$I_{CC}$	$\pm 50$	mA
Power Dissipation	$P_D$	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	$T_{stg}$	-65~150	°C

\*500mW in the range of  $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$ . From  $T_a = 65^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  a derating factor of  $-10\text{mW}/^{\circ}\text{C}$  shall be applied until 300mW.

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	$V_{CC}$	2~6	V
Input Voltage	$V_{IN}$	0~ $V_{CC}$	V
Output Voltage	$V_{OUT}$	0~ $V_{CC}$	V
Operating Temperature	$T_{opr}$	-40~85	°C
Input Rise and Fall Time	$t_r, t_f$	0~1000 ( $V_{CC} = 2.0\text{V}$ ) 0~500 ( $V_{CC} = 4.5\text{V}$ ) 0~400 ( $V_{CC} = 6.0\text{V}$ )	ns

## DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}$ (V)	$T_a = 25^{\circ}\text{C}$			$T_a = -40 \sim 85^{\circ}\text{C}$		UNIT		
				MIN.	TYP.	MAX.	MIN.	MAX.			
High - Level Input Voltage	$V_{IH}$		2.0	1.50	—	—	1.50	—	V		
			4.5	3.15	—	—	3.15	—			
			6.0	4.20	—	—	4.20	—			
Low - Level Input Voltage	$V_{IL}$		2.0	—	—	0.50	—	0.50	V		
			4.5	—	—	1.35	—	1.35			
			6.0	—	—	1.80	—	1.80			
High - Level Output Voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -20\mu\text{A}$	2.0	1.9	2.0	—	1.9	—	V	
				4.5	4.4	4.5	—	4.4	—		
			4.5	$I_{OH} = -4\text{ mA}$ $I_{OH} = -5.2\text{ mA}$	4.5	4.18	4.31	—	4.13		—
					6.0	5.68	5.80	—	5.63		—
Low - Level Output Voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 20\mu\text{A}$	2.0	—	0.0	0.1	—	0.1	V	
				4.5	—	0.0	0.1	—	0.1		
			4.5	$I_{OL} = 4\text{ mA}$ $I_{OL} = 5.2\text{ mA}$	4.5	—	0.17	0.26	—		0.33
					6.0	—	0.18	0.26	—		0.33
Input Leakage Current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND	6.0	—	—	$\pm 0.1$	—	$\pm 1.0$	$\mu\text{A}$		
Quiescent Supply Current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	6.0	—	—	4.0	—	40.0			

TIMING REQUIREMENTS (Input  $t_r = t_f = 6\text{ns}$ )

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}$ (V)	$T_a = 25^\circ\text{C}$		$T_a = -40\sim 85^\circ\text{C}$	UNIT
				TYP.	LIMIT	LIMIT	
Minimum Pulse Width ( $\overline{CK}$ )	$t_{W(H)}$ $t_{W(L)}$		2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Pulse Width (CLR)	$t_{W(H)}$		2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Removal Time	$t_{rem}$		2.0	—	25	30	
			4.5	—	5	6	
			6.0	—	5	5	
Clock Frequency ( $\overline{CKA}$ )	f		2.0	—	6	5	MHz
			4.5	—	32	26	
			6.0	—	38	31	
Clock Frequency ( $\overline{CKB}$ )	f		2.0	—	6	5	
			4.5	—	31	25	
			6.0	—	36	29	

AC ELECTRICAL CHARACTERISTICS ( $C_L = 15\text{pF}$ ,  $V_{CC} = 5\text{V}$ ,  $T_a = 25^\circ\text{C}$ , Input  $t_r = t_f = 6\text{ns}$ )

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	$t_{TLH}$		—	4	8	ns
	$t_{THL}$					
Propagation Delay Time ( $\overline{CKA} - QA$ )	$t_{pLH}$		—	10	20	
	$t_{pHL}$					
Propagation Delay Time ( $\overline{CKA} - QC$ )	$t_{pLH}$ $t_{pHL}$	QA connected to $\overline{CKB}$	—	29	51	
Propagation Delay Time ( $\overline{CKB} - QB, QD$ )	$t_{pLH}$ $t_{pHL}$		—	12	22	
Propagation Delay Time ( $\overline{CKB} - QC$ )	$t_{pLH}$ $t_{pHL}$		—	17	32	
Propagation Delay Time (CLR - Qn)	$t_{pHL}$		—	12	26	
Maximum Clock Frequency ( $\overline{CKA}$ )	$f_{MAX}$		35	84	—	MHz
Maximum Clock Frequency ( $\overline{CKB}$ )	$f_{MAX}$		33	65	—	

**AC ELECTRICAL CHARACTERISTICS (  $C_L = 50\text{pF}$ , Input  $t_r = t_f = 6\text{ns}$  )**

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}$ (V)	$T_a = 25^\circ\text{C}$			$T_a = -40\sim 85^\circ\text{C}$		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	$t_{TLH}$ $t_{THL}$		2.0	—	30	75	—	95	ns
			4.5	—	8	15	—	19	
			6.0	—	7	13	—	16	
Propagation Delay Time ( $\overline{\text{CKA}} - \text{QA}$ )	$t_{pLH}$ $t_{pHL}$		2.0	—	39	120	—	150	
			4.5	—	13	24	—	30	
			6.0	—	11	20	—	26	
Propagation Delay Time ( $\text{CKA} - \text{QC}$ )	$t_{pLH}$ $t_{pHL}$	QA connected to CKB	2.0	—	102	290	—	365	
			4.5	—	34	58	—	73	
			6.0	—	29	49	—	62	
Propagation Delay Time ( $\overline{\text{CKB}} - \text{QB}, \text{QD}$ )	$t_{pLH}$ $t_{pHL}$		2.0	—	45	130	—	165	
			4.5	—	15	26	—	33	
			6.0	—	13	22	—	28	
Propagation Delay Time ( $\overline{\text{CKB}} - \text{QC}$ )	$t_{pLH}$ $t_{pHL}$		2.0	—	63	185	—	230	
			4.5	—	21	37	—	46	
			6.0	—	18	31	—	39	
Propagation Delay Time ( $\text{CLR} - \text{Qn}$ )	$t_{pHL}$		2.0	—	45	150	—	190	
			4.5	—	15	30	—	38	
			6.0	—	13	26	—	32	
Maximum Clock Frequency ( $\overline{\text{CKA}}$ )	$f_{MAX}$		2.0	6	20	—	5	—	MHz
			4.5	32	77	—	26	—	
			6.0	38	90	—	31	—	
Maximum Clock Frequency ( $\overline{\text{CKB}}$ )	$f_{MAX}$		2.0	6	15	—	5	—	
			4.5	32	60	—	25	—	
			6.0	36	70	—	29	—	
Input Capacitance	$C_{IN}$			—	5	10	—	10	pF
Power Dissipation Capacitance	$C_{PD} (1)$			—	44	—	—	—	

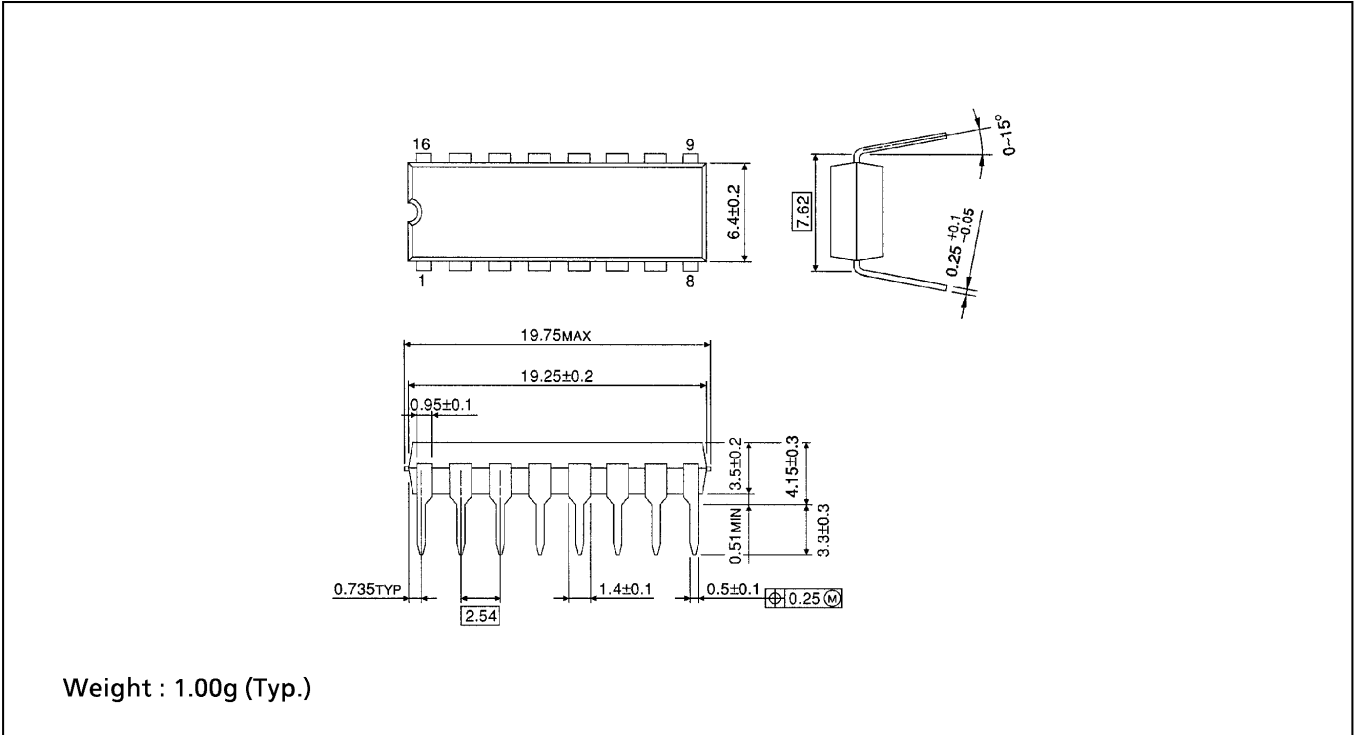
Note (1)  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 2 \text{ (per Counter)}$$

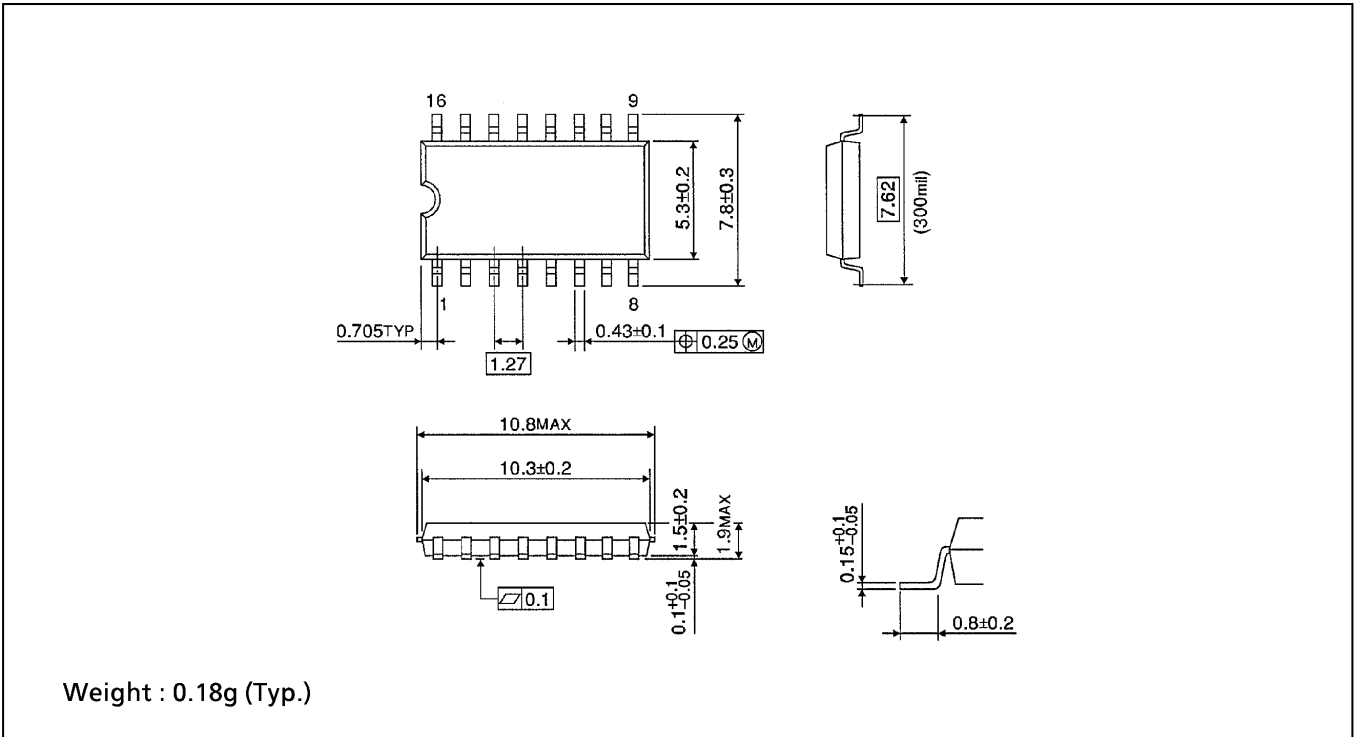
DIP 16PIN OUTLINE DRAWING (DIP16-P-300-2.54A)

Unit in mm



SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27)

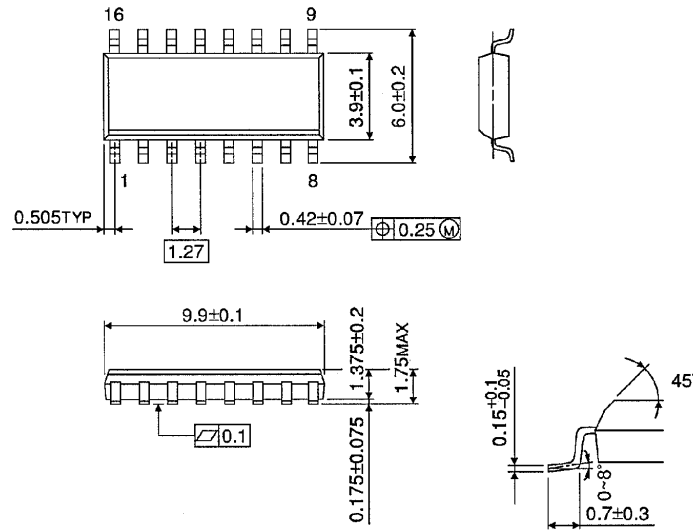
Unit in mm



**SOP 16PIN (150mil BODY) OUTLINE DRAWING (SOL16-P-150 -1.27)**

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)