DATA SHEET

PCF8831
STN RGB - 160 output row driver

Preliminary specification

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Philips
Semiconductors

PHILIPS

CONTENTS

1 FEATURES

- Row driver for LCD dot matrix
- 160 row outputs
- Selectable scan direction
- Support of display off function
- Support of N-line inversion
- Programmable connection to display module
- Logic supply voltage: 2.4 to 3.5 V
- Display supply voltage range: 15 to 40 V
- Low power consumption; suitable for battery operated systems
- CMOS compatible inputs
- Manufactured in silicon gate CMOS process.

2 APPLICATIONS

- Mobile phones
- Personal Digital Assistant (PDA)
- Automotive information systems
- Point-of-sale terminals
- Instrumentation.

3 GENERAL DESCRIPTION

The PCF8831 is a row driver for driving colour STN displays. It is designed to operate with the PCF8832 column driver IC.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8831U	–	chip with bumps in tray	–

5 BLOCK DIAGRAM

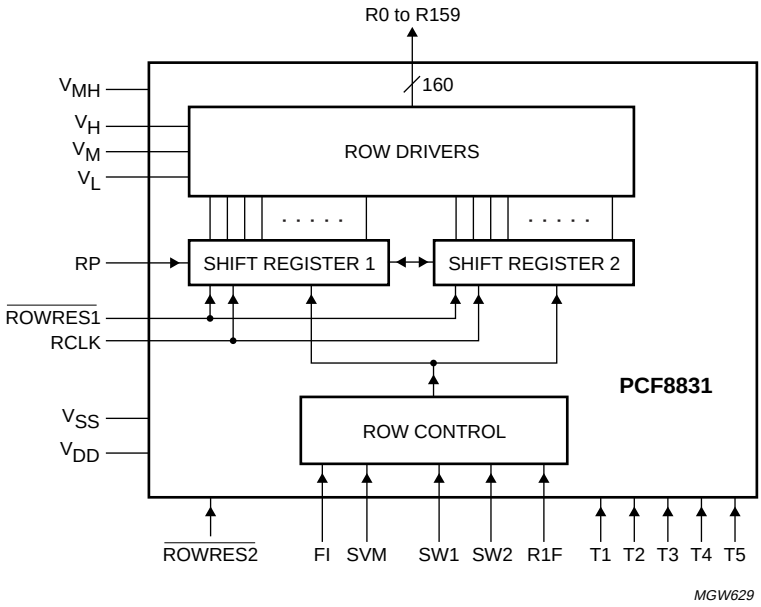


Fig.1 Block diagram.

6 PINNING

SYMBOL	PAD[1]	TYPE	DESCRIPTION
R159 to R0	2 to 161	O	LCD row outputs
RCLK	187	I	clock input to the shift register; data is transmitted with the positive clock edge; connect RCLK to the RCLK output of the PCF8832 column driver
RP	188	I	row pulse input; driven by the RP output of the PCF8832 column driver
FI	189	I	frame inversion input; controls frame and N-line inversion; FI is synchronized internally by the rising edge of RCLK; FI can change only when RP changes; connect FI to the FI output of the PCF8832 column driver
SVM	190	I	input that switches the non-selected level (V_M or V_{SS}, depending on $\overline{ROWRES2}$) to all row outputs; connect SVM to the SVM output of the PCF8832 column driver
$\overline{ROWRES1}$	191	I	external reset input 1; when LOW, the shift register is reset at the next rising edge of RCLK and all outputs (R0 to R159) go to their non-selected level; connect $\overline{ROWRES1}$ to the $\overline{RESROW}$ output of the PCF8832 column driver
$\overline{ROWRES2}$	192	I	external reset input 2; when LOW, the non-selected level goes to V_{SS}; when HIGH, the non-selected level goes to V_M; connect $\overline{ROWREST}$ to the $\overline{RESROW}$ output of the PCF8832 column driver
R1F	193	I	inputs R1F (row block 1 first), SW1 (swap row block 1) and SW2 (swap row block 2) control the shift direction through the register and the order of the register; see Table 1; connect to the corresponding signal outputs of the PCF8832 column driver, or connect directly to V_{DD} or V_{SS} as required by the display module configuration
SW1	194	I	
SW2	195	I	
T1 to T5	196 to 200	I	test inputs; connect to V_{SS} for normal operation
V_{SS}	201 to 207	PS	logic power supply, negative; normally connected to system ground
V_{DD}	208 to 214	PS	logic power supply, positive; 2.4 to 3.5 V referred to V_{SS}
V_M	215 to 221	PS	MID-level LCD driving voltage; level is between V_H and V_L; output at rows for non-selecting periods when $\overline{ROWRES2}$ is HIGH; 1.25 to 2.0 V referred to V_{SS}
V_{MH}	222 to 228	PS	auxiliary supply voltage for row switch; higher than V_M; limited at V_L + 40 V
V_H	229 to 235	PS	HIGH-level LCD driving voltage; top level of the positive selecting pulse of row outputs
V_L	236 to 242	PS	LOW-level LCD driving voltage; bottom level of the negative selecting pulse of row outputs

Note

1. Dummy pads are located at positions 1 (slanted), 162 to 186 and 243 to 272.

7 FUNCTIONAL DESCRIPTION

7.1 Row driver

The row driver comprises high voltage outputs, level shifters and logic circuits.

The row driver power supplies are:

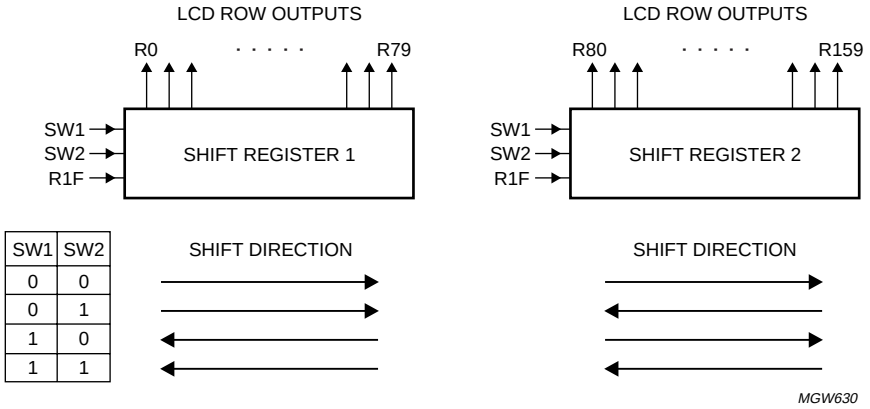
- V_H for the top level of selecting pulses
- V_L for the bottom level of selecting pulses
- V_M for the non-selecting level when $\overline{ROWRES2}$ = HIGH; the non-selecting level goes to V_{SS} when $\overline{ROWRES2}$ = LOW (active)
- V_{MH} is an intermediate auxiliary supply
- V_{DD} and V_{SS} for the logic circuits.

7.2 80-bit shift register

Two shift registers of 80 bits each are contained in the PCF8831 row driver. With $\overline{ROWRES1}$, the complete shift register will be reset at the next rising edge of RCLK. The two shift registers can be configured for different applications by row control signals R1F, SW1 and SW2.

7.3 Row control

Row control signals SW1, SW2 and R1F control the shift direction through the register and the order of the register (see Fig.2). Some switching combinations require the order of one or both shift registers to be swapped as shown by the example in Fig.3. All row control combinations are shown in Table 1, these can be software controlled when connected to the corresponding row control signals of the PCF8832 column driver.



SW1	SW2
0	0
0	1
1	0
1	1

Fig.2 Shift directions; R1F = 1.

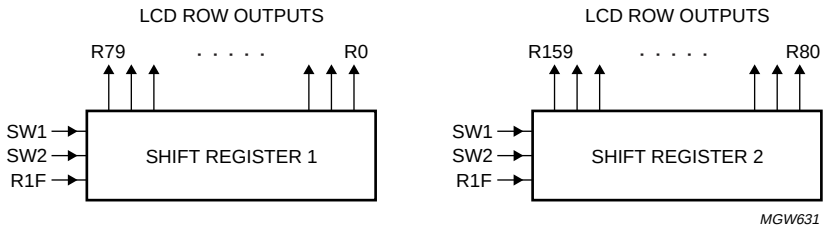


Fig.3 Row swapping; SW1 = SW2 = 1.

Table 1 Row control switching

ROW CONTROL SIGNALS			FIRST REGISTER SELECTED	SECOND REGISTER SELECTED
R1F	**SW1**	**SW2**		
1	0	0	R0 to R79	R80 to R159
1	0	1	R0 to R79	R159 to R80
1	1	0	R79 to R0	R80 to R159
1	1	1	R79 to R0	R159 to R80
0	0	0	R80 to R159	R0 to R79
0	0	1	R159 to R80	R0 to R79
0	1	0	R80 to R159	R79 to R0
0	1	1	R159 to R80	R79 to R0

7.4 Frame control

The signal FI controls frame inversion (Fig.4) and N-line inversion (Fig.5). Software control of FI is performed via the PCF8832 column driver.

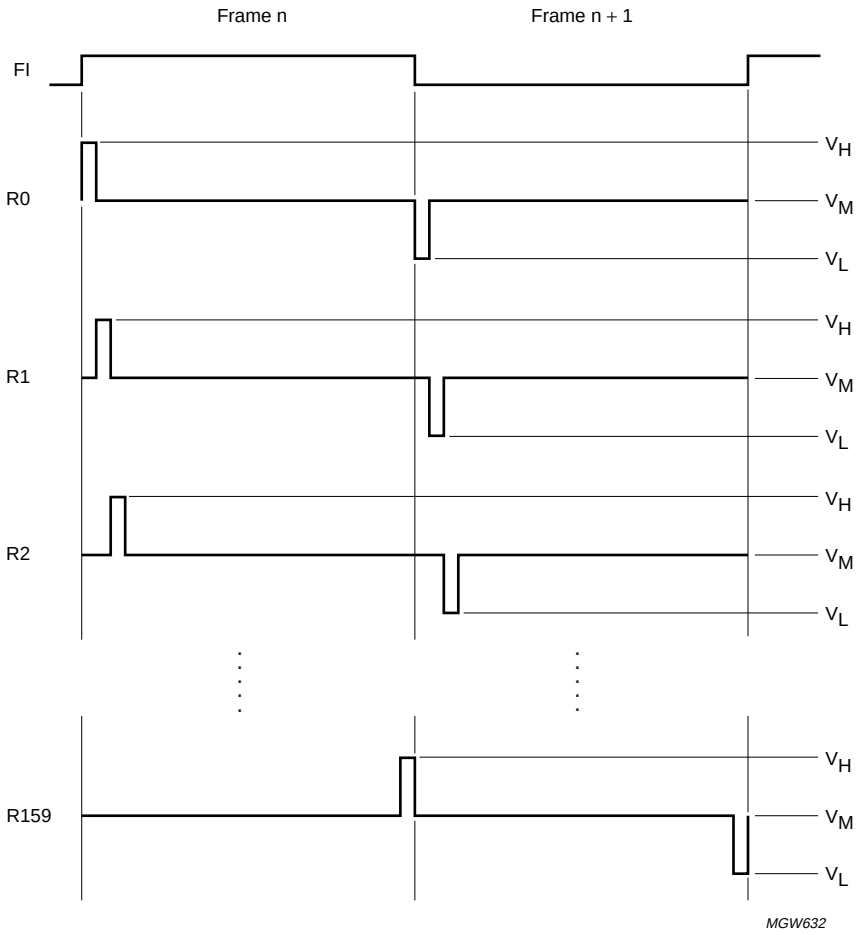


Fig.4 Frame inversion.

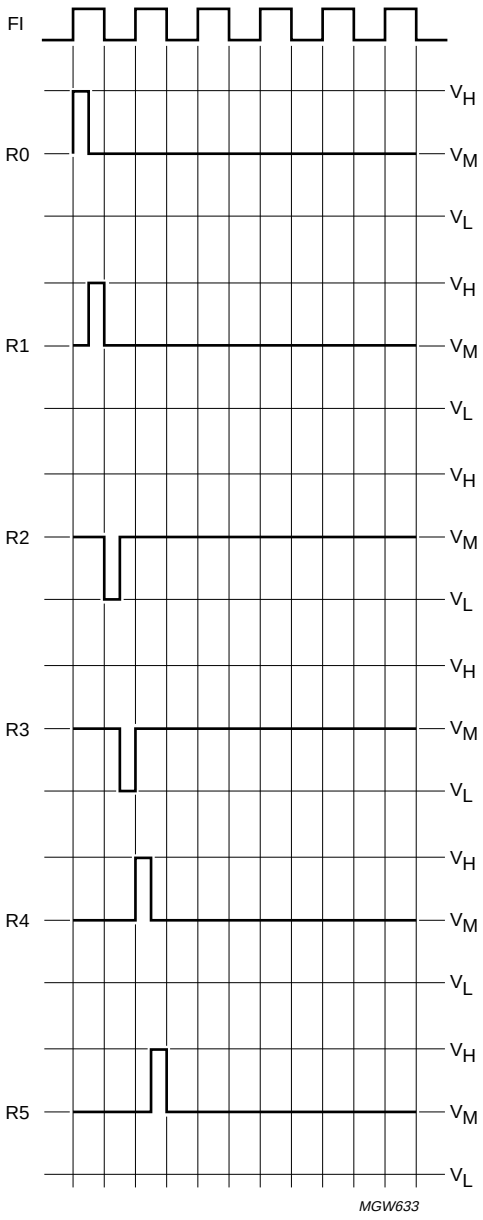


Fig.5 N-line inversion; N = 2.

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); note 1.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	logic supply positive voltage	V_{SS} – 0.3	V_{SS} + 7.0	V
V_{SS}	logic supply negative voltage	V_L – 0.3	V_L + 40.0	V
V_{MH}	auxiliary supply voltage for row switching	V_L – 0.3	V_L + 45.0	V
V_H	HIGH-level LCD driving voltage	V_L – 0.3	V_L + 45	V
V_M	MID-level LCD driving voltage	V_L – 0.3	V_H + 0.3	V
		V_H – 45.0	V_L + 45.0	V
		V_{SS} – 0.3	V_{SS} + 7.0	V
V_I	input voltage	V_{SS} – 0.3	V_{DD} + 0.3	V
T_{oper}	operating temperature	–40	+85	°C
T_{stg}	storage temperature	–65	+150	°C

Note

1. Parameters are valid over the operating temperature range; all voltages are referred to V_L; substrate potential = V_L; unless otherwise specified.

9 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is recommended to take normal precautions appropriate to handling MOS devices (see *“Handling MOS Devices”*).

10 DC CHARACTERISTICS

(V_{DD} – V_{SS}) = 2.4 to 3.5 V; (V_H – V_L) = 15 to 55 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_L	LOW-level LCD driving voltage		–	0	–	V
V_H	HIGH-level LCD driving voltage		V_L + 15.0	–	V_L + 45.0	V
V_M	MID-level LCD driving voltage		V_{SS}	$\frac{V_L + V_H}{2}$	V_{DD}	V
V_{MH}	auxiliary supply voltage for row switching		note 1	V_M + 10	V_L + 40	V
V_{SS}	logic supply negative voltage		V_M – 2.0	–	V_M – 1.25	V
V_{DD}	logic supply positive voltage		V_{SS} + 2.4	–	V_{SS} + 3.5	V
V_{IH}	HIGH-level input voltage	all inputs; referred to V_{SS}	V_{SS} + 0.8 × (V_{DD} – V_{SS})	–	V_{DD}	V
V_{IL}	LOW-level input voltage	all inputs; referred to V_{SS}	V_{SS}	–	V_{SS} + 0.2 × (V_{DD} – V_{SS})	V
I_{LI}	input leakage current	all inputs				
		$V_I = V_{DD}$	–	–	5	µA
		$V_I = V_{SS}$	–5	–	–	µA
R_O	row output on-state resistance	notes 2 and 3				
		I_O = +100 µA	–	600	tbf	Ω
		I_O = ±100 µA	–	600	tbf	Ω
		I_O = –100 µA	–	600	tbf	Ω
I_{DD}	current at pad V_{DD}	notes 3, 4 and 5	–	30	tbf	µA
I_{VH}	current at pad V_H		–	10	tbf	µA
I_{VMH}	current at pad V_{MH}		–	3	tbf	µA
I_{VM}	current at pad V_M		–	2	tbf	µA
I_{VL}	current at pad V_L		–	13	tbf	µA

Notes

1. The minimum level of (V_{MH} – V_M) depends on (V_M – V_L); a lower level of (V_M – V_L) requires lower offset of V_{MH} referred to V_M. A higher level of (V_{MH} – V_M) improves dynamic behaviour. A minimum level of (V_{MH} – V_M) = 2.5 V + 0.2 × (V_M – V_L) should be maintained.
2. Row outputs tested one at a time.
3. (V_H – V_L) = 37 V; V_{MH} = V_H; (V_{DD} – V_{SS}) = 2.8 V; $V_M = \frac{V_H + V_L}{2}$; ($V_M$ – V_{SS}) = 1.47 V.
4. f_{RCLK} = 19.2 kHz; SVM = 0; $\overline{\text{ROWRES1}}$ = $\overline{\text{ROWRES2}}$ = HIGH; single line mode; all row outputs open-circuit.
5. Frame inversion frequency $f_{FI} = \frac{f_{RCLK}}{2 \times 160}$.

11 AC CHARACTERISTICS

(V_{DD} – V_{SS}) = 2.4 to 3.5 V; (V_H – V_L) = 15 to 55 V; T_{amb} = –40 to +85 °C; see Fig.6.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
f_{RCLK}	RCLK clock frequency	–	19.2	700	kHz
t_{RCLKL}	RCLK clock LOW time	100	–	–	ns
t_{RCLKH}	RCLK clock HIGH time	100	–	–	ns
t_r	input rise time RCLK, RP, FI, SVM, $\overline{ROWRES1}$ and $\overline{ROWRES2}$	–	–	50	ns
t_f	input fall time RCLK, RP, FI, SVM, $\overline{ROWRES1}$ and $\overline{ROWRES2}$	–	–	50	ns
$t_{su(D)}$	data setup time RP, FI and $\overline{ROWRES1}$	50	–	–	ns
$t_{h(D)}$	data hold time RP, FI and $\overline{ROWRES1}$	50	–	–	ns

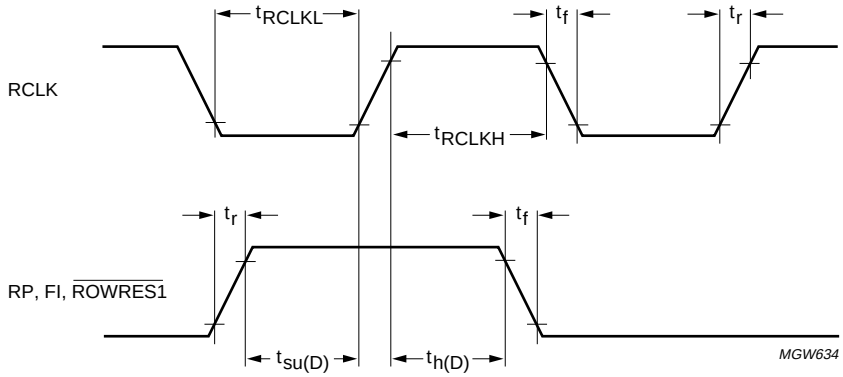


Fig.6 AC waveforms showing RCLK and data input.

11.1 Power-up and power-down sequences

When the PCF8831 is powering-up or powering-down, the various supply voltages and some interface signals have to be applied in a certain sequence.

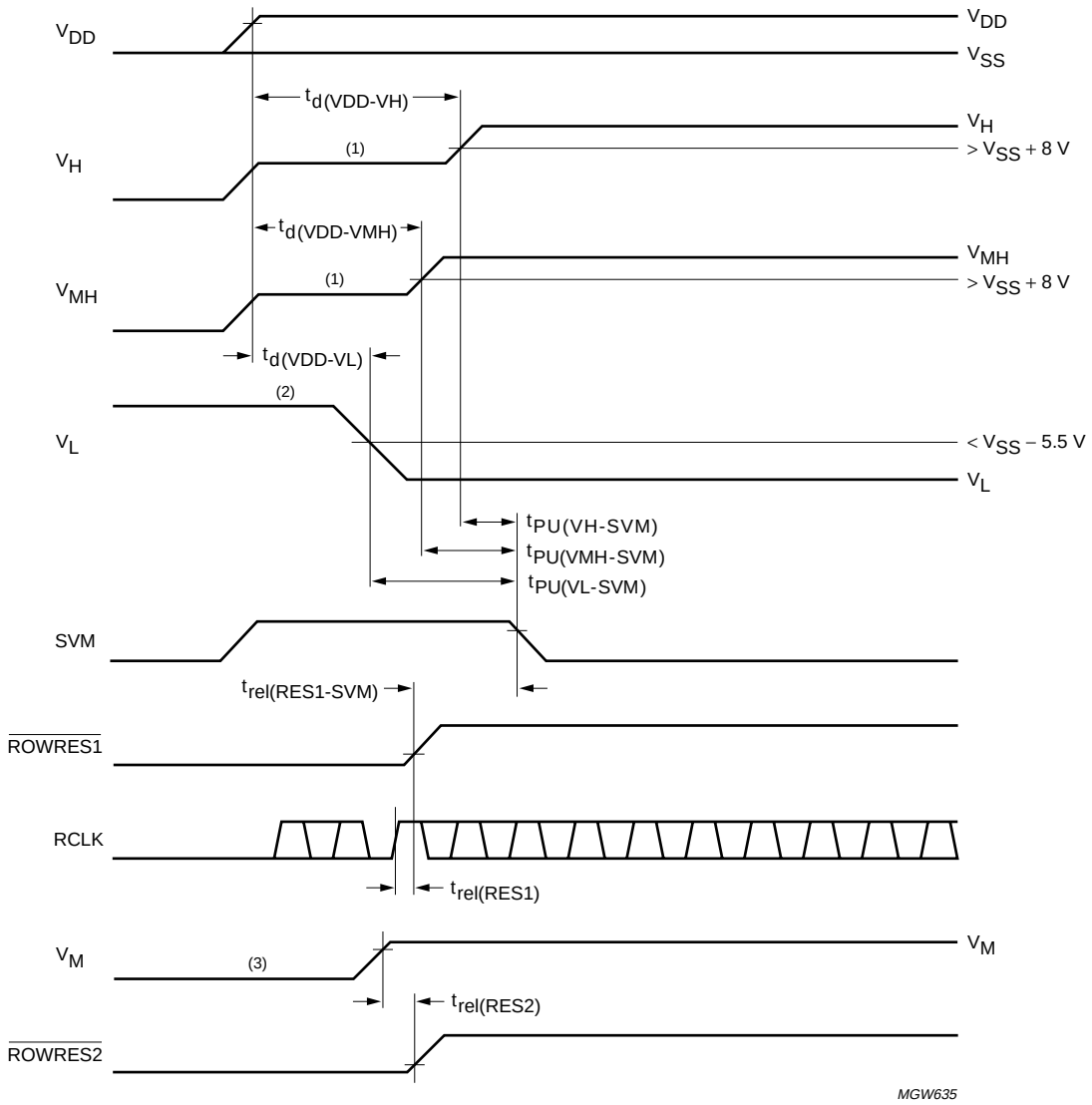
Table 2 Power-up and power-down sequences

T_{amb} = −40 to +85 °C; refer to Figs 7 and 8.

SYMBOL	PARAMETER	CONDITIONS	MIN.	UNIT
$t_{d(VDD-VH)}$	delay $V_{DD(on)}$ to $V_{H(on)}$	note 1	0	ns
$t_{d(VDD-VMH)}$	delay $V_{DD(on)}$ to $V_{MH(on)}$	note 1	0	ns
$t_{d(VDD-VL)}$	delay $V_{DD(on)}$ to $V_{L(on)}$	note 2	0	ns
$t_{d(VH-VDD)}$	delay $V_{H(off)}$ to $V_{DD(off)}$	note 1	0	ns
$t_{d(VMH-VDD)}$	delay $V_{MH(off)}$ to $V_{DD(off)}$	note 1	0	ns
$t_{d(VL-VDD)}$	delay $V_{L(off)}$ to $V_{DD(off)}$	note 2	0	ns
$t_{PU(VH-SVM)}$	power-up time $V_{H(on)}$ to SVM inactive	SVM falls to V_{SS}	0	ns
$t_{PU(VMH-SVM)}$	power-up time $V_{MH(on)}$ to SVM inactive	SVM falls to V_{SS}	0	ns
$t_{PU(VL-SVM)}$	power-up time $V_{L(on)}$ to SVM inactive	SVM falls to V_{SS}	0	ns
$t_{rel(RES1-SVM)}$	$\overline{\text{ROWRES1}}$ release time to SVM inactive	release $\overline{\text{ROWRES1}}$ before making SVM inactive	0	ns
$t_{rel(RES1)}$	$\overline{\text{ROWRES1}}$ release time	allow at least one rising RCLK edge before releasing $\overline{\text{ROWRES1}}$	50	ns
$t_{rel(RES2)}$	$\overline{\text{ROWRES2}}$ release time	define V_M when $\overline{\text{ROWRES2}}$ is inactive; note 3	0	ns
$t_{PD(VH)}$	power-down time from SVM active to $V_{H(off)}$		0	ns
$t_{PD(VMH)}$	power-down time from SVM active to $V_{MH(off)}$		0	ns
$t_{PD(VL)}$	power-down time from SVM active to $V_{L(off)}$		0	ns

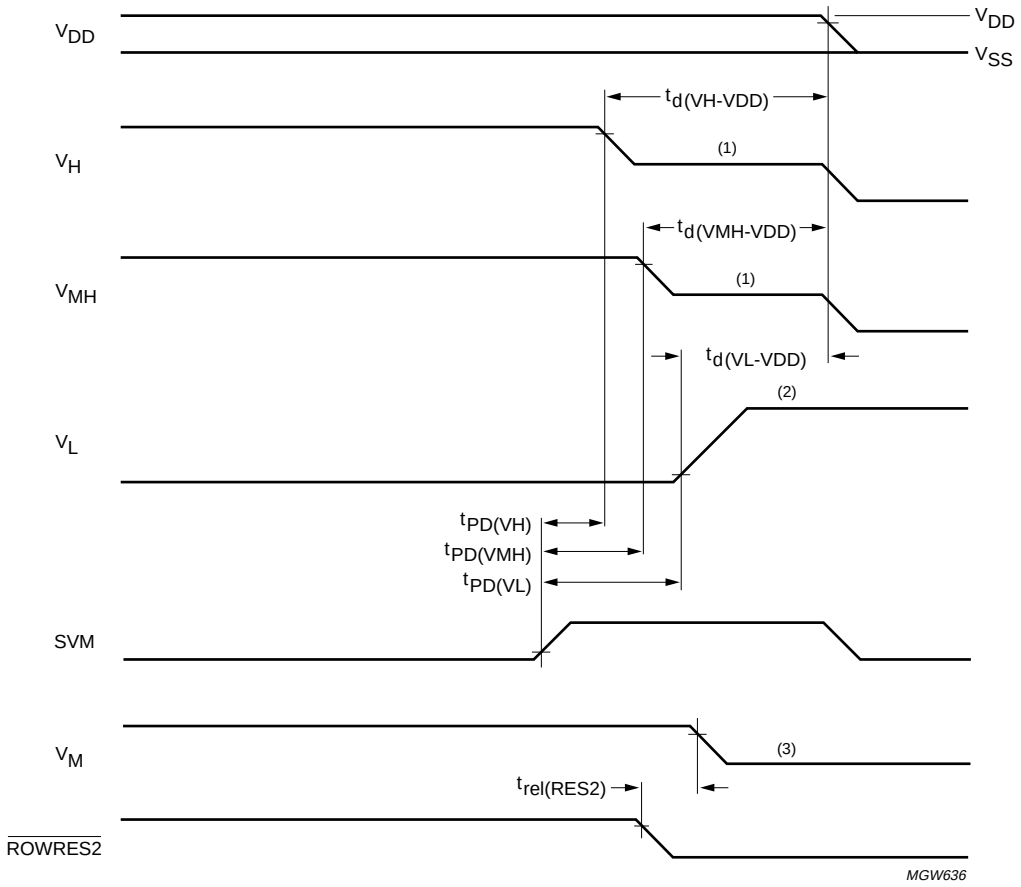
Notes

1. With no V_H or V_{MH} supply, both pads V_H and V_{MH} are clamped by separate internal diodes to V_{DD}, see Fig.10.
2. When no V_L is supplied, pad V_L is clamped to V_{SS} by a separate internal diode, see Fig.10.
3. When $\overline{\text{ROWRES2}}$ is active (at V_{SS}), the level not-selected goes to V_{SS} and pad V_M can be disconnected.



(1) With no V_H or V_{MH} supply, both pads V_H and V_{MH} are clamped by separate internal diodes to V_{DD}; see Table 2 and Fig.10.
(2) When no V_L is supplied, pad V_L is clamped to V_{SS} by a separate internal diode; see Table 2 and Fig.10.
(3) When $\overline{ROWRES2}$ is active (at V_{SS}), the level not-selected goes to V_{SS} and V_M can be disconnected; see Table 2 and Fig.10.

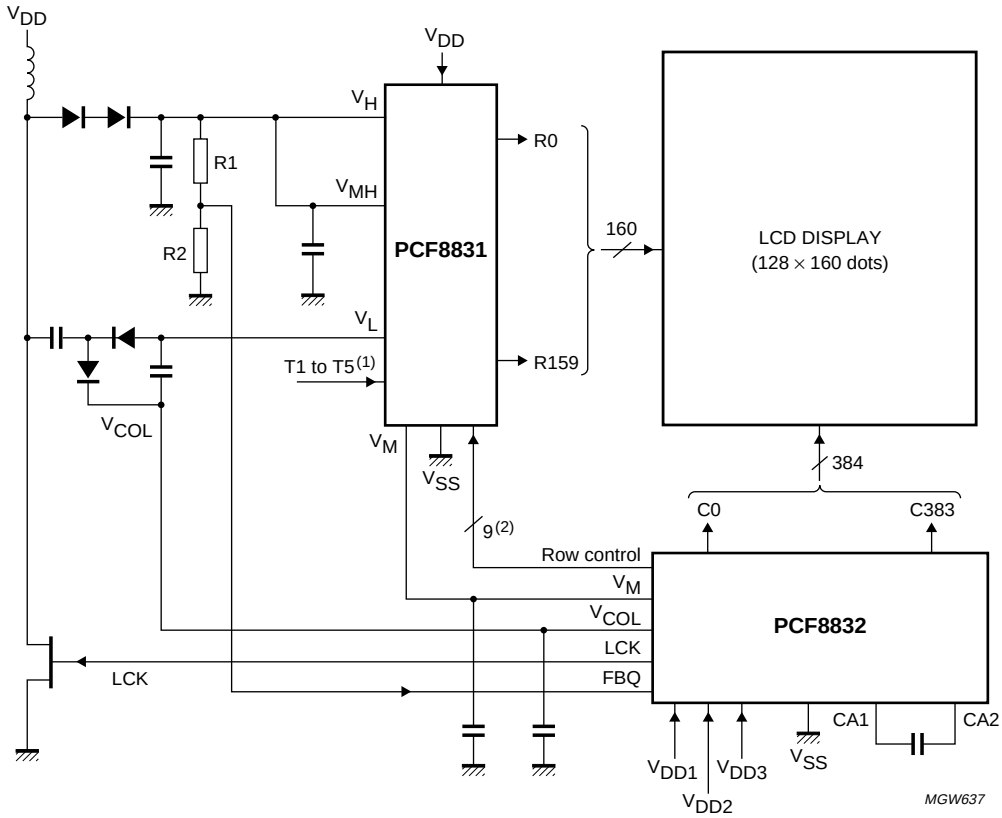
Fig.7 Power-up sequence.



(1) With no V_H or V_{MH} supply, both pads V_H and V_{MH} are clamped by separate internal diodes to V_{DD}; see Table 2 and Fig.10.
(2) When no V_L is supplied, pad V_L is clamped to V_{SS} by a separate internal diode; see Table 2 and Fig.10.
(3) When $\overline{ROWRES2}$ is active (at V_{SS}), the level not-selected goes to V_{SS} and pad V_M can be disconnected; see Table 2 and Fig.10.

Fig.8 Power-down sequence.

12 APPLICATION INFORMATION

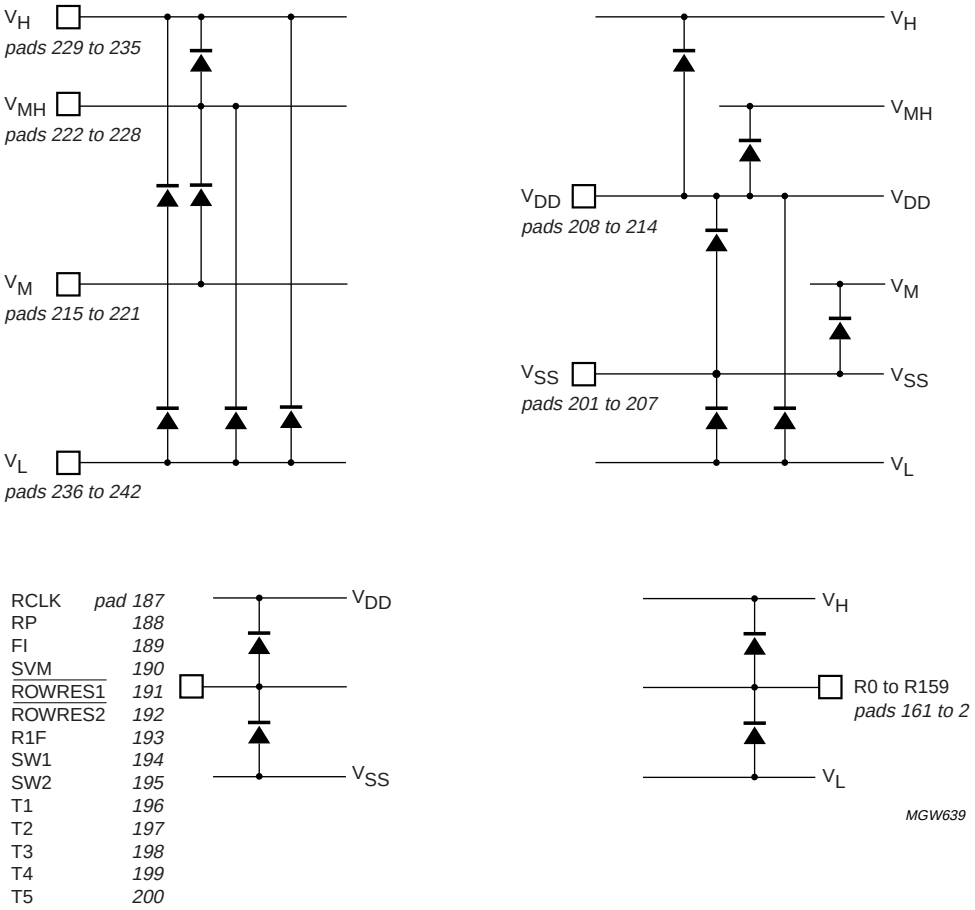


(1) Test inputs T1 to T5 have to be tied to V_{SS}.

(2) Row control signals are RCLK, RP, FI, SVM, $\overline{\text{RESROW1}}$, $\overline{\text{RESROW2}}$, SW1, SW2 and R1F.

Fig.9 Application example using PCF8831 with PCF8832.

13 INTERNAL PROTECTION CIRCUITS



Protection diode maximum forward current = 5 mA.

Fig.10 Protection circuit diagrams.

14 BONDING PAD INFORMATION

Table 3 Pad locations

All x and y coordinates are referenced to the centre of the chip (dimensions in μm; see Fig.13)

SYMBOL	PAD	x	y
Dummy (slanted)	1	−6116.0	−768.0
R159	2	−5984.0	−768.0
R158	3	−5909.0	−768.0
R157	4	−5834.0	−768.0
R156	5	−5759.0	−768.0
R155	6	−5684.0	−768.0
R154	7	−5609.0	−768.0
R153	8	−5534.0	−768.0
R152	9	−5459.0	−768.0
R151	10	−5384.0	−768.0
R150	11	−5309.0	−768.0
R149	12	−5234.0	−768.0
R148	13	−5159.0	−768.0
R147	14	−5084.0	−768.0
R146	15	−5009.0	−768.0
R145	16	−4934.0	−768.0
R144	17	−4859.0	−768.0
R143	18	−4784.0	−768.0
R142	19	−4709.0	−768.0
R141	20	−4634.0	−768.0
R140	21	−4559.0	−768.0
R139	22	−4484.0	−768.0
R138	23	−4409.0	−768.0
R137	24	−4334.0	−768.0
R136	25	−4259.0	−768.0
R135	26	−4184.0	−768.0
R134	27	−4109.0	−768.0
R133	28	−4034.0	−768.0
R132	29	−3959.0	−768.0
R131	30	−3884.0	−768.0
R130	31	−3809.0	−768.0
R129	32	−3734.0	−768.0
R128	33	−3659.0	−768.0
R127	34	−3584.0	−768.0
R126	35	−3509.0	−768.0
R125	36	−3434.0	−768.0
R124	37	−3359.0	−768.0
R123	38	−3284.0	−768.0
R122	39	−3209.0	−768.0
R121	40	−3134.0	−768.0
R120	41	−3059.0	−768.0
R119	42	−2984.0	−768.0
R118	43	−2909.0	−768.0
R117	44	−2834.0	−768.0
R116	45	−2759.0	−768.0
R115	46	−2684.0	−768.0
R114	47	−2609.0	−768.0
R113	48	−2534.0	−768.0
R112	49	−2459.0	−768.0
R111	50	−2384.0	−768.0
R110	51	−2309.0	−768.0
R109	52	−2234.0	−768.0
R108	53	−2159.0	−768.0
R107	54	−2084.0	−768.0
R106	55	−2009.0	−768.0
R105	56	−1934.0	−768.0
R104	57	−1859.0	−768.0
R103	58	−1784.0	−768.0
R102	59	−1709.0	−768.0
R101	60	−1634.0	−768.0
R100	61	−1559.0	−768.0
R99	62	−1484.0	−768.0
R98	63	−1409.0	−768.0
R97	64	−1334.0	−768.0
R96	65	−1259.0	−768.0
R95	66	−1184.0	−768.0
R94	67	−1109.0	−768.0
R93	68	−1034.0	−768.0
R92	69	−959.0	−768.0
R91	70	−884.0	−768.0
R90	71	−809.0	−768.0
R89	72	−734.0	−768.0
R88	73	−659.0	−768.0
R87	74	−584.0	−768.0
R86	75	−509.0	−768.0
R85	76	−434.0	−768.0
R84	77	−359.0	−768.0

SYMBOL	PAD	x	y
R83	78	−284.0	−768.0
R82	79	−209.0	−768.0
R81	80	−134.0	−768.0
R80	81	−59.0	−768.0
R79	82	+91.0	−768.0
R78	83	+166.0	−768.0
R77	84	+241.0	−768.0
R76	85	+316.0	−768.0
R75	86	+391.0	−768.0
R74	87	+466.0	−768.0
R73	88	+541.0	−768.0
R72	89	+616.0	−768.0
R71	90	+691.0	−768.0
R70	91	+766.0	−768.0
R69	92	+841.0	−768.0
R68	93	+916.0	−768.0
R67	94	+991.0	−768.0
R66	95	+1066.0	−768.0
R65	96	+1141.0	−768.0
R64	97	+1216.0	−768.0
R63	98	+1291.0	−768.0
R62	99	+1366.0	−768.0
R61	100	+1441.0	−768.0
R60	101	+1516.0	−768.0
R59	102	+1591.0	−768.0
R58	103	+1666.0	−768.0
R57	104	+1741.0	−768.0
R56	105	+1816.0	−768.0
R55	106	+1891.0	−768.0
R54	107	+1966.0	−768.0
R53	108	+2041.0	−768.0
R52	109	+2116.0	−768.0
R51	110	+2191.0	−768.0
R50	111	+2266.0	−768.0
R49	112	+2341.0	−768.0
R48	113	+2416.0	−768.0
R47	114	+2491.0	−768.0
R46	115	+2566.0	−768.0
R45	116	+2641.0	−768.0
R44	117	+2716.0	−768.0
R43	118	+2791.0	−768.0

SYMBOL	PAD	x	y
R42	119	+2866.0	−768.0
R41	120	+2941.0	−768.0
R40	121	+3016.0	−768.0
R39	122	+3091.0	−768.0
R38	123	+3166.0	−768.0
R37	124	+3241.0	−768.0
R36	125	+3316.0	−768.0
R35	126	+3391.0	−768.0
R34	127	+3466.0	−768.0
R33	128	+3541.0	−768.0
R32	129	+3616.0	−768.0
R31	130	+3691.0	−768.0
R30	131	+3766.0	−768.0
R29	132	+3841.0	−768.0
R28	133	+3916.0	−768.0
R27	134	+3991.0	−768.0
R26	135	+4066.0	−768.0
R25	136	+4141.0	−768.0
R24	137	+4216.0	−768.0
R23	138	+4291.0	−768.0
R22	139	+4366.0	−768.0
R21	140	+4441.0	−768.0
R20	141	+4516.0	−768.0
R19	142	+4591.0	−768.0
R18	143	+4666.0	−768.0
R17	144	+4741.0	−768.0
R16	145	+4816.0	−768.0
R15	146	+4891.0	−768.0
R14	147	+4966.0	−768.0
R13	148	+5041.0	−768.0
R12	149	+5116.0	−768.0
R11	150	+5191.0	−768.0
R10	151	+5266.0	−768.0
R9	152	+5341.0	−768.0
R8	153	+5416.0	−768.0
R7	154	+5491.0	−768.0
R6	155	+5566.0	−768.0
R5	156	+5641.0	−768.0
R4	157	+5716.0	−768.0
R3	158	+5791.0	−768.0
R2	159	+5866.0	−768.0

SYMBOL	PAD	x	y
R1	160	+5941.0	−768.0
R0	161	+6016.0	−768.0
Dummy	162	+6155.0	−768.0
Dummy	163	6096.5	865.7
Dummy	164	6021.5	865.7
Dummy	165	5796.5	865.7
Dummy	166	5721.5	865.7
Dummy	167	5646.5	865.7
Dummy	168	5571.5	865.7
Dummy	169	5496.5	865.7
Dummy	170	5421.5	865.7
Dummy	171	5346.5	865.7
Dummy	172	5271.5	865.7
Dummy	173	5196.5	865.7
Dummy	174	5121.5	865.7
Dummy	175	5046.5	865.7
Dummy	176	4971.5	865.7
Dummy	177	4896.5	865.7
Dummy	178	4821.5	865.7
Dummy	179	4746.5	865.7
Dummy	180	4671.5	865.7
Dummy	181	4596.5	865.7
Dummy	182	4521.5	865.7
Dummy	183	4446.5	865.7
Dummy	184	3921.5	865.7
Dummy	185	3846.5	865.7
Dummy	186	3771.5	865.7
RCLK	187	3506.0	865.7
RP	188	3350.0	865.7
FI	189	3186.0	865.7
SVM	190	3030.0	865.7
$\overline{\text{ROWRES1}}$	191	2866.0	865.7
$\overline{\text{ROWRES2}}$	192	2710.0	865.7
R1F	193	2546.0	865.7
SW1	194	2214.0	865.7
SW2	195	2050.0	865.7
T1	196	1894.0	865.7
T2	197	1730.0	865.7
T3	198	1574.0	865.7
T4	199	1410.0	865.7
T5	200	1254.0	865.7

SYMBOL	PAD	x	y
V_{SS}	201	1139.0	865.7
V_{SS}	202	1064.0	865.7
V_{SS}	203	989.0	865.7
V_{SS}	204	865.0	865.7
V_{SS}	205	790.0	865.7
V_{SS}	206	661.5	865.7
V_{SS}	207	586.5	865.7
V_{DD}	208	326.7	865.7
V_{DD}	209	251.7	865.7
V_{DD}	210	176.7	865.7
V_{DD}	211	101.7	865.7
V_{DD}	212	26.7	865.7
V_{DD}	213	−48.3	+865.7
V_{DD}	214	−123.3	+865.7
V_M	215	−882.9	+865.7
V_M	216	−957.9	+865.7
V_M	217	−1032.9	+865.7
V_M	218	−1107.9	+865.7
V_M	219	−1182.9	+865.7
V_M	220	−1257.9	+865.7
V_M	221	−1332.9	+865.7
V_{MH}	222	−1630.7	+865.7
V_{MH}	223	−1705.7	+865.7
V_{MH}	224	−1780.7	+865.7
V_{MH}	225	−1855.7	+865.7
V_{MH}	226	−1930.7	+865.7
V_{MH}	227	−2005.7	+865.7
V_{MH}	228	−2080.7	+865.7
V_H	229	−2334.3	+865.7
V_H	230	−2409.3	+865.7
V_H	231	−2484.3	+865.7
V_H	232	−2559.3	+865.7
V_H	233	−2634.3	+865.7
V_H	234	−2709.3	+865.7
V_H	235	−2784.3	+865.7
V_L	236	−3013.5	+865.7
V_L	237	−3088.5	+865.7
V_L	238	−3163.5	+865.7
V_L	239	−3238.5	+865.7
V_L	240	−3313.5	+865.7
V_L	241	−3388.5	+865.7

SYMBOL	PAD	x	y
V_L	242	–3463.5	+865.7
Dummy	243	–3728.5	+865.7
Dummy	244	–3803.5	+865.7
Dummy	245	–3878.5	+865.7
Dummy	246	–3953.5	+865.7
Dummy	247	–4103.5	+865.7
Dummy	248	–4178.5	+865.7
Dummy	249	–4253.5	+865.7
Dummy	250	–4328.5	+865.7
Dummy	251	–4403.5	+865.7
Dummy	252	–4478.5	+865.7
Dummy	253	–4553.5	+865.7
Dummy	254	–4628.5	+865.7
Dummy	255	–4703.5	+865.7
Dummy	256	–4778.5	+865.7
Dummy	257	–4853.5	+865.7
Dummy	258	–4928.5	+865.7
Dummy	259	–5003.5	+865.7
Dummy	260	–5078.5	+865.7
Dummy	261	–5153.5	+865.7
Dummy	262	–5228.5	+865.7
Dummy	263	–5303.5	+865.7
Dummy	264	–5378.5	+865.7
Dummy	265	–5453.5	+865.7
Dummy	266	–5528.5	+865.7
Dummy	267	–5603.5	+865.7
Dummy	268	–5678.5	+865.7
Dummy	269	–5753.5	+865.7
Dummy	270	–5978.5	+865.7
Dummy	271	–6053.5	+865.7
Dummy	272	–6128.5	+865.7
Alignment marks (see Fig.12)			
Alignment circle 1		5909.0	865.7
Alignment circle 2		–5866.0	+865.7

Table 4 Bonding pad dimensions

PAD	SIZE	UNIT
Minimum pad pitch	75	µm
Pad size; aluminium	tbf	µm
Bump dimensions	$50 \times 80 \times 17.5$ (±5)	µm
Wafer thickness (excluding bumps)	381	µm

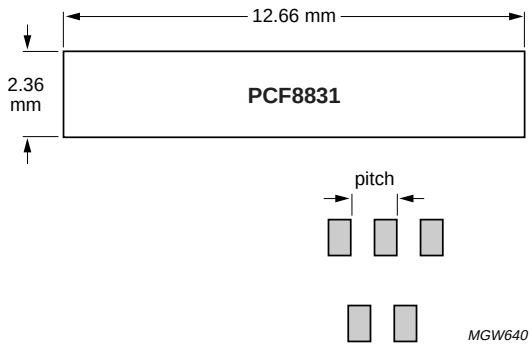


Fig.11 Bonding pads.

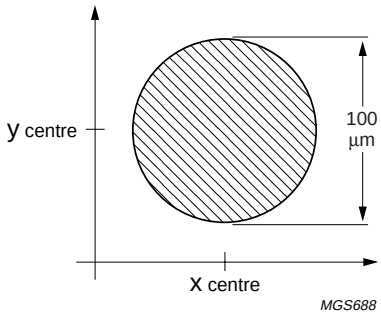
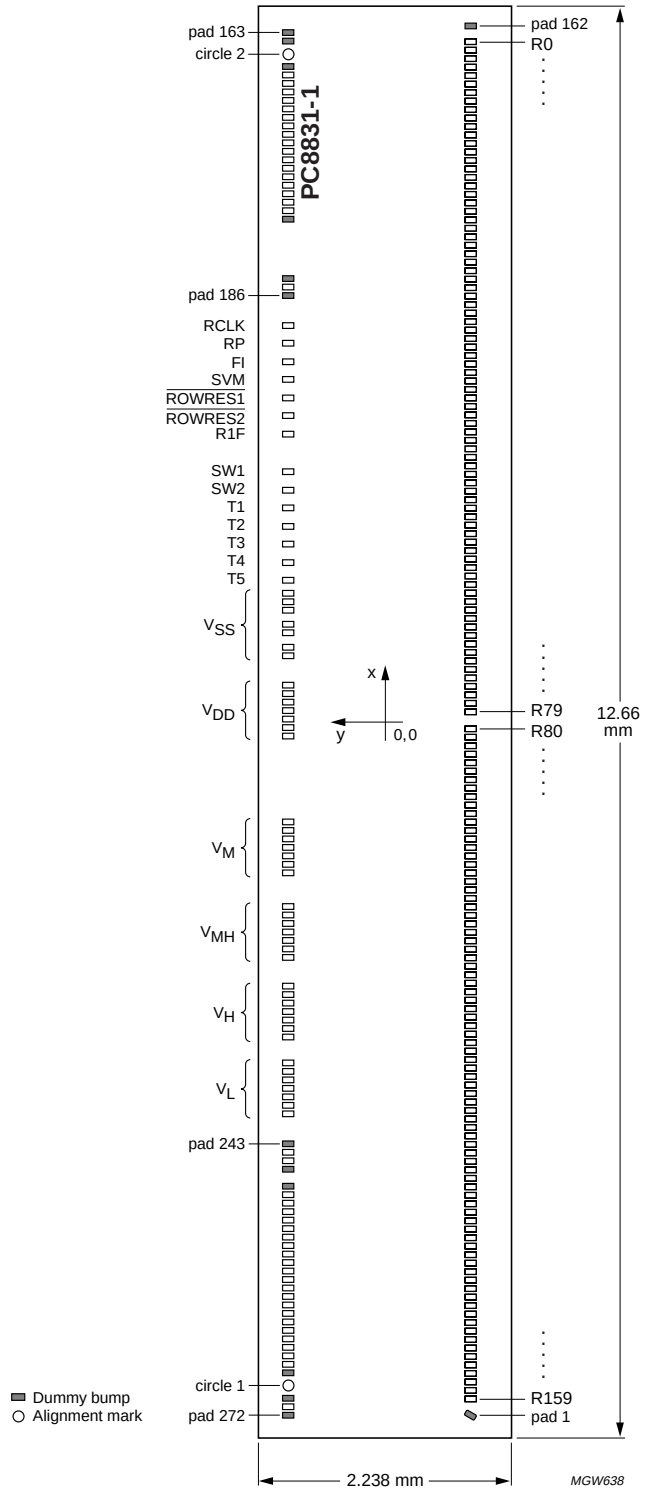


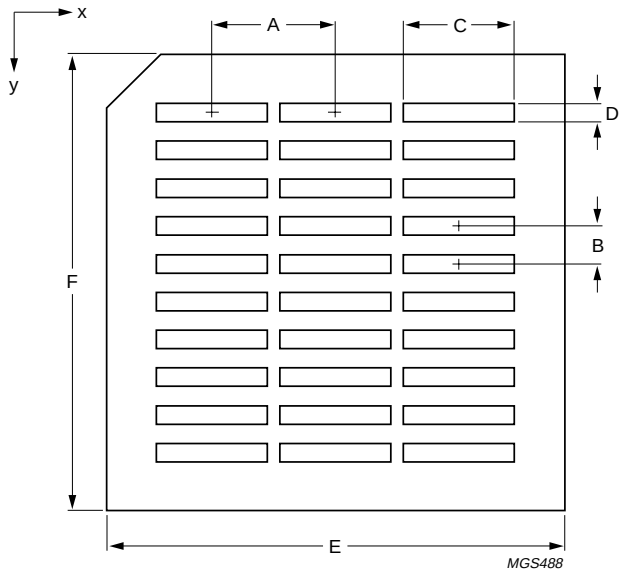
Fig.12 Alignment mark detail.



Circles 1 and 2 are alignment marks (see Fig.12).

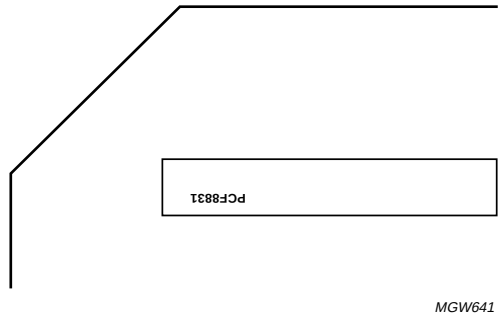
Fig.13 Bonding pad location.

15 TRAY INFORMATION



The dimensions are given in Table 5.

Fig.14 Tray details.



The orientation of the IC in a pocket is indicated by the position of the IC type name on the die surface with respect to the chamfer on the upper left corner of the tray. Refer to the bonding pad location diagram for the orientation and position of the type name on the die surface.

Fig.15 Tray alignment.

Table 5 Tray dimensions

DIMENSIONS	DESCRIPTION	VALUE
A	pocket pitch, x direction	14.86 mm
B	pocket pitch, y direction	4.45 mm
C	pocket width, x direction	12.76 mm
D	pocket width, y direction	2.34 mm
E	tray width, x direction	50.8 mm
F	tray width, y direction	50.8 mm
–	number of pockets in x direction	3
–	number of pockets in y direction	10

16 DATA SHEET STATUS

DATA SHEET STATUS[1]	PRODUCT STATUS[2]	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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