

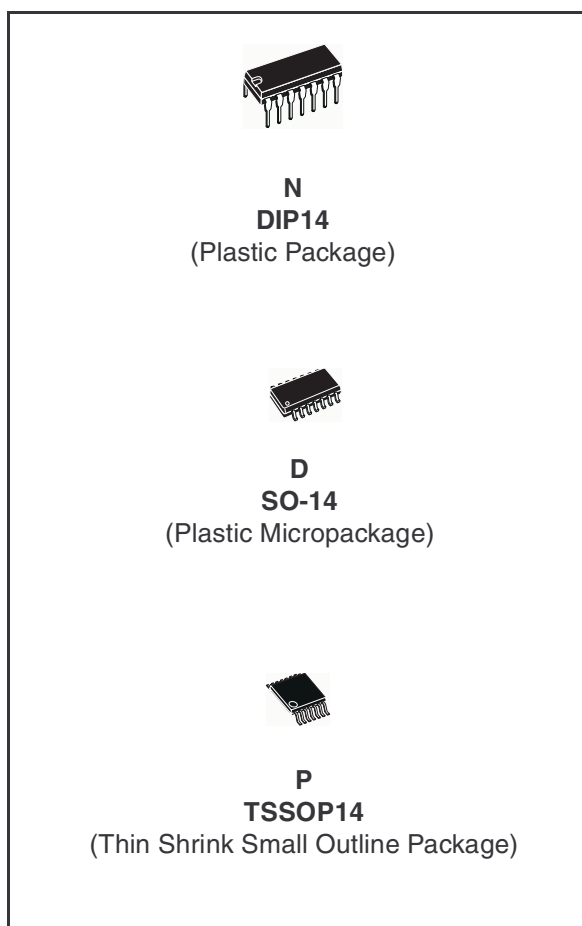
## Low Power Quad Voltage Comparator

- Wide single supply voltage range or dual supplies for all devices: +2V to +36V or  $\pm 1V$  to  $\pm 18V$
- Very low supply current (1.1mA) independent of supply voltage (1.4mW/comparator at +5V)
- Low input bias current: 25nA typ.
- Low input offset current:  $\pm 5nA$  typ.
- Input common-mode voltage range includes ground
- Low output saturation voltage: 250mV typ. ( $I_O = 4mA$ )
- Differential input voltage range equal to the supply voltage
- TTL, DTL, ECL, MOS, CMOS compatible outputs

### Description

This device consists of four independent precision voltage comparators. All these comparators were designed specifically to operate from a single supply over a wide range of voltages. Operation from split power supplies is also possible.

These comparators also have a unique characteristic in that the input common-mode voltage range includes ground even though operated from a single power supply voltage



### Order Codes

Part Number	Temperature Range	Package	Packaging	Marking
LM2901N	-40°C, +125°C	DIP14	Tube	LM2901N
LM2901D/LM2901DT		SO-14	Tube or Tape & Reel	2901
LM2901PT		TSSOP14 (Thin Shrink Outline Package)	Tape & Reel	2901
LM2901YD/YDT		SO-14 (automotive grade level)	Tube or Tape & Reel	2901Y

# 1 Absolute Maximum Ratings

**Table 1. Key parameters and their absolute maximum ratings**

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply Voltage	±18 to 36	V
V <sub>ID</sub>	Differential Input Voltage	±36	V
V <sub>I</sub>	Input Voltage	-0.3 to +36	V
	Output Short-circuit to Ground <sup>(1)</sup>		
P <sub>d</sub>	Power Dissipation <sup>(2)</sup> DIP14 SO-14 TSSOP14	1500 830 710	mW
T <sub>J</sub>	Junction Temperature	+150	°C
T <sub>stg</sub>	Storage Temperature Range	-65 to +150	°C
ESD	HBM: Human Body Model <sup>(3)</sup>	1.5	Kv
	MM: Machine Model <sup>(4)</sup>	100	V
	CDM: Charged Device Model	1500	V

- Short-circuit from the output to V<sub>CC</sub><sup>+</sup> can cause excessive heating and eventual destruction. The maximum output current is approximately 20mA, independent of the magnitude of V<sub>CC</sub><sup>+</sup>
- P<sub>d</sub> is calculated with T<sub>amb</sub> = +25°C, T<sub>j</sub> = +150°C and  
 R<sub>thja</sub> = 80°C/W for DIP14 package  
 R<sub>thja</sub> = 150°C/W for SO-14 package  
 R<sub>thja</sub> = 175°C/W for TSSOP14 package
- Human body model, 100pF discharged through a 1.5kΩ resistor into pin of device.
- Machine model ESD, a 200pF cap is charged to the specified voltage, then discharged directly into the IC with no external series resistor (internal resistor < 5Ω), into pin to pin of device.

**Table 2. Operating conditions**

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply Voltage	2 to 32 ±1 to ±16	V
V <sub>icm</sub>	Common Mode Input Voltage Range	0 to (V <sub>CC</sub> <sup>+</sup> - 1.5)	V
T <sub>oper</sub>	Operating Free-Air Temperature range	-40 to +125	°C

## 2 Typical Application Schematics

Figure 1. Schematic diagram (1/4 LM2901)

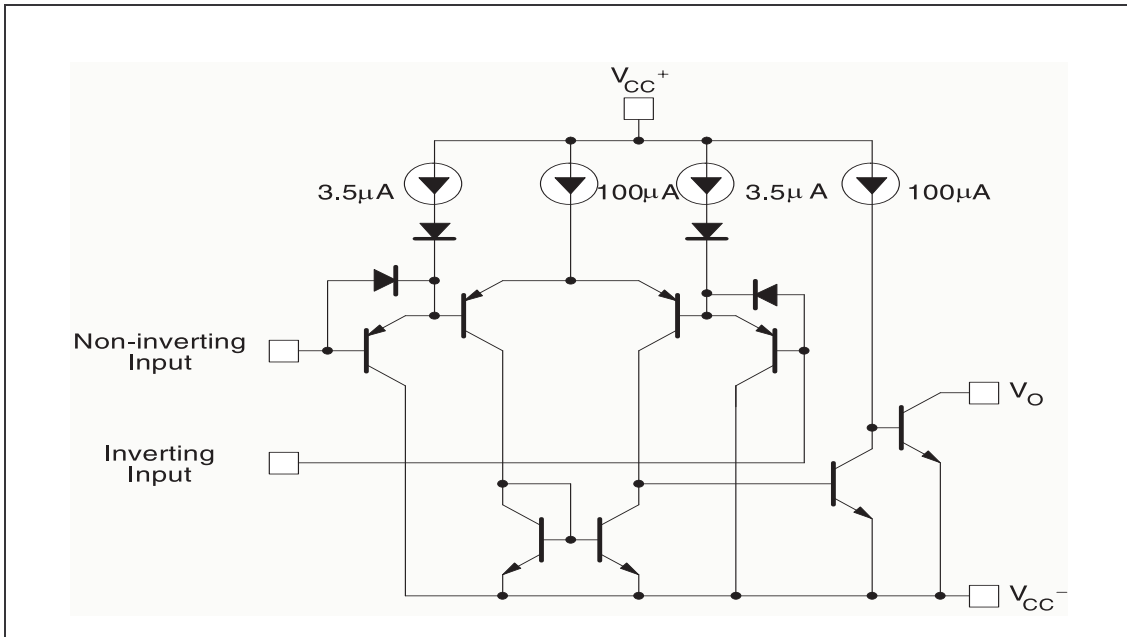
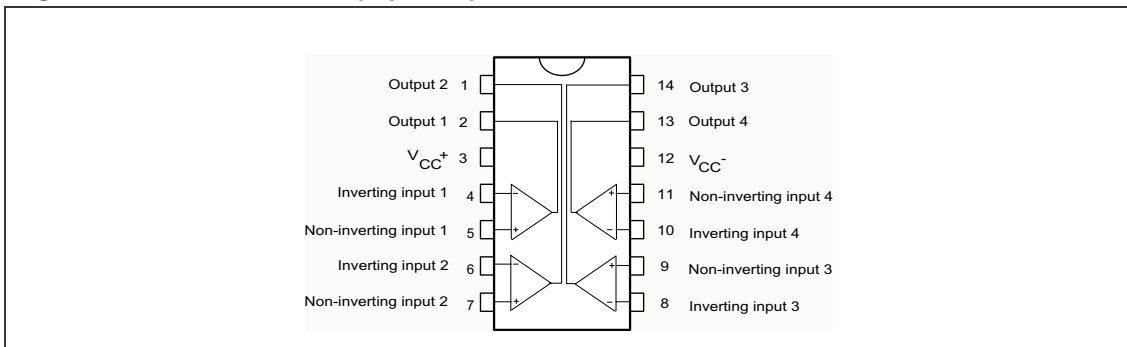


Figure 2. Pin connection (top view)



### 3 Electrical Characteristics

Table 3.  $V_{CC}^+ = 5V$ ,  $V_{CC}^- = GND$ ,  $T_{amb} = 25^\circ C$  (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{io}$	Input Offset Voltage <sup>(1)</sup> $T_{amb} = +25^\circ C$ $T_{min} \leq T_{amb} \leq T_{max}$ .		1	7 15	mV
$I_{io}$	Input Offset Current $T_{amb} = +25^\circ C$ $T_{min} \leq T_{amb} \leq T_{max}$ .		5	50 150	nA
$I_{ib}$	Input Bias Current ( $I_{I^+}$ or $I_{I^-}$ ) <sup>(2)</sup> $T_{amb} = 2.5V$ $T_{min} \leq T_{amb} \leq T_{max}$ .		25	250 400	nA
$A_{vd}$	Large Signal Voltage Gain ( $V_{CC} = 15V, R_L = 15k\Omega, V_o = 1$ to $11V$ )	25	200		V/mV
$I_{cc}$	Supply Current (all comparators) $V_{CC} = +5V$ , no load $V_{CC} = +30V$ , no load		1.1 1.3	2 2.5	mA
$V_{icm}$	Input Common Mode Voltage Range ( $V_{CC} = 30V$ ) <sup>(3)</sup> $T_{amb} = +25^\circ C$ $T_{min} \leq T_{amb} \leq T_{max}$ .	0 0		$V_{CC}^+ - 1.5$ $V_{CC}^+ - 2$	V
$V_{id}$	Differential Input Voltage <sup>(4)</sup>			$V_{CC}^+$	V
$V_{OL}$	Low Level Output Voltage $V_{id} = -1V, I_{sink} = 4mA$ $T_{amb} = +25^\circ C$ $T_{min} \leq T_{amb} \leq T_{max}$		250	400 700	mV
$I_{oh}$	High Level Output Current ( $V_{CC} = V_o = 30V, V_{id} = 1V$ ) $T_{amb} = +25^\circ C$ $T_{min} \leq T_{amb} \leq T_{max}$		0.1	1	nA $\mu A$
$I_{sink}$	Output Sink Current ( $V_{id} = -1V, V_o = 1.5V$ )	6	16		mA
$t_{re}$	Small Signal Response Time <sup>(5)</sup> ( $R_L = 5.1k\Omega$ connected to $V_{CC}^+$ )		1.3		$\mu s$
$t_{rel}$	Large Signal Response Time <sup>(6)</sup> TTL Input ( $V_{ref} = +1.4V, R_L = 5.1k\Omega$ to $V_{CC}^+$ ) Output Signal at 50% of final value Output Signal at 95% of final value			500 1	ns $\mu s$

1. At output switch point,  $V_o \approx 1.4V$ ,  $R_S = 0$  with  $V_{CC}^+$  from 5V to 30V, and over the full input common-mode range (0V to  $V_{CC}^+ - 1.5V$ ).
2. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading charge exists on the reference of input lines
3. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is  $V_{CC}^+ - 1.5V$ , but either or both inputs can go to +30V without damage.
4. The response time specified is for a 100mV input step with 5mV overdrive.
5. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than -0.3V (or 0.3V below the negative power supply, if used)
6. Maximum values are guaranteed by design.

Figure 3. Supply current versus supply voltage

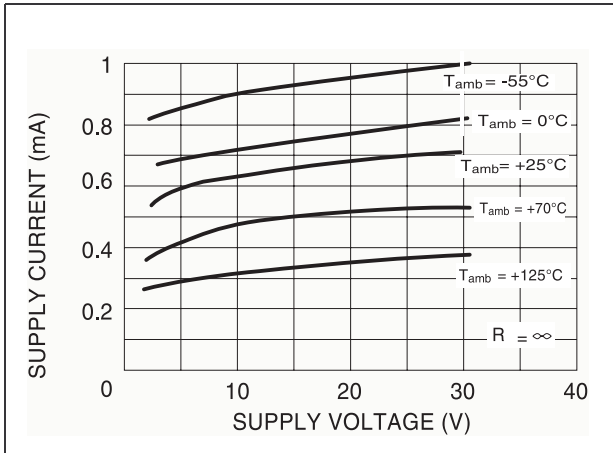


Figure 4. Input current versus supply voltage

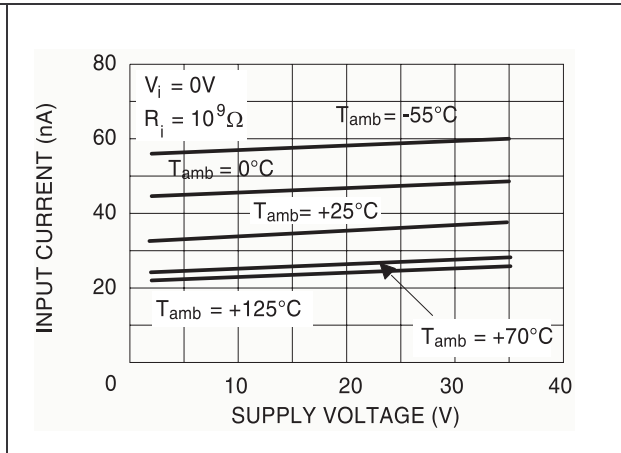


Figure 5. Output saturation voltage versus output current

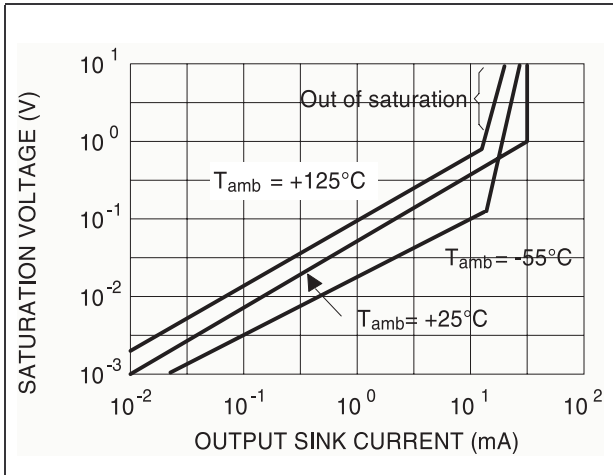


Figure 6. Response time for various input overdrives - negative transition

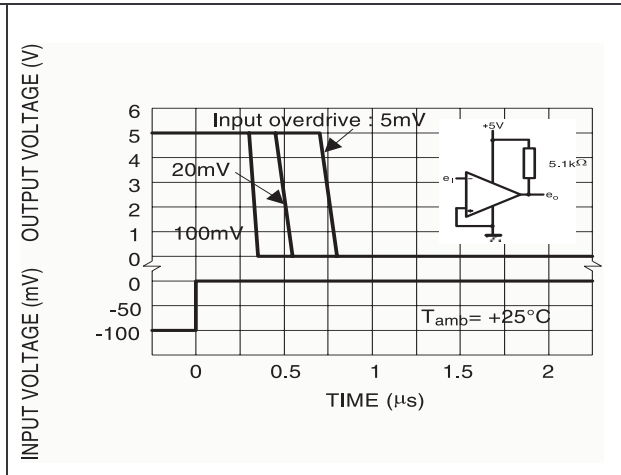
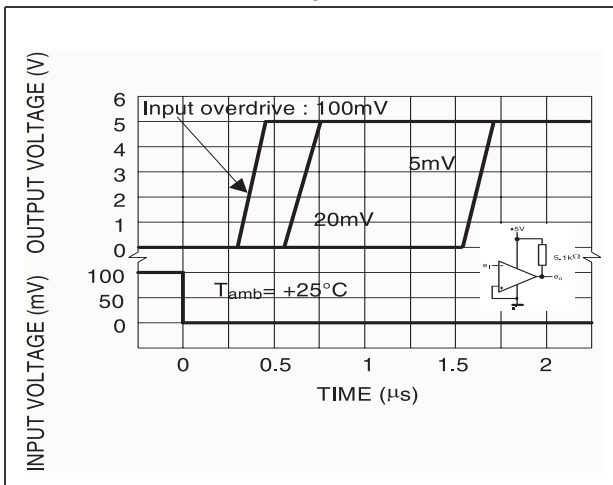


Figure 7. Response time for various input overdrives - positive transition



# 4 Typical Applications

Figure 8. Basic comparator

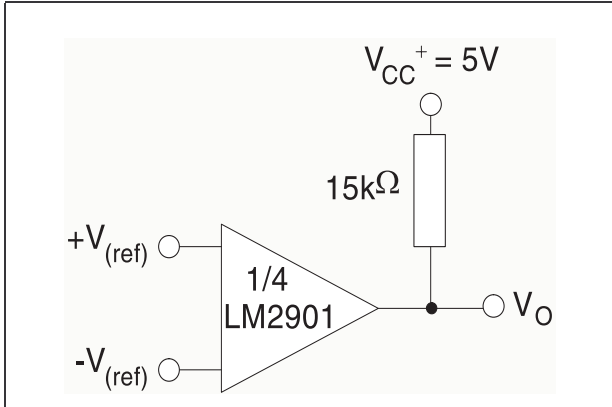


Figure 9. Driving CMOS

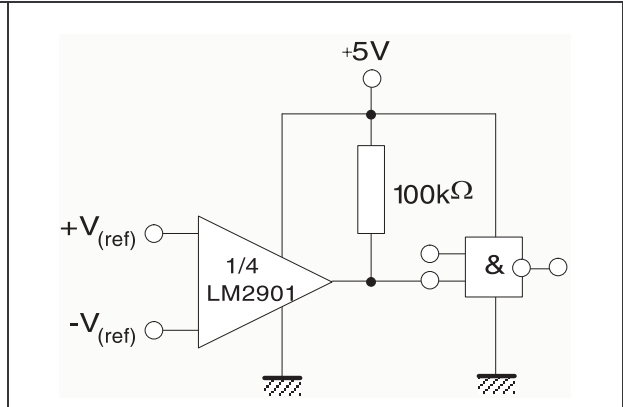


Figure 10. Driving TTL

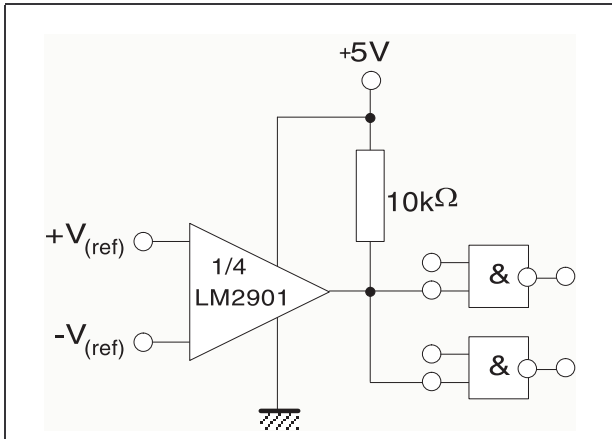


Figure 11. Low frequency op-amp

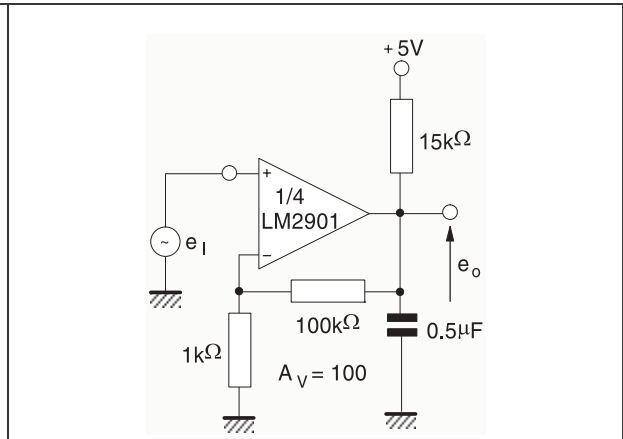


Figure 12. Low frequency op-amp

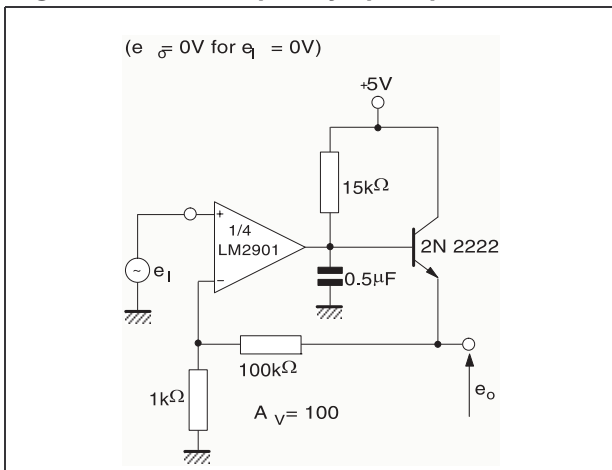


Figure 13. Transducer amplifier

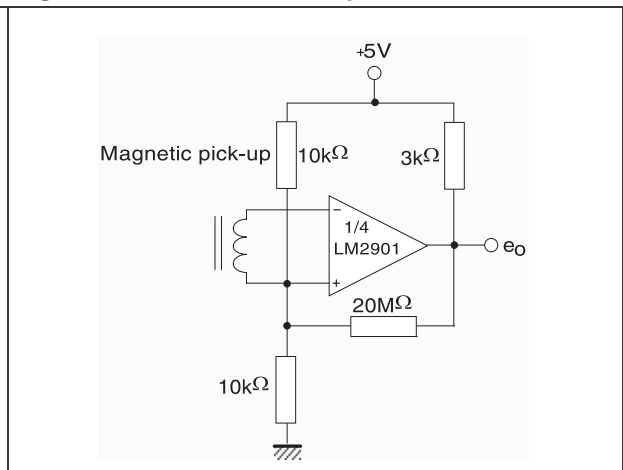


Figure 14. Low frequency op- amp with offset adjust

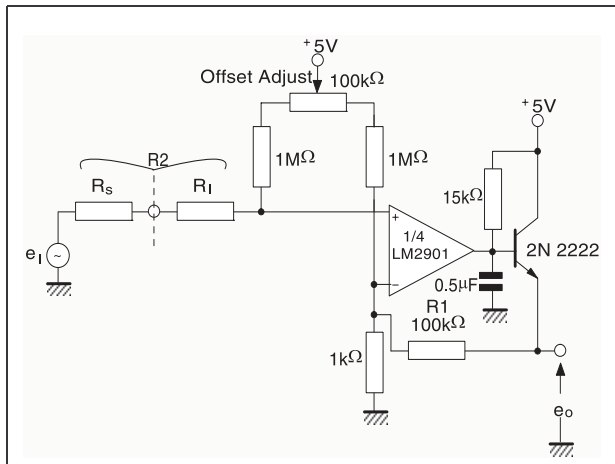


Figure 15. Zero crossing detector (single power supply)

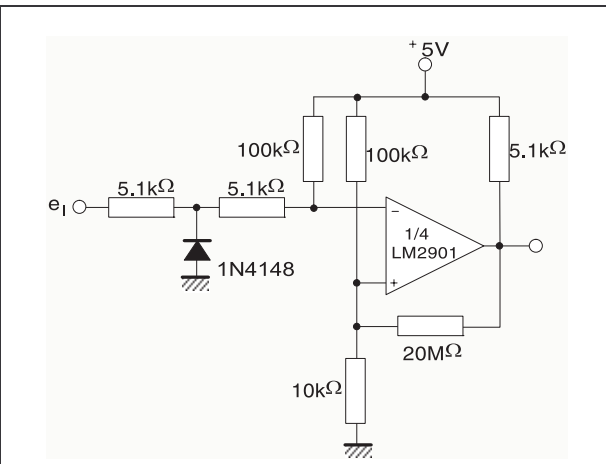


Figure 16. Limit comparator

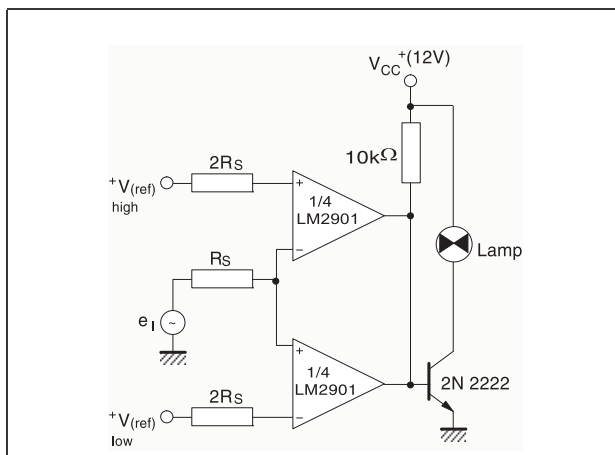


Figure 17. Split-supply applications - zero crossing detector

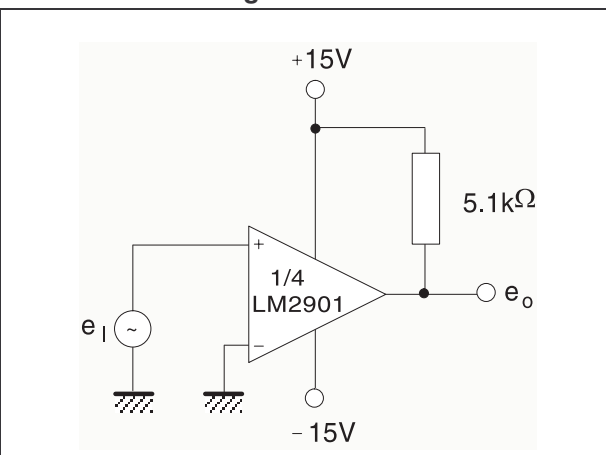


Figure 18. Crystal controlled oscillator

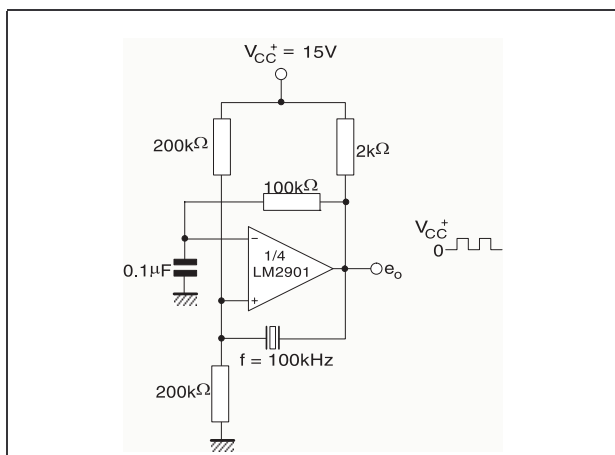


Figure 19. Comparator with a negative reference

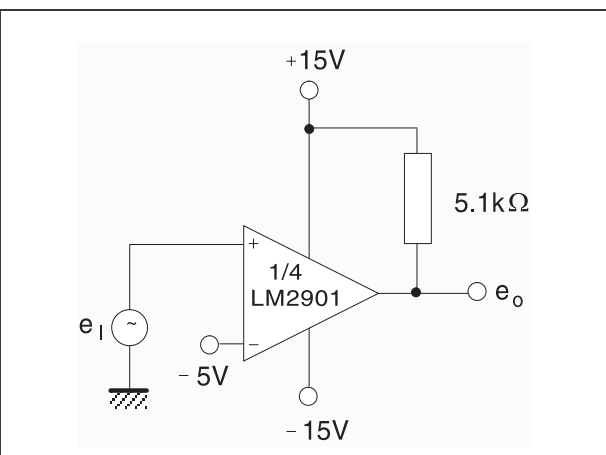


Figure 20. Time delay generator

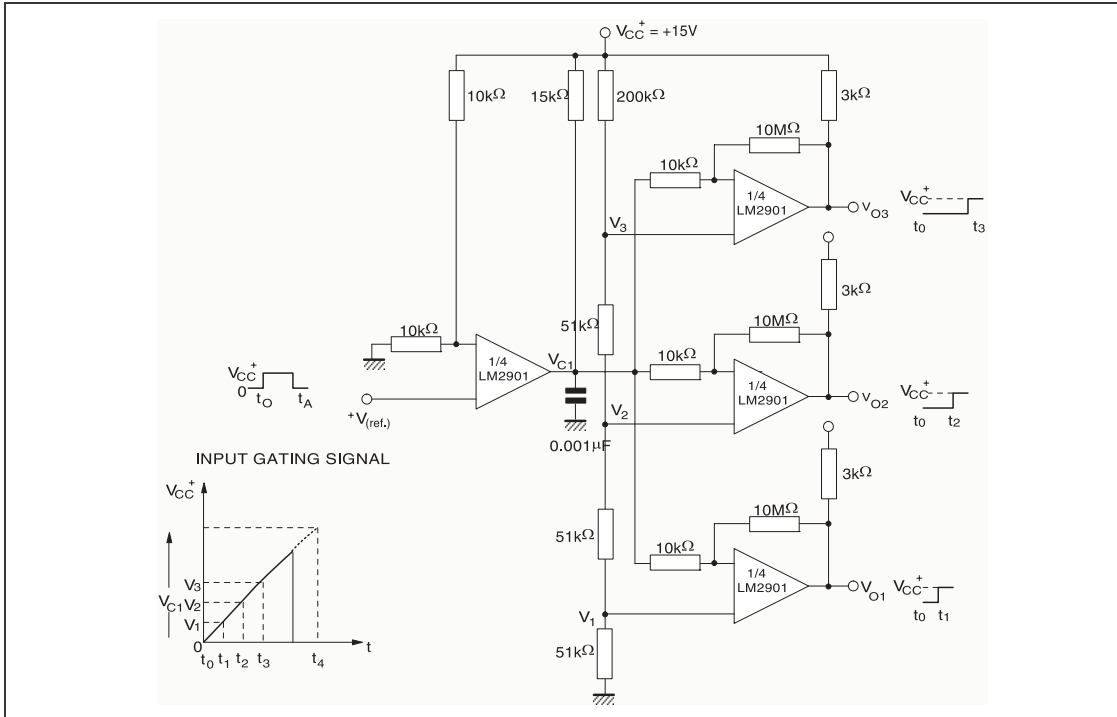
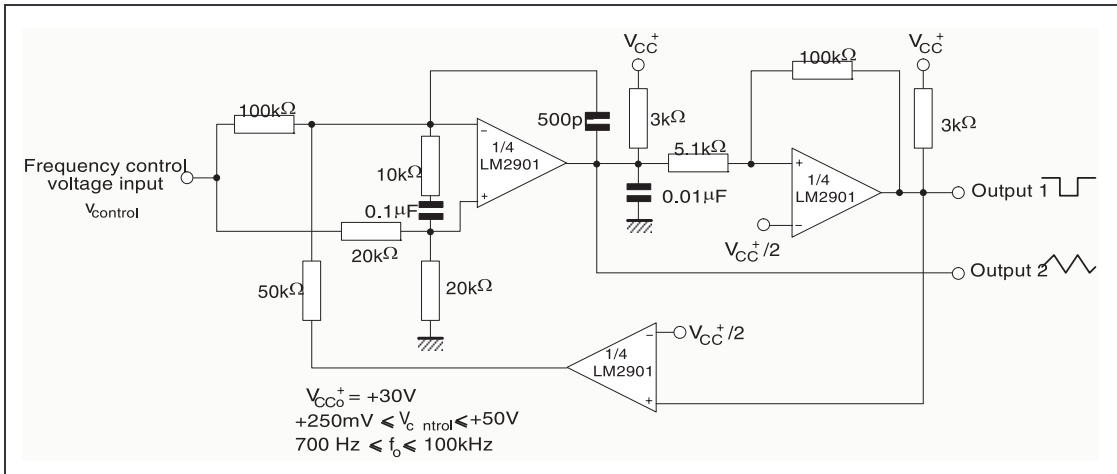


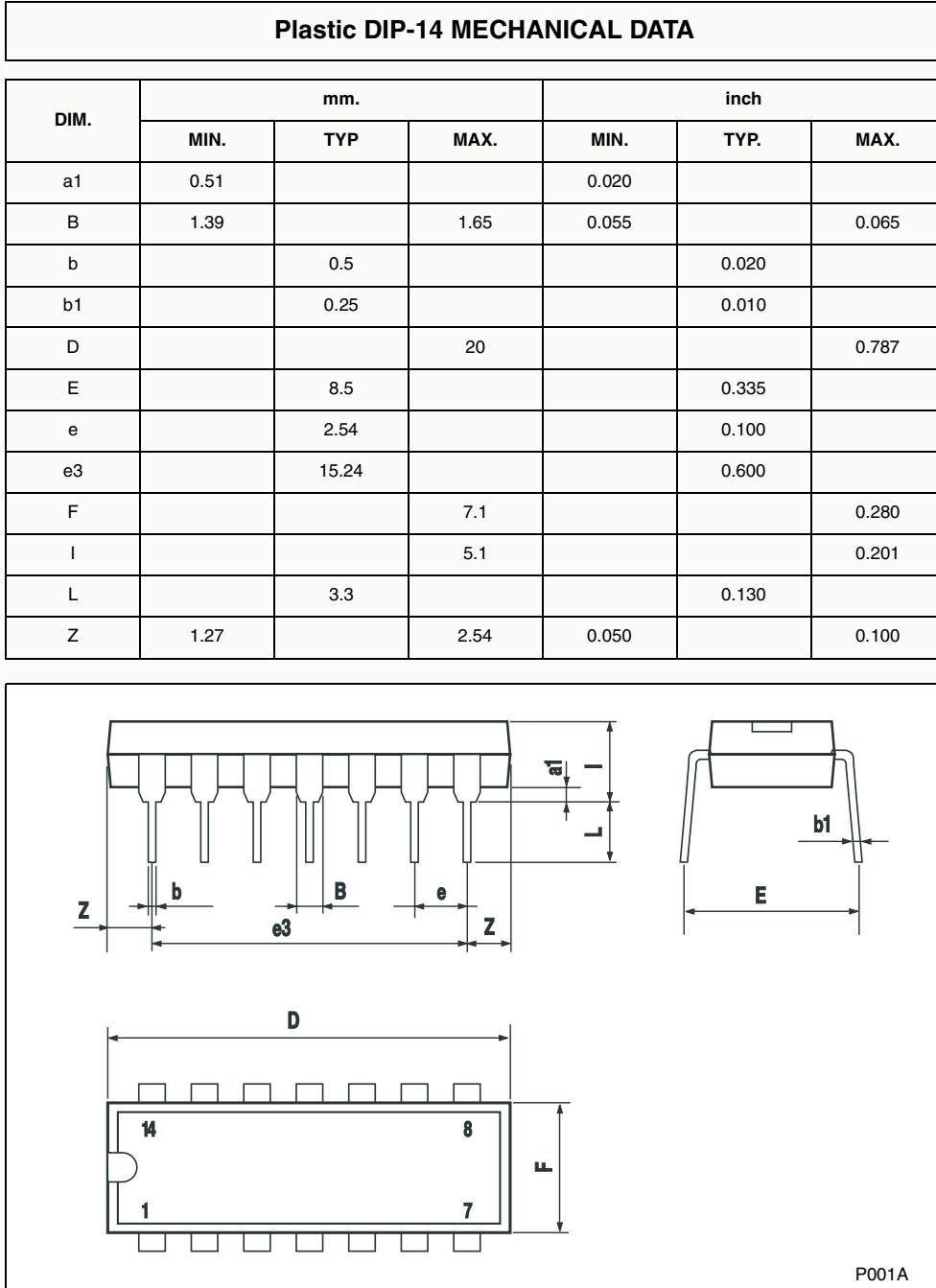
Figure 21. Two-decade high-frequency VCO





## 5 PACKAGE MECHANICAL DATA

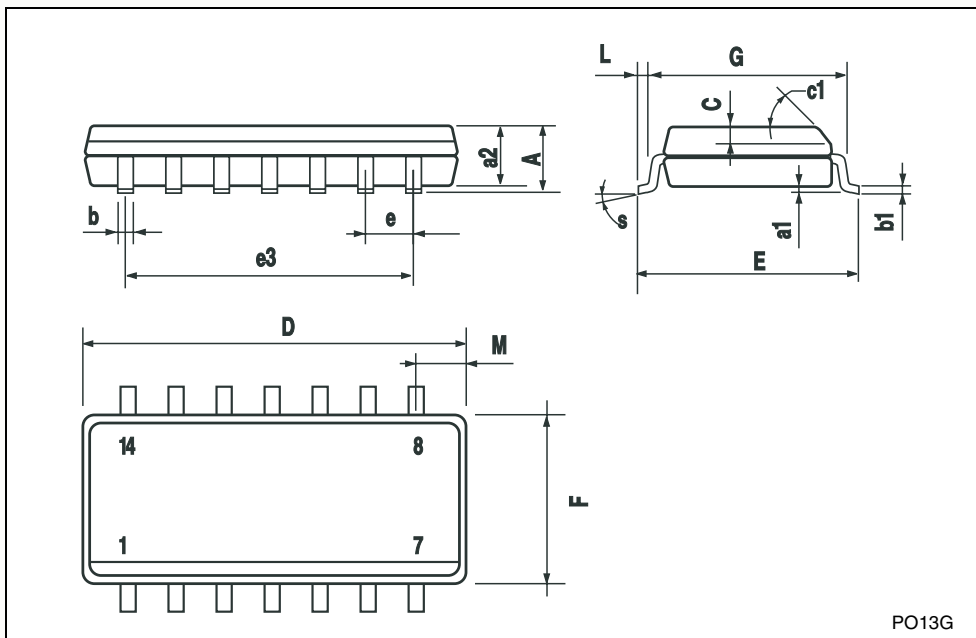
### 5.1 DIP14 package



5.2 SO-14 package

SO-14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8° (max.)					

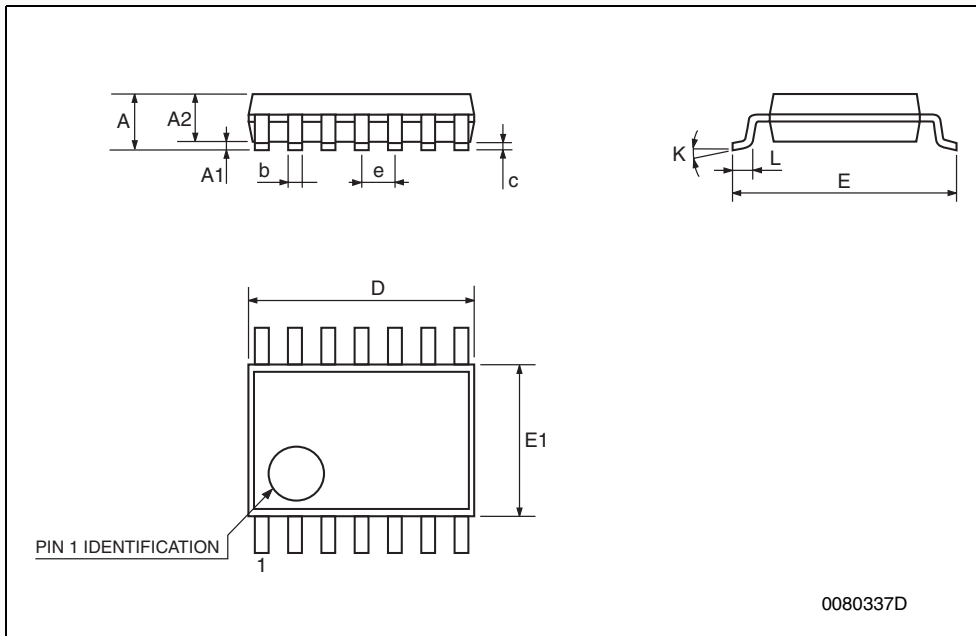


PO13G

5.3 TSSOP14 package

TSSOP14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



## 6 Revision History

Date	Revision	Changes
Jan. 2002	1	Initial release.
July 2005	2	1 - PPAP references inserted in the datasheet see <i>Table : Order Codes on page 1</i> . 2 - ESD protection inserted in <i>Table 1 on page 2</i> .

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