

# HAT2050T

Silicon N Channel Power MOS FET  
High Speed Power Switching

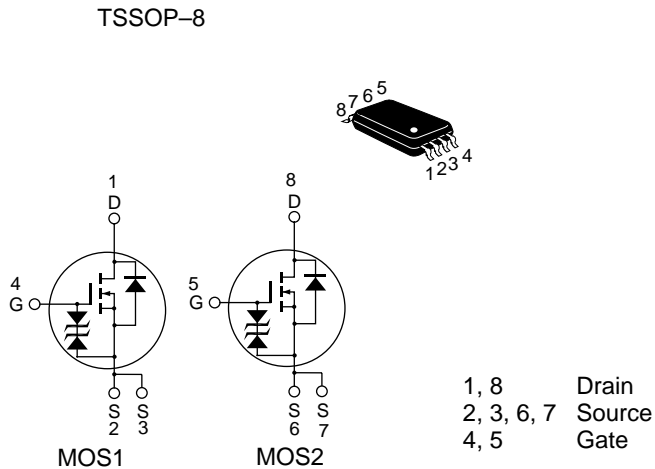
# HITACHI

ADE-208-660A (Z)  
2nd. Edition  
February 1999

## Features

- Low on-resistance
- Capable of 4 V gate drive
- Low drive current
- High density mounting

## Outline



## Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	100	V
Gate to source voltage	$V_{GSS}$	$\pm 20$	V
Drain current	$I_D$	1	A
Drain peak current	$I_{D(pulse)}$ <sup>Note1</sup>	4	A
Body-drain diode reverse drain current	$I_{DR}$	1	A
Channel dissipation	Pch <sup>Note2</sup>	1.0	W
Channel dissipation	Pch <sup>Note3</sup>	1.5	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	- 55 to + 150	°C

Note: 1.  $PW \leq 10\mu s$ , duty cycle  $\leq 1\%$

2. 1 Drive operation : When using the glass epoxy board (FR4 40 x 40 x 1.6 mm),  $PW \leq 10s$

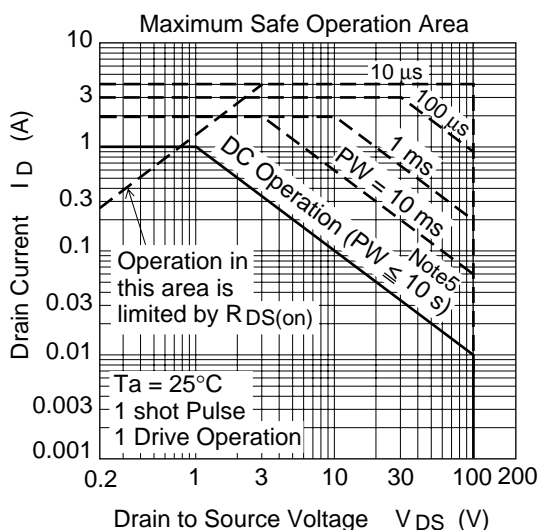
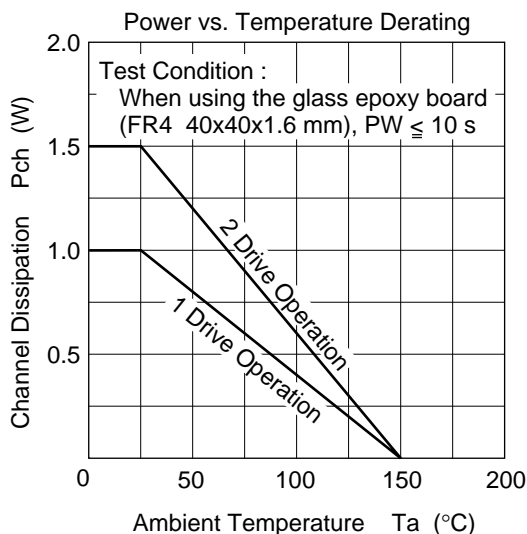
3. 2 Drive operation : When using the glass epoxy board (FR4 40 x 40 x 1.6 mm),  $PW \leq 10s$

## Electrical Characteristics (Ta = 25°C)

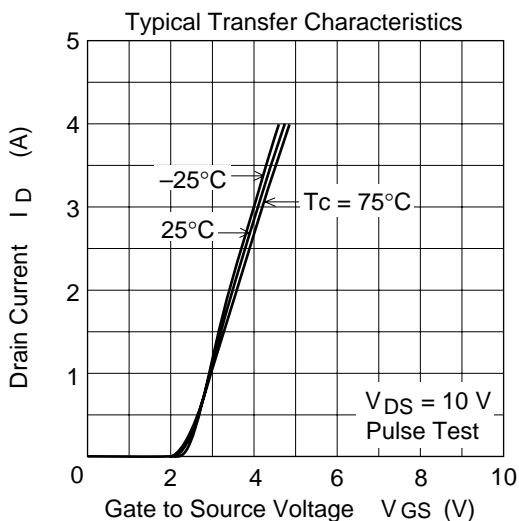
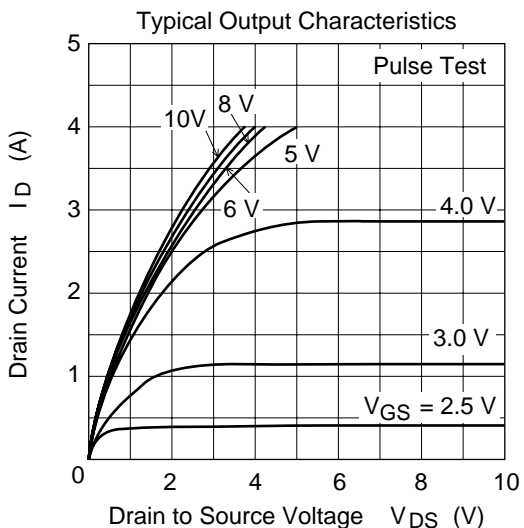
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	100	—	—	V	$I_D = 10\text{ mA}$ , $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	$\pm 20$	—	—	V	$I_G = \pm 100\ \mu A$ , $V_{DS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 10$	$\mu A$	$V_{GS} = \pm 16\text{ V}$ , $V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	1	$\mu A$	$V_{DS} = 100\text{ V}$ , $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.3	—	2.3	V	$V_{DS} = 10\text{ V}$ , $I_D = 1\text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.56	0.75	$\Omega$	$I_D = 0.5\text{ A}$ , $V_{GS} = 10\text{ V}$ <sup>Note4</sup>
	$R_{DS(on)}$	—	0.72	1.0	$\Omega$	$I_D = 0.5\text{ A}$ , $V_{GS} = 4\text{ V}$ <sup>Note4</sup>
Forward transfer admittance	$ y_{fs} $	0.7	1.1	—	S	$I_D = 0.5\text{ A}$ , $V_{DS} = 10\text{ V}$ <sup>Note4</sup>
Input capacitance	Ciss	—	90	—	pF	$V_{DS} = 10\text{ V}$
Output capacitance	Coss	—	42	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss	—	20	—	pF	$f = 1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	11	—	ns	$V_{GS} = 4\text{ V}$ , $I_D = 0.5\text{ A}$
Rise time	$t_r$	—	24	—	ns	$V_{DD} \cong 10\text{ V}$
Turn-off delay time	$t_{d(off)}$	—	14	—	ns	
Fall time	$t_f$	—	11	—	ns	
Body-drain diode forward voltage	$V_{DF}$	—	0.84	1.1	V	$I_F = 1\text{ A}$ , $V_{GS} = 0$ <sup>Note4</sup>
Body-drain diode reverse recovery time	$t_{rr}$	—	85	—	ns	$I_F = 1\text{ A}$ , $V_{GS} = 0$ $diF/dt = 20\text{ A}/\mu s$

Note: 4. Pulse test

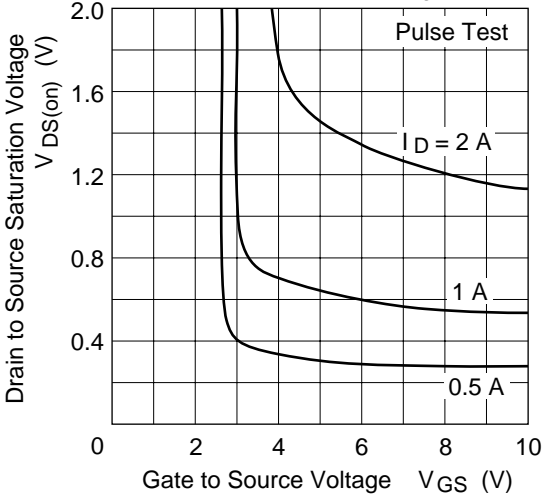
Main Characteristics



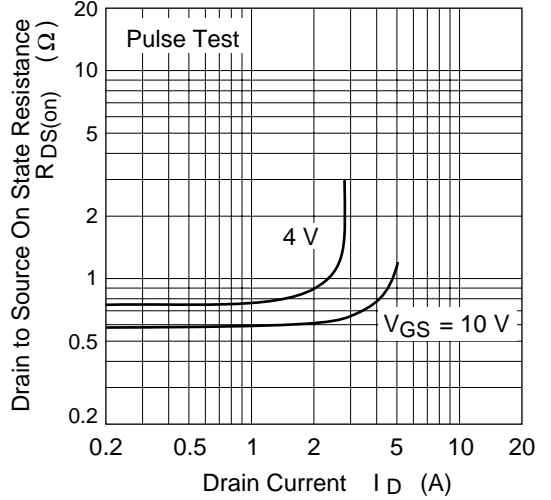
Note 5 :  
When using the glass epoxy board  
(FR4 40x40x1.6 mm)



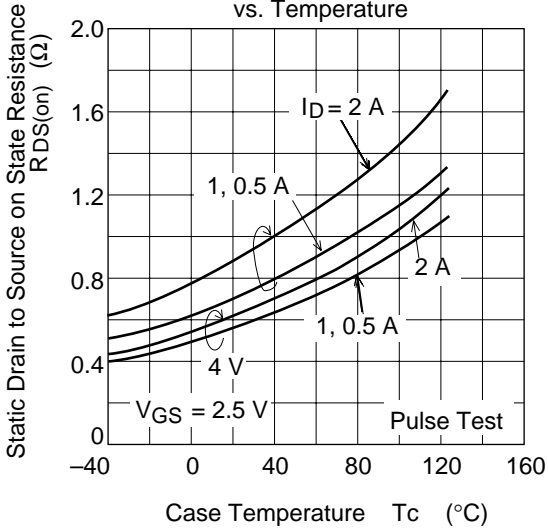
Drain to Source Saturation Voltage vs. Gate to Source Voltage



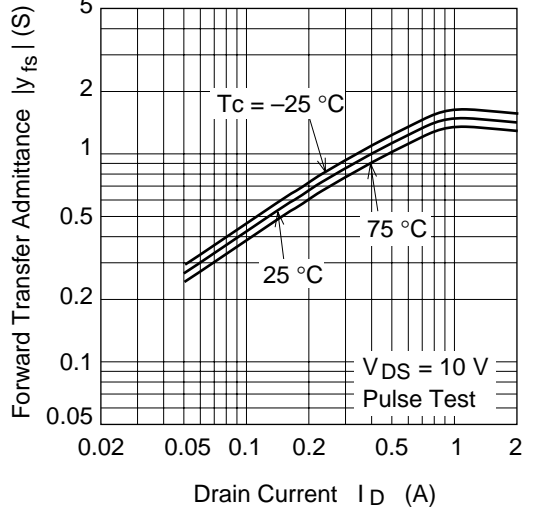
Static Drain to Source on State Resistance vs. Drain Current

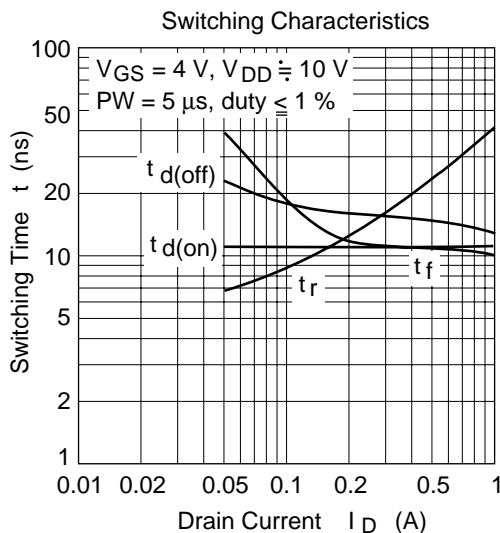
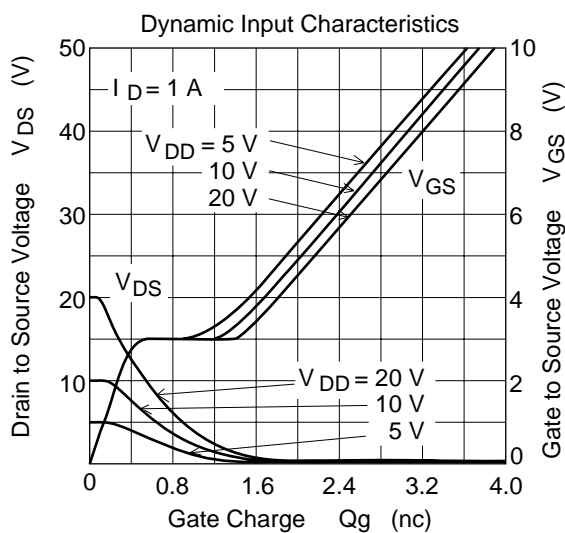
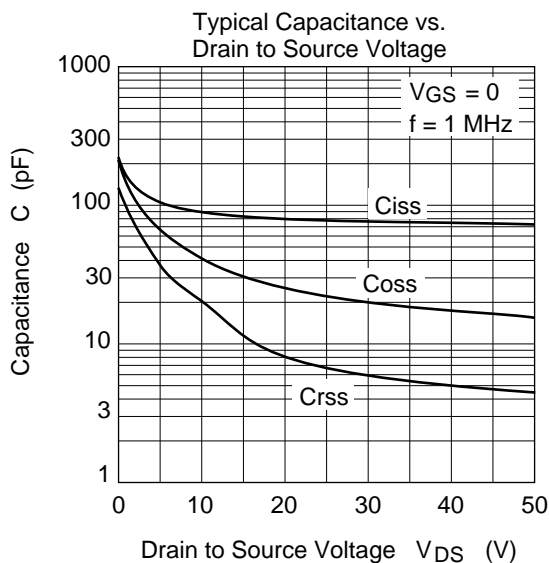
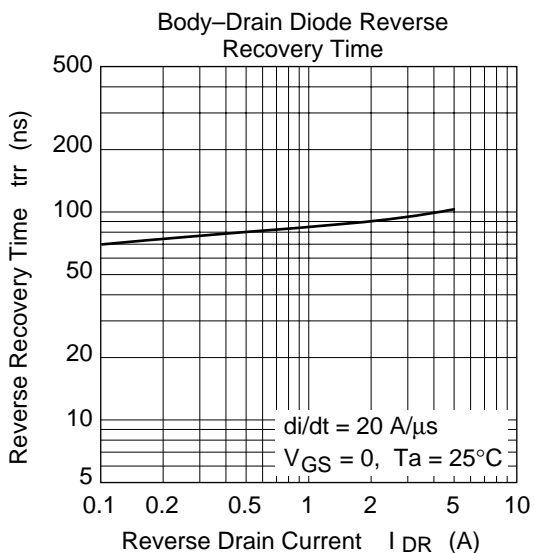


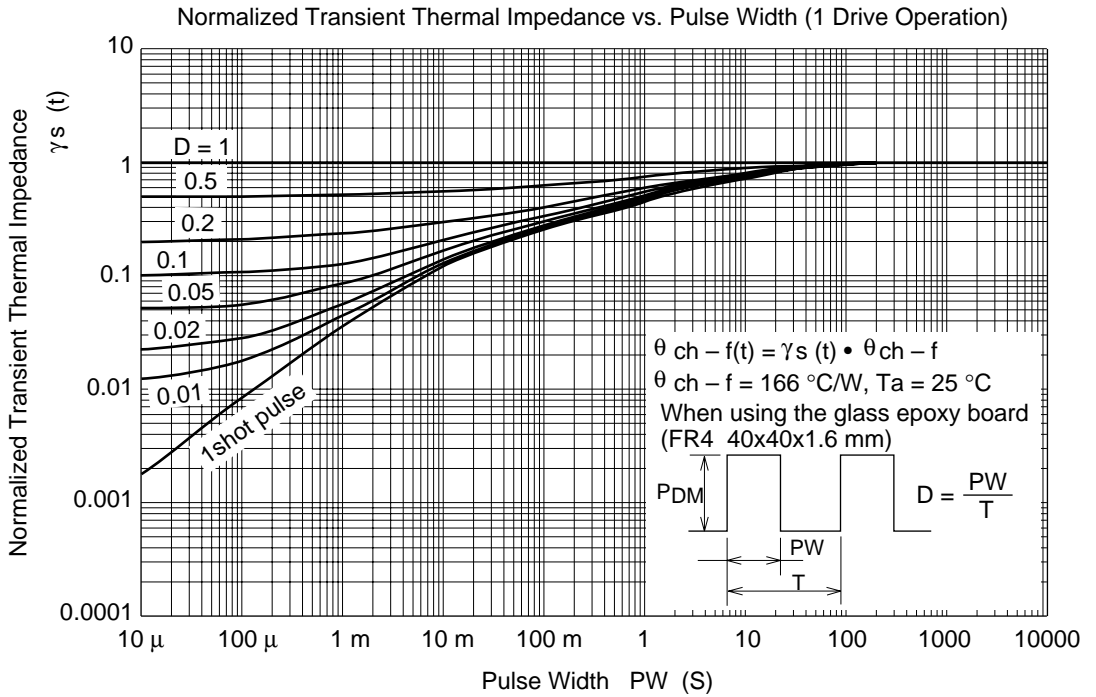
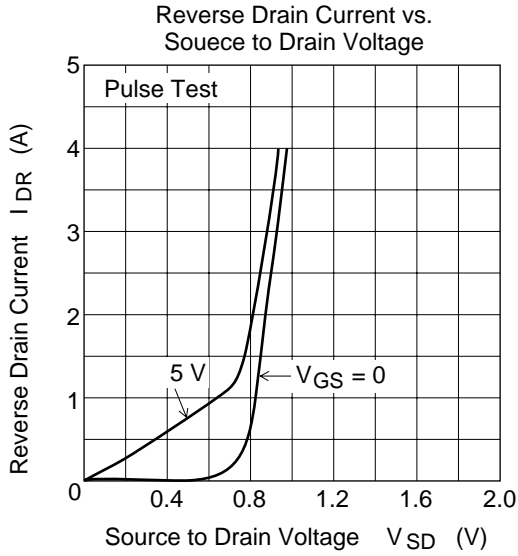
Static Drain to Source on State Resistance vs. Temperature

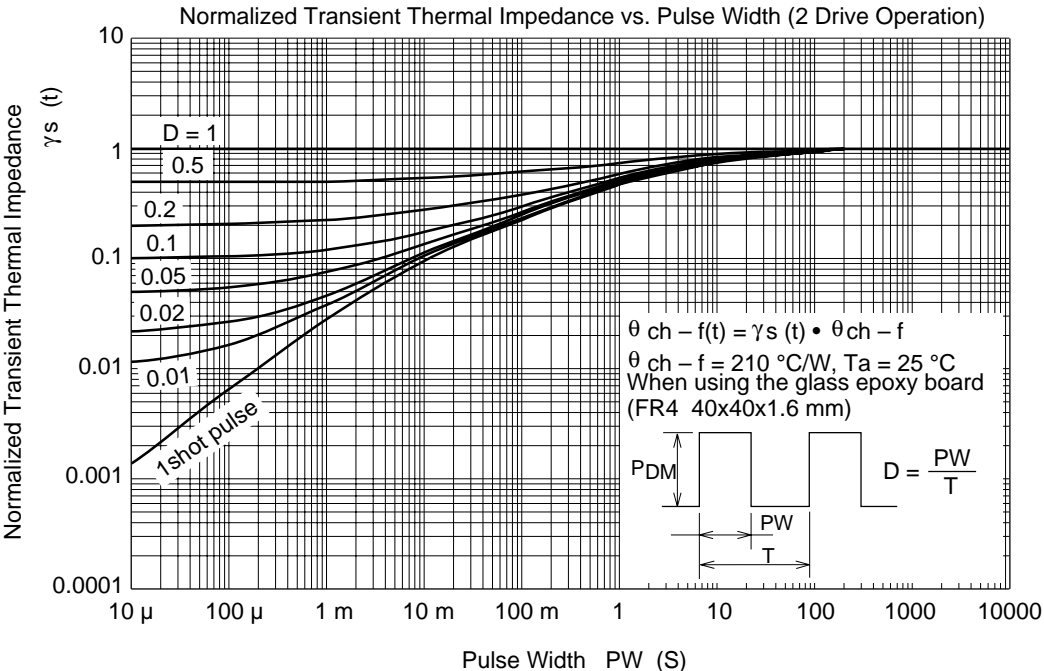


Forward Transfer Admittance vs. Drain Current

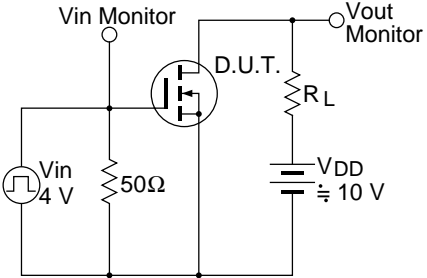




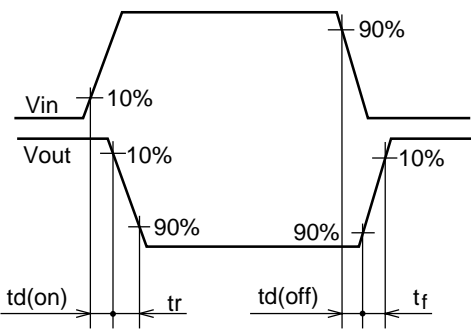




Switching Time Test Circuit

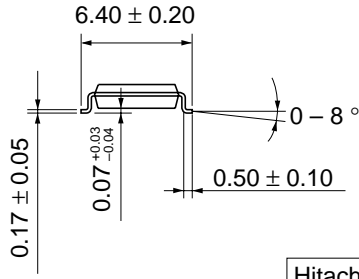
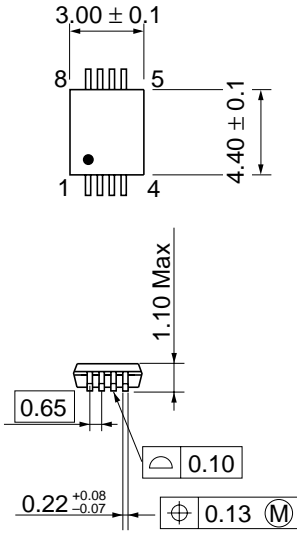


Switching Time Waveform



## Package Dimensions

Unit: mm



Hitachi Code	TTP-8D
EIAJ Code	—
JEDEC Code	—



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